EECE416: Microcomputer Fundamentals and Design

PIC - Introduction

PIC16F877

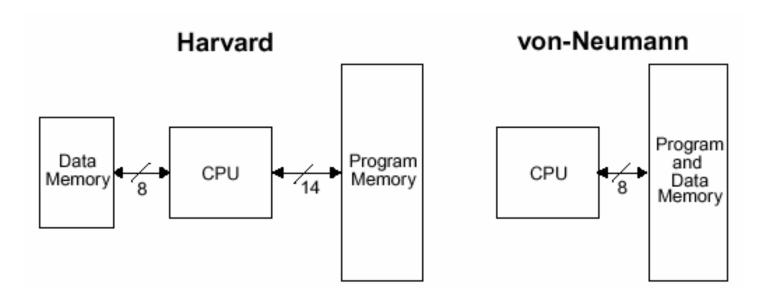
source: www.mwftr.com

Dr. Charles J. Kim

Howard University

Peripheral Interface Controller

- **#PIC:** Peripheral Interface Controller
- Microchip Technology (www.microchip.com)
- **#** Harvard Architecture



PIC- continued

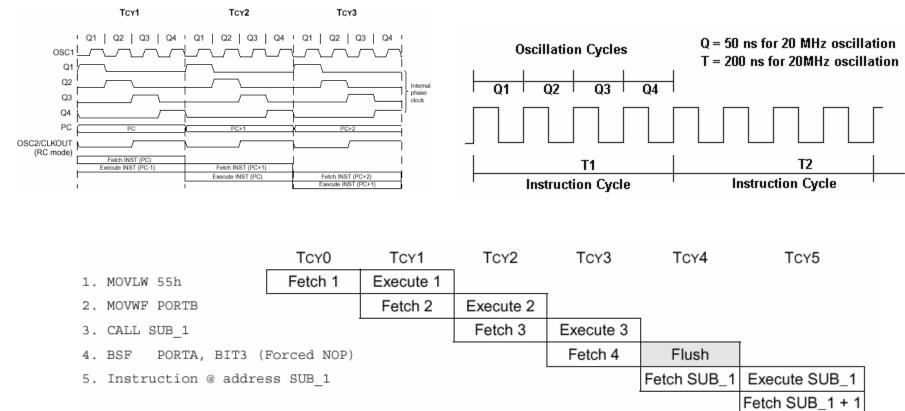
- **#**Origin: Harvard Architecture for DAPRA Project
 - Beaten by Princeton (Single memory)

 - PIC for General Instruments
 - Compensation for poor I/O
 - □GI spun off into Arizona Microchip
 Technology (1985)-→Microchip Technology



PIC -continued

- ★ A Large Register Set: 368 Bytes + W
- **RISC Architecture--pipelining**
- # 35 fixed length (14-bit) single-cycle instructions



PIC-continued

- # 8-bit machine
- # Operating Speed: Up to 20 MHz
- **38** 8K 14-bit Words FLASH Memory (for Program)
- # 368 Bytes RAM (for Data)
- # 256 Bytes EEPROM (for Data)
- # Power Saving Mode

 PIC 16 F817/R17A

 RESPONDED

 PIC 16 F817/R17A

 368 Bytes

256 Bytes

PIC -continued

- **#Low-power consumption:**
 - < 2 mA typical @ 5V, 4 MHz</p>
 - △20 mA typical @ 3V, 32 kHz
 - < 1 mA typical standby current</p>
- ₩ Wide Operating Voltage: 2.0 5.0 V
- **X** Timers
 - ☐ Timer0: 8-bit timer/counter with 8-bit prescaler
 - ☐ Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
 - ☐ Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler

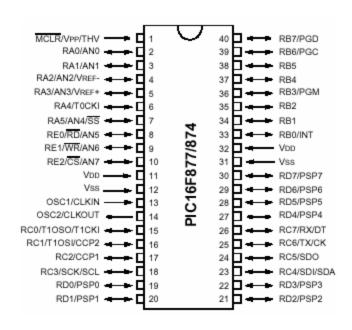
PIC -continued

- **#Capture, Compare, PWM modules**
 - Capture is 16-bit, max. resolution is 12.5 ns
 - Compare is 16-bit, max. resolution is 200 ns
 - PWM max. resolution is 10-bit
- #10-bit multi-channel A-to-D Converter
- ¥I²C (Inter IC)Bus
- **#USART** for Serial Communication
- #5 I/O Ports: A, B, C, D, and E

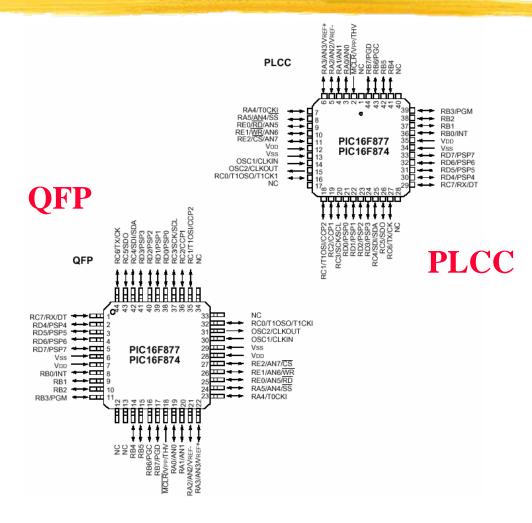
16F87x Family

Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F873	PIC16F874	PIC16F876	PIC16F877
Operating Frequency	DC - 20 MHz			
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	_	PSP	_	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Instruction Set	35 instructions	35 instructions	35 instructions	35 instructions

PIN and PACKAGE





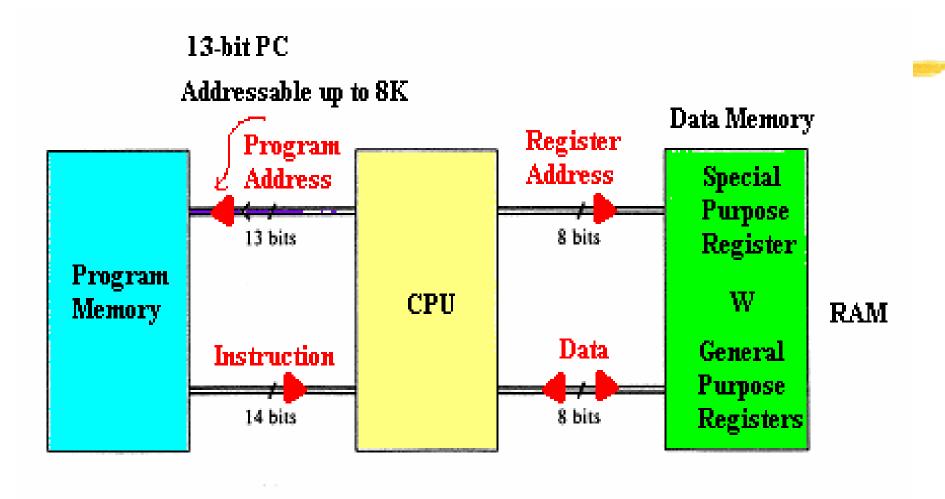


PIN

Pin Name	DIP Pin#	I/O/P Type	
OSC1/CLKIN	13	- 1	
OSC2/CLKOUT	14	0	
MCLR/VPP	1	I/P	
RA0/AN0	2	I/O	
RA1/AN1	3	I/O	
RA2/AN2/VREF-	4	I/O	
RA3/AN3/VREF+	5	I/O	
RA4/T0CKI	6	I/O	
RA5/SS/AN4	7	I/O	
RB0/INT	33	I/O	
RB1	34	I/O	
RB2	35	I/O	
RB3/PGM	36	I/O	
RB4	37	I/O	
RB5	38	I/O	
RB6/PGC	39	I/O	
RB7/PGD	40	I/O	

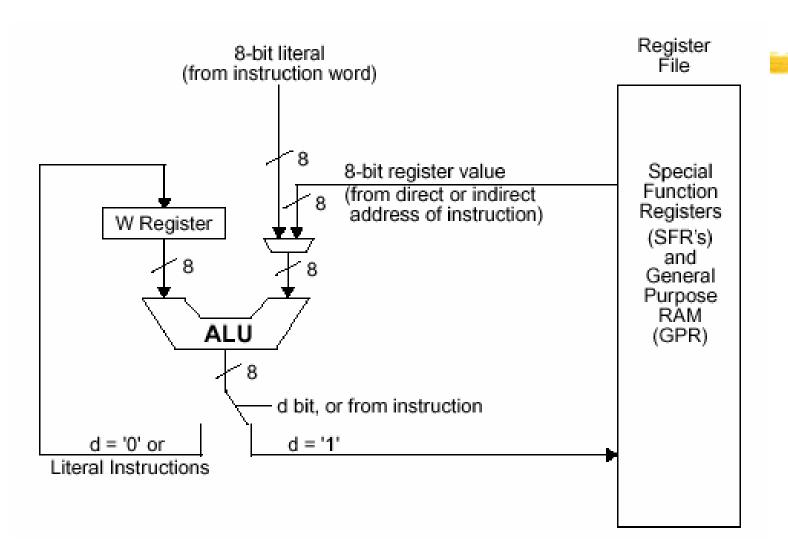
Pin Name	DIP Pin#	I/O/P Type
RC0/T10S0/T1CKI	15	I/O
RC1/T1OSI/CCP2	16	I/O
RC2/CCP1	17	1/0
RC3/SCK/SCL	18	1/0
RC4/SDI/SDA	23 24	1/0
RC5/SDO		1/0
RC6/TX/CK	25	1/0
RC7/RX/DT	26	I/O
RD0/PSP0	19	I/O
RD1/PSP1	20	I/O
RD2/PSP2	21	I/O
RD3/PSP3	22	I/O
RD4/PSP4	27	I/O
RD5/PSP5	28	I/O
RD6/PSP6	29	I/O
RD7/PSP7	30	I/O
RE0/RD/AN5	8	I/O
RE1/WR/AN6	9	I/O
RE2/CS/AN7	10	I/O
Vss	12,31	Р
VDD	11,32	Р

F877 Architecture



BLOCK Diagram PORTA 8 Data Bus Program Counter FLASH RA0/AN0 RA1/AN1 Program Memory RA2/AN2/VREF-RAM 8 Level Stack RA3/AN3/VREF+ File RA4/T0CKI (13-bit) Registers RA5/AN4/SS Program RAM Addr (1) PORTB Bus RB0/INT Addr MUX RB1 Instruction reg RB2 Indirect Direct Addr RB3/PGM Addr RB4 RB5 FSR reg RB6/PGC RB7/PGD STATUS reg PORTC RC0/T1OSO/T1CKI RC1/T1OSI/CCP2 RC2/CCP1 MUX Power-up RC3/SCK/SCL Timer RC4/SDI/SDA Oscillator RC5/SDO Instruction Start-up Timer Decode & RC6/TX/CK ALU Control RC7/RX/DT Power-on Reset PORTD Timing Watchdog Generation Timer OSC1/CLKIN Brown-out OSC2/CLKOUT RD7/PSP7:RD0/PSP0 Reset In-Circuit Debugger Low-Voltage Programming Parallel Slave Port PORTE RE0/AN5/RD 図 RE1/AN6/WR MCLR VDD, Vss X RE2/AN7/CS Timer0 Timer1 Timer2 10-bit A/D Data EEPROM Synchronous USART CCP1,2 Serial Port

ALU and W register



PROGRAM MEMORY

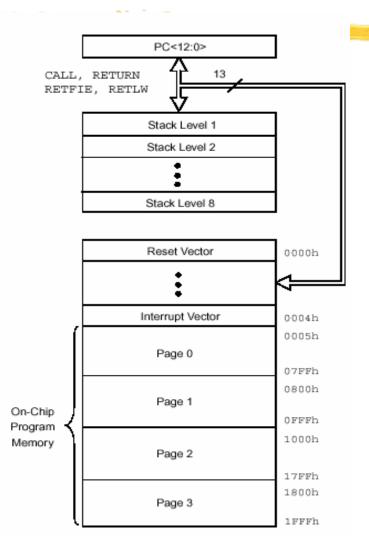
#13-bit PC

****Addressable up to 8Kx14-bit**

#FLASH Memory

Reset Vector: \$0000

#Interrupt: \$0004



DATA memory ("Register File")

- #Partitioned into 4 Banks (or Pages): 0-3
- #Each Bank: 128 Bytes
- **#Upper Locations: GPR (General Purpose) Reg.--**RAM
- **K**Lower Location: SFR (Special Function) Reg.
- **#BANK SELECTION:**

 - □RP1: Status < 6 >
 - □RP0: Status < 5 >

RP1:RP0	Bank
00	0
01	1
10	2
11	3

Register File Map

						A	Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD (1)	08h	TRISD (1)	88h		108h		188h
PORTE (1)	09h	TRISE (1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved ⁽²⁾	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h		90h		110h		190h
TMR2	11h	SSPCON2	91h		111h	l I	191h
T2CON	12h	PR2	92h		112h	l I	192h
SSPBUF	13h	SSPADD	93h		113h	l I	193h
SSPCON	14h	SSPSTAT	94h		114h	l I	194h
CCPR1L	15h		95h		115h	l I	195h
CCPR1H	16h		96h		116h	l I	196h
CCP1CON	17h		97h	General Purpose	117h	General	197h
RCSTA	18h	TXSTA	98h	Register	118h	Purpose Register	198h
TXREG	19h	SPBRG	99h	16 Bytes	119h	16 Bytes	199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh	l I	19Bh
CCPR2H	1Ch		9Ch		11Ch	l I	19Ch
CCP2CON	1Dh		9Dh		11Dh	l I	19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh	l I	19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
1						l I	
						I	
General Purpose		General Purpose		General Purpose		General Purpose	
Register		Register		Register		Register	
96 Bytes		80 Bytes	EE.	80 Bytes	4055	80 Bytes	1EFh
oo bytes		\vdash	EFh F0h		16Fh 170h		1F0h
		accesses	. 011	accesses 70h-7Fh	.,,	accesses 70h - 7Fh	
	7Fh	70h-7Fh	FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

File

^{*} Not a physical register.

Note 1: These registers are not implemented on 28-pin devices.

^{2:} These registers are reserved, maintain these registers clear.

Special Function Registers (bank 0)

Addres s	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 0	0										
00h(4)	INDF	Addressing	this location	uses conten	its of FSR to a	address data	memory (no	t a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	dule's registe	ır						XXXX XXXX	uuuu uuuu
02h ⁽⁴⁾	PCL	Program Co	ounter's (PC)	Least Signif	ficant Byte					0000 0000	0000 0000
03h(4)	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽⁴⁾	FSR	Indirect data	a memory ac	idress pointe	er.					XXXX XXXX	uuuu uuuu
05h	PORTA	_		'	ta Latch when	written: POF	TA pins who	en read		0x 0000	Ou 0000
06h	PORTB	PORTB Da	ta Latch whe		ORTB pins wh					XXXX XXXX	uuuu uuuu
07h	PORTC				ORTC pins wh					XXXX XXXX	uuuu uuuu
08h ⁽⁵⁾	PORTD	PORTD Da	ta Latch whe	en written: PO	ORTD pins wh	en read				XXXX XXXX	uuuu uuuu
09h(5)	PORTE	_	_	_	_	_	RE2	RE1	RE0	xxx	иии
0Ah(1,4)	PCLATH	_	_	_	Write Buffer	for the upper	5 bits of the	Program Co	ounter	0 0000	0 0000
0Bh(4)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTE	RBIF	0000 000x	0000 0001
0Ch	PIR1	PSPIF ⁽³⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	_	(6)	_	EEIF	BCLIF	_	_	CCP2IF	-x-0 00	-1-0 00
0Eh	TMR1L	Holding reg	jister for the l	Least Signific	cant Byte of th	e 16-bit TMR	1 register			хххх хххх	uuuu uuuu
0Fh	TMR1H	Holding reg	jister for the I	Most Signific	ant Byte of th	e 16-bit TMR	1 register			XXXX XXXX	uuuu uuuu
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	dule's registe	ır.						0000 0000	0000 0000
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR20N	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	us Serial Por	t Receive Bu	ffer/Transmit I	Register				XXXX XXXX	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	l Register1 (l	LSB)					XXXX XXXX	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	l Register1 (I	MSB)					XXXX XXXX	uuuu uuuu
17h	CCP1CON	_	_	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	USART Tra	USART Transmit Data Register								0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								XXXX XXXX	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								XXXX XXXX	uuuu uuuu
1Dh	CCP2CON	_	_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh	ADRESH	A/D Result	Register Hig	h Byte						XXXX XXXX	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/ DONE	_	ADON	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

- Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.
- 3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.
- 4: These registers can be addressed from any bank.
- PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.
- 6: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

Special Function Registers (bank 1)

Addres s	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 1											
80h ⁽⁴⁾	INDF	Addressing	this location	uses conten	its of FSR to a	address data	memory (no	t a physical	register)	0000 0000	0000 0000
81h	OPTION_R EG	RBPU	INTEDG	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(4)	PCL	Program Co	ounter's (PC)	Least Signif	ficant Byte					0000 0000	0000 0000
83h(4)	STATUS	IRP	RP1	RP0	TO	DE	Z	DC	C	0001 1xxx	000g guuu
84h(4)	FSR	Indirect dat	a memory ac	dress pointe	er				•	XXXX XXXX	uuuu uuuu
85h	TRISA	_	_		ta Direction R	egister				11 1111	11 1111
86h	TRISB	PORTB Da	ta Direction F							1111 1111	1111 1111
87h	TRISC	PORTC Da	ta Direction F	Register						1111 1111	1111 1111
88h(5)	TRISD	PORTD Da	ta Direction f	Register						1111 1111	1111 1111
89h(5)	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE	Data Direc	tion Bits	0000 -111	0000 -111
8Ah(1.4)	PCLATH	_	_	_	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	0 0000
8Bh(4)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTE	RBIF	0000 000x	DD00 000u
8Ch	PIE1	PSPIE ⁽³⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	_	(6)	_	EEIE	BCLIE	_	_	CCP2IE	-r-0 00	-x-0 00
8Eh	PCON	_		_	_	_	_	POR	BOR	qq	
8Fh	_	Unimpleme	nted							_	_
90h	_	Unimpleme	nted							_	_
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
92h	PR2	Timer2 Peri	iod Register							1111 1111	1111 1111
93h	SSPADD	Synchronou	is Serial Port	t (I ² C mode)	Address Reg	ister				0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
95h	_	Unimpleme	nted							_	_
96h	_	Unimpleme	nted							_	_
97h	_	Unimpleme	nted							_	_
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generator R	egister						0000 0000	0000 0000
9Ah	_	Unimpleme	Unimplemented								_
9Bh	_	Unimpleme	nted							_	_
9Ch	_	Unimpleme	nted							_	_
9Dh	_	Unimpleme	nted							_	_
9Eh	ADRESL	A/D Result	Register Low	r Byte						XXXX XXXX	uuuu uuuu
9Fh	ADCON1	ADFM	_	_	_	PCFG3	PCFG2	PCFG1	PCFG0	0 0000	0 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

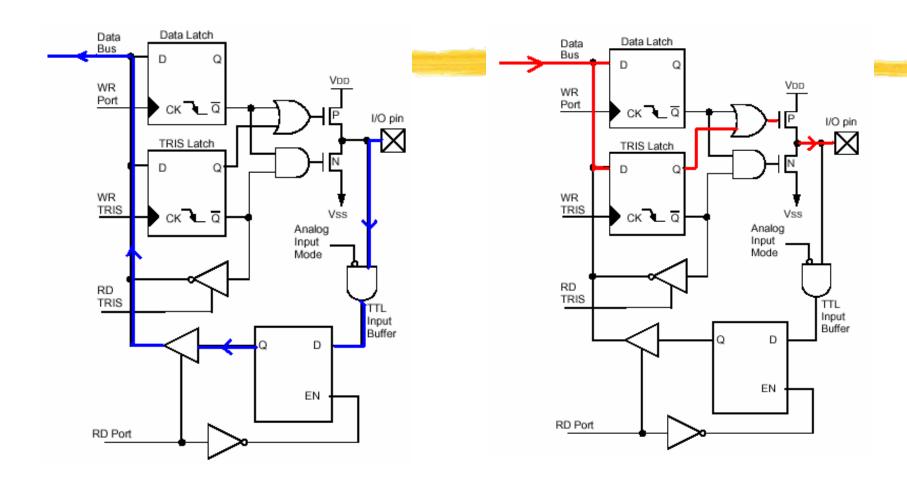
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 - 3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.
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 - 5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.
 - 6: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

Special Function Registers(bank 2 & 3)

Addres s	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 2											
100h ⁽⁴⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register) 00									
101h	TMR0	Timer0 mod	dule's registe	r						жжж жжж	uuuu uuuu
102h ⁽⁴⁾	PCL	Program Co	ounter's (PC)	Least Signil	ficant Byte					0000 0000	0000 0000
103h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	z	DC	С	0001 1xxx	000q quuu
104h ⁽⁴⁾	FSR	Indirect dat	a memory ad	ddress pointe	er					XXXX XXXX	uuuu uuuu
105h	_	Unimpleme								_	_
106h	PORTB	PORTB Da	ta Latch whe	n written: Po	ORTB pins wh	en read				XXXX XXXX	uuuu uuuu
107h	_	Unimpleme	nted							_	_
108h	_	Unimpleme	nted							_	_
109h	_	Unimpleme	nted							_	_
10Ah(1.4)	PCLATH	_	_	_	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	0 0000
10Bh ⁽⁴⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTE	RBIF	0000 000x	0000 000ш
10Ch	EEDATA	EEPROM d	ata register	•		•			•	XXXX XXXX	uuuu uuuu
10Dh	EEADR	EEPROM a	ddress regis	ter						жжж жжж	uuuu uuuu
10Eh	EEDATH	_	_	EEPROM o	tata register hi	igh byte				жжж жжж	uuuu uuuu
10Fh	EEADRH	_	_	_	EEPROM ac	ldress registe	r high byte			XXXX XXXX	uuuu uuuu
Bank 3											
180h ⁽⁴⁾	INDF	Addressing	this location	uses conter	nts of FSR to a	address data	memory (no	t a physical	register)	0000 0000	0000 0000
181h	OPTION_R EG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h ⁽⁴⁾	PCL	Program Co	ounter's (PC)	Least Sign	nificant Byte					0000 0000	0000 0000
183h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
184h ⁽⁴⁾	FSR	Indirect dat	a memory ac	idress pointe	er.					жжж жжж	uuuu uuuu
185h	_	Unimpleme	nted							_	_
186h	TRISB	PORTB Da	ta Direction I	Register						1111 1111	1111 1111
187h	_	Unimplemented									_
188h	_	Unimplemented								_	_
189h	_	Unimplemented								_	_
18Ah ^(1,4)	PCLATH	Write Buffer for the upper 5 bits of the Program Counter							ounter	0 0000	0 0000
18Bh ⁽⁴⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTE	RBIF	0000 000x	0000 000ш
18Ch	EECON1	EEPGD WRERR WREN WR RD									x u000
18Dh	EECON2	EEPROM o	ontrol registe	er2 (not a ph	ysical register)					
18Eh	_	Reserved n	naintain dea	r						0000 0000	0000 0000
18Fh	_	Reserved n	naintain dea	r						0000 0000	0000 0000

- Legend: x = unknown, u = unchanged, q = value depends on condition, = unimplemented read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.
- Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
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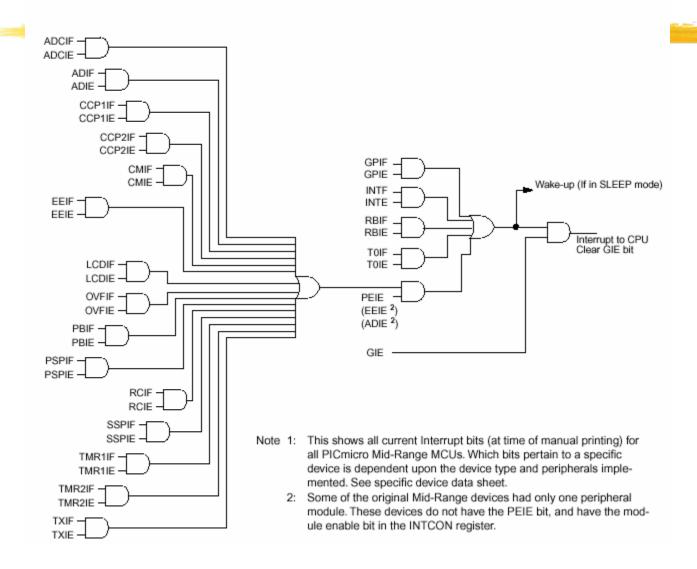
Input/Output Ports



Interrupts

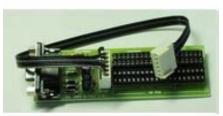
PIR/PIE Registers

INTCON Register



16F877 Hex Code Download









Boot Loader Option

Bootstrap loader

Also known as **bootstrapping** or **boot loader**, a **bootstrap** loader is a <u>program</u> that resides in the computers <u>EPROM</u>, <u>ROM</u>, or other <u>non-volatile memory</u> that automatically executed by the processor when the computer is turned on. The bootstrap loader reads the <u>hard disk</u> <u>drives</u> boot sector to continue the process of loading the computers <u>Operating System</u>.

boot loader

A small <u>program</u> that loads the <u>operating system</u> into the computer's <u>memory</u> when the <u>system</u> is <u>booted</u> and also starts the <u>operating system</u>.

bootstrap

noun 1 a loop at the back of a boot, used to pull it on. 2
 Computing the action of loading a program into a computer by means of a few initial instructions which enable the introduction of the rest of the program from an input device.

boot-strap

noun (plural boot-straps)

Definition:

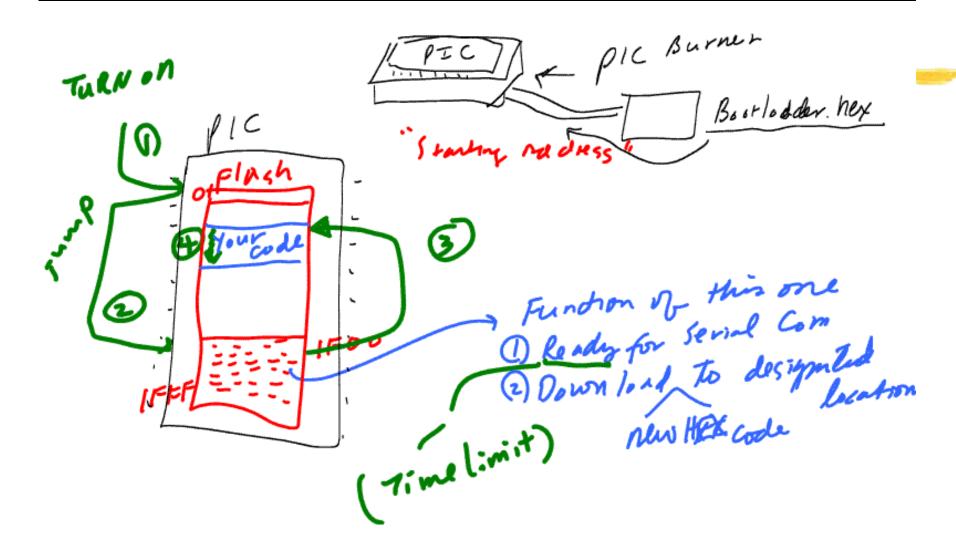
loop attached to boot: a leather or fabric loop on the back or side of a boot to help pull it on

adjective

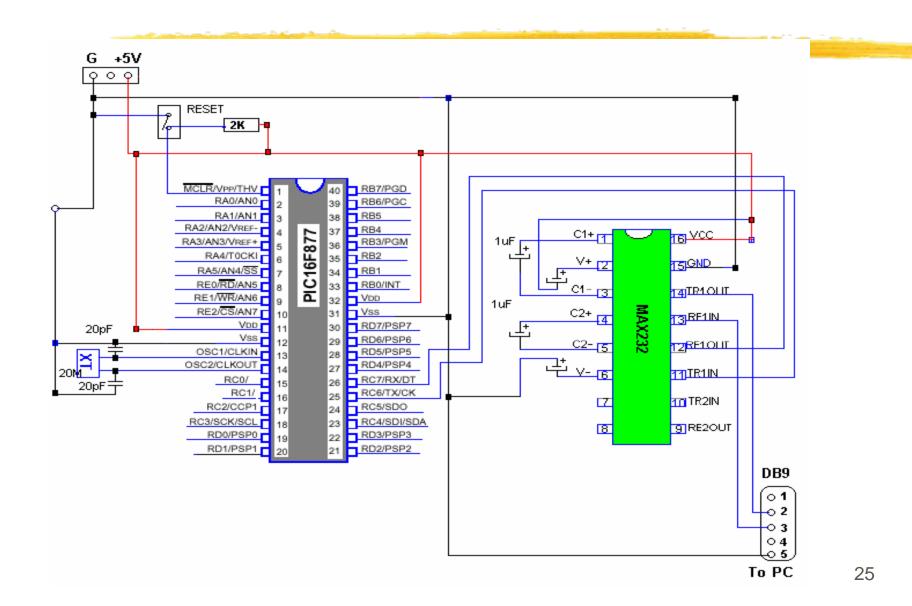
Definition:

self-reliant and self-sustaining: relying solely on somebody's own efforts and resources

PIC16F877 Bootloader



Minimum Hardware for Boot Loaded Platform

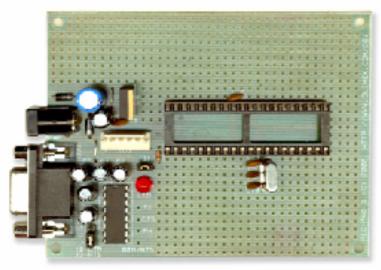


Commercially Available PIC16F877 Board

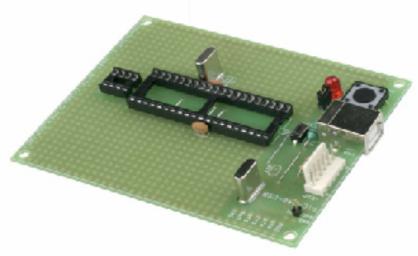


www.olimex.com >>>Proto Board

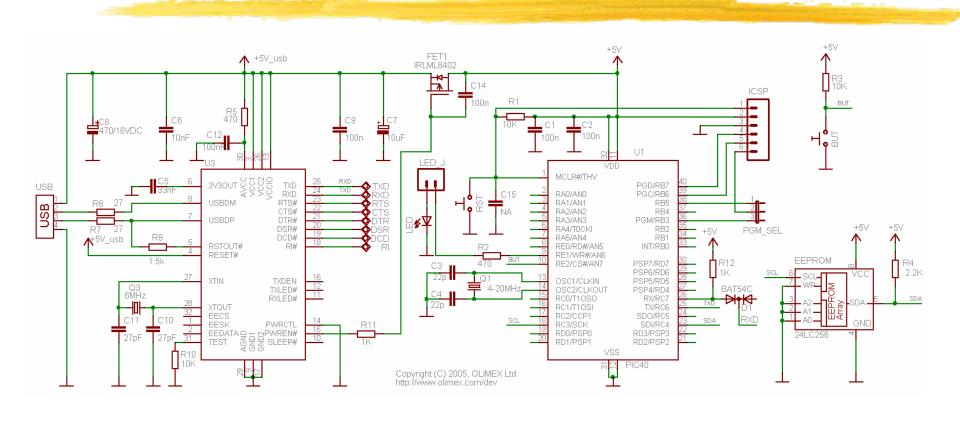
PIC-40B



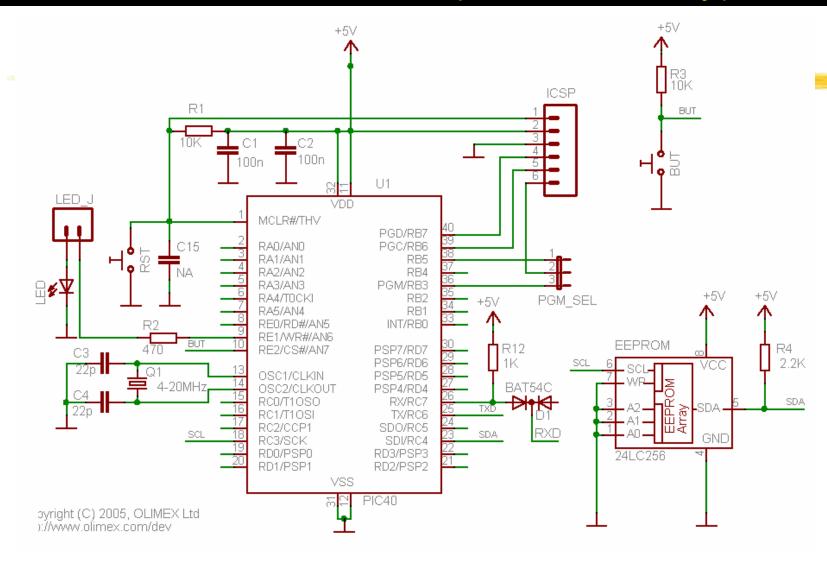
PIC-40B-USB



PIC-40B-USB Schematic



PIC-40B-USB Schematic (PIC area only)



Other PIC Board (Not fully evaluated yet)

- # DLP-245PB-G-USB
- **X** Not evaluated
- # Problem in Bootloader downloading
- # Problem in USB driver with Windows

