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EECE416 Microcomputer Fundamentals

68000 Processor

1. Chip Signal Description

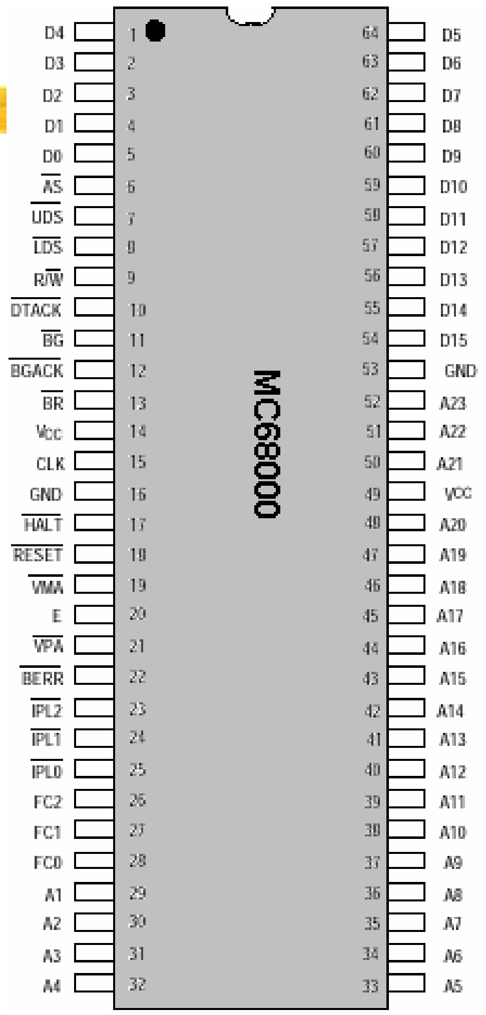
2. Instruction and Programming

Dr. Charles Kim

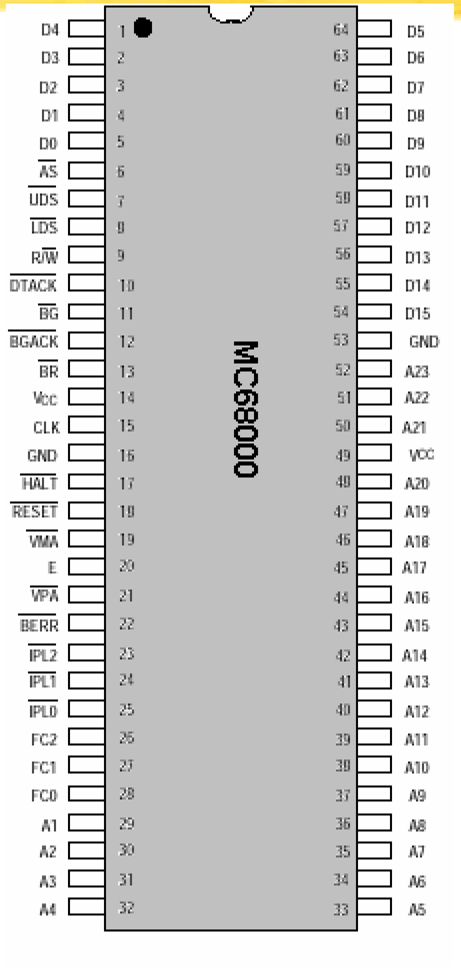
Howard University

68000 Microprocessor

- 64 pins
- 32- bit Data and Address Registers
- 16- bit Data Bus
- 24- bit Address Bus (16MB)
- 14 Addressing Modes
- Memory- Mapped Input/ Output
- Program Counter (PC)
- 5 Main Data Types- *L, W, B, b, BCD*
- 7 interrupt levels
- Clock speeds: 4MHz to 12.5MHz
- Synchronous and asynchronous data transfers

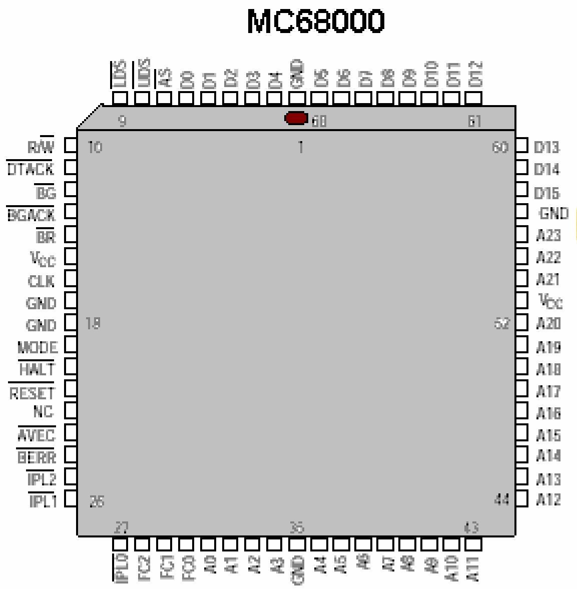


PIN and PACKAGE



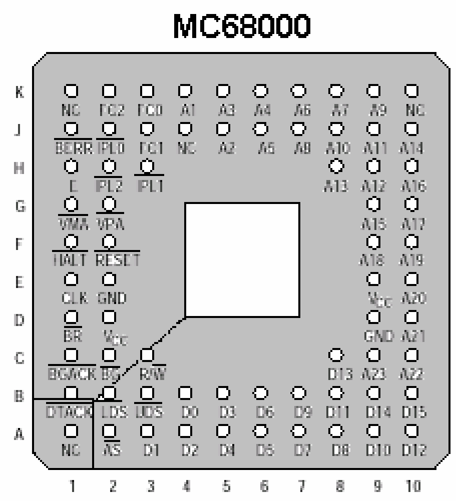
DIP

PLCC


MC68000
LDS UDS AS D0 D1 D2 D3 D4 GND D5 D6 D7 D8 D9 D10 D11 D12
9 68 61
R/W DTACK BG BGACK BR Vcc CLK GND GND MODE HALT RESET NC AVEC BERR IPL2 IPL1
10 1 60
18 52
26 44
27 35 43
D13 D14 D15 GND A23 A22 A21 Vcc A20 A19 A18 A17 A16 A15 A14 A13 A12
IPL0 FC2 FC1 FC0 A0 A1 A2 A3 GND A4 A5 A6 A7 A8 A9 A10 A11

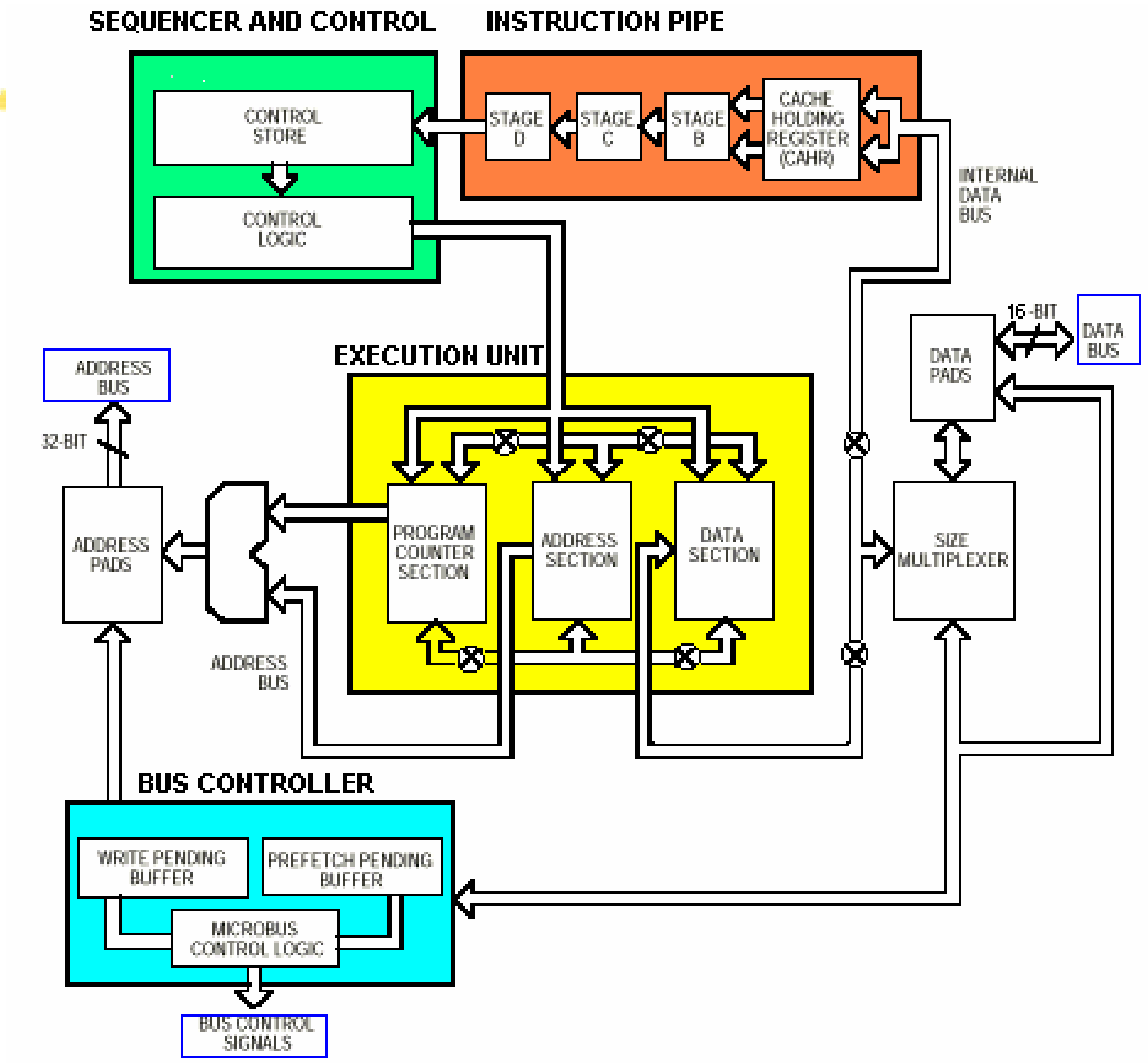
* Top View

PLCC Socket

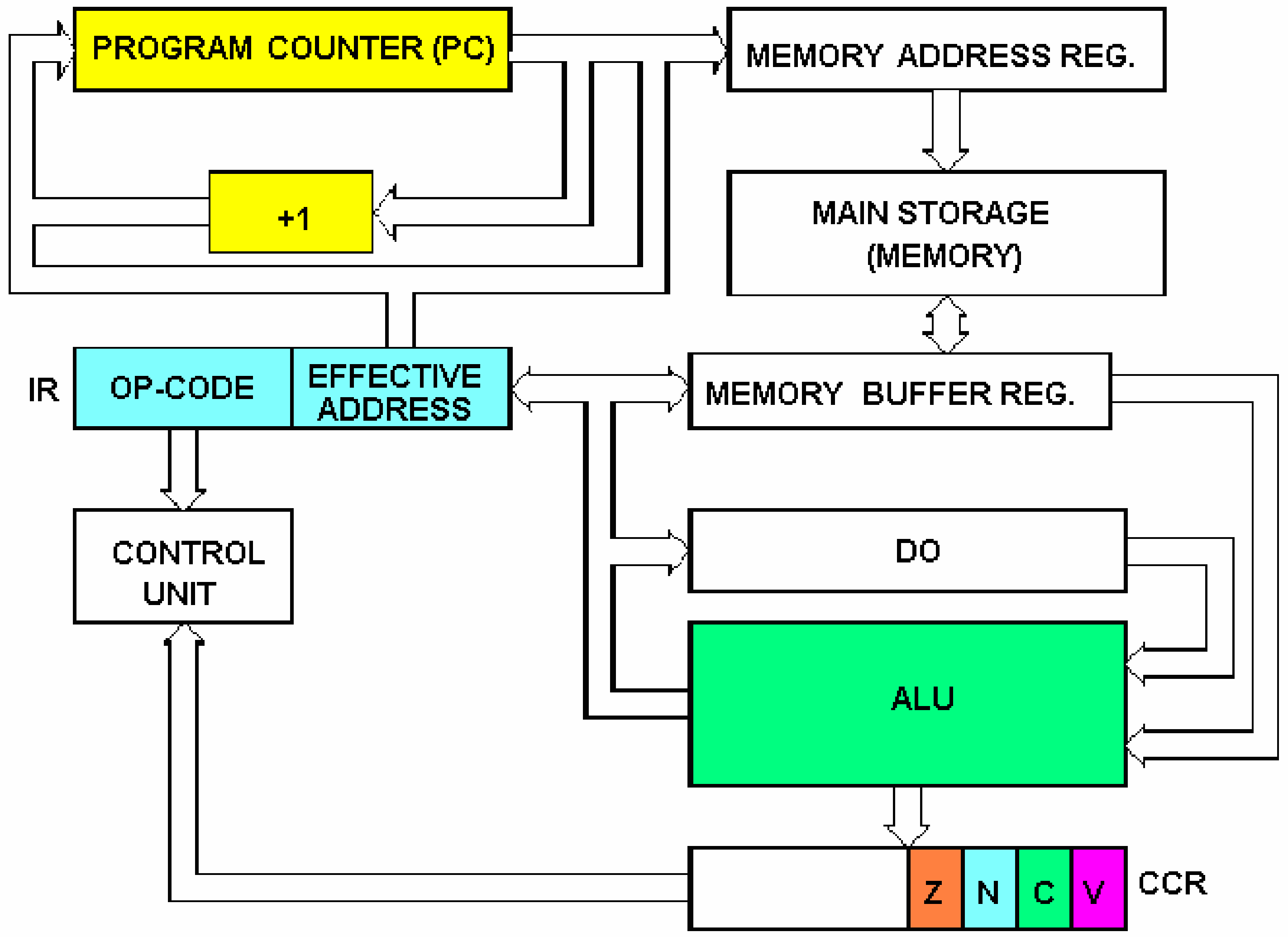

MC68000
K NC FC2 FC0 A1 A3 A4 A6 A7 A9 NC
J BERR IPL0 FC1 NC A2 A5 A8 A10 A11 A14
H E IPL2 IPL1 A13 A12 A16
G VMA VPA A15 A17
F HALT RESET A18 A19
E CLK GND Vcc A20
D BR Vcc GND A21
C BGACK BG R/W D13 A23 A22
B DTACK LDS UDS D0 D3 D6 D9 D11 D14 D15
A NC AS D1 D2 D4 D5 D7 D8 D10 D12
1 2 3 4 5 6 7 8 9 10

* Bottom View

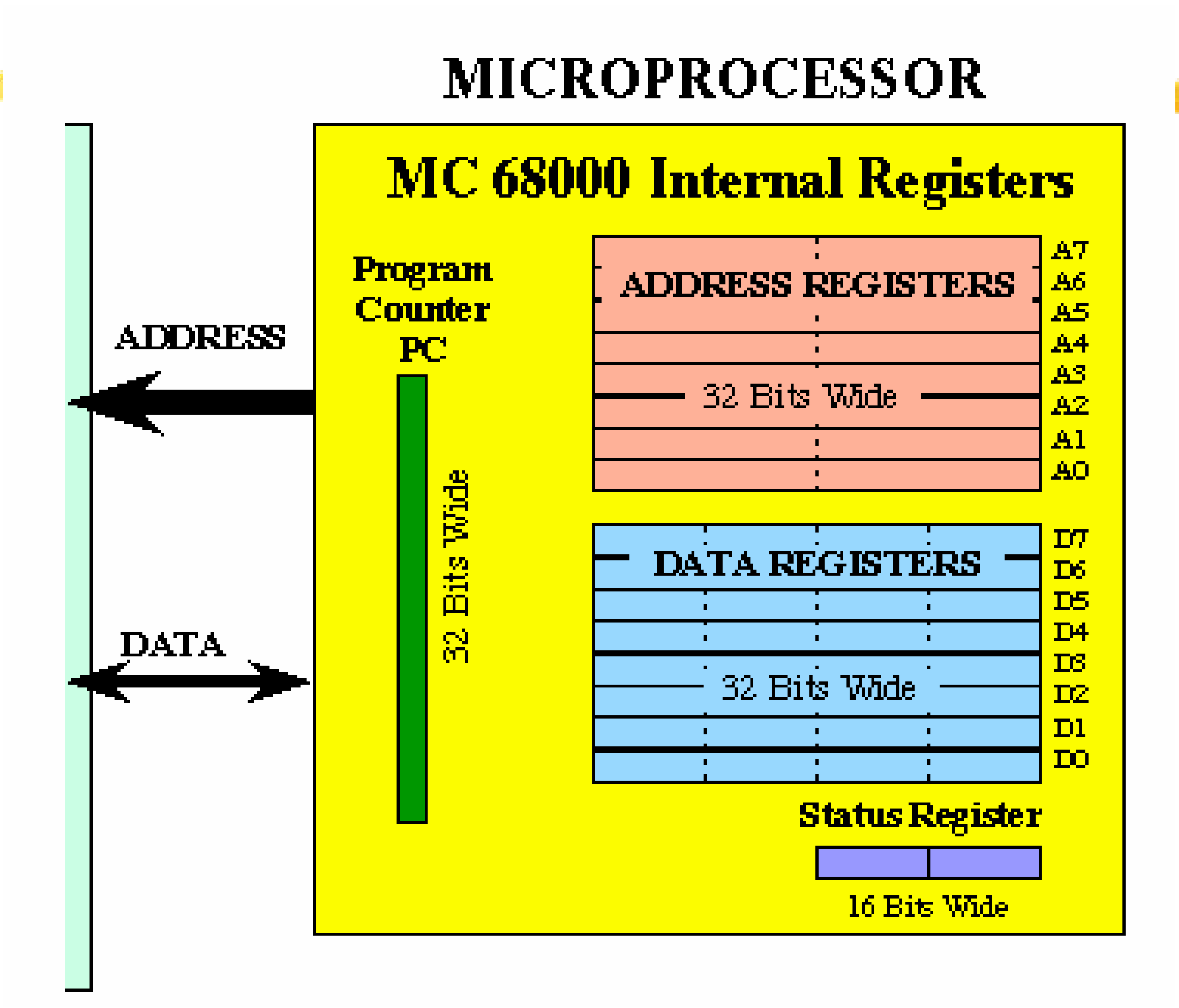
BLOCK Diagram



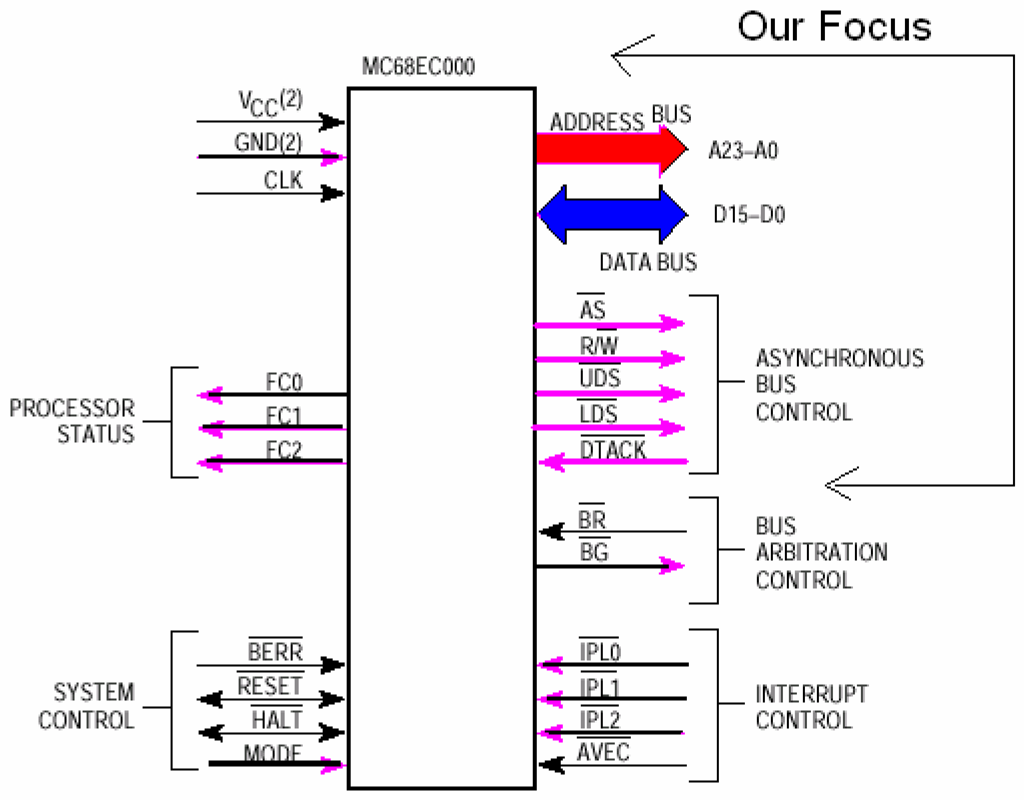
Core Structure

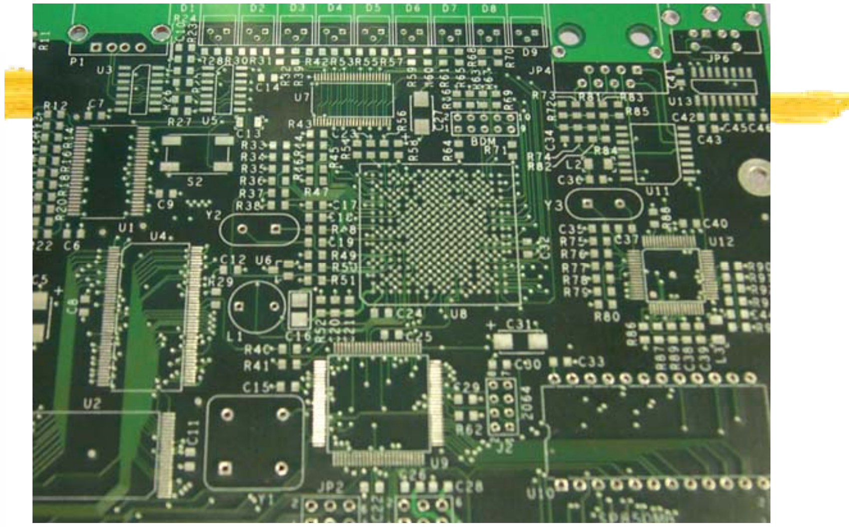


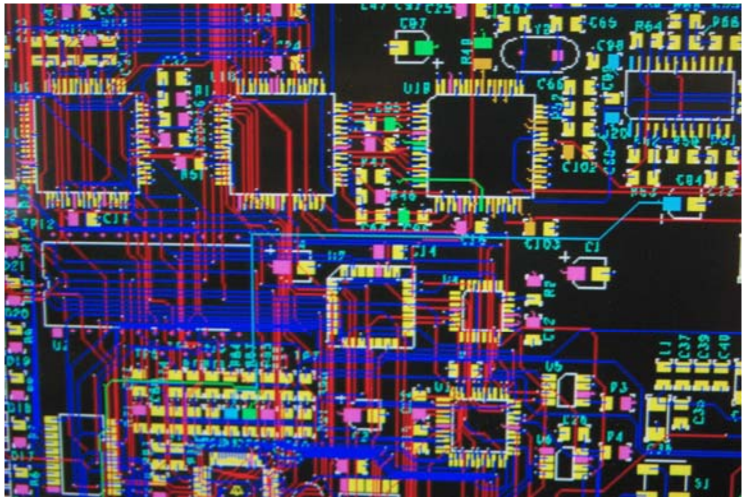
Internal Structure - Registers



Connecting with Memory, I/O, and Peripherals

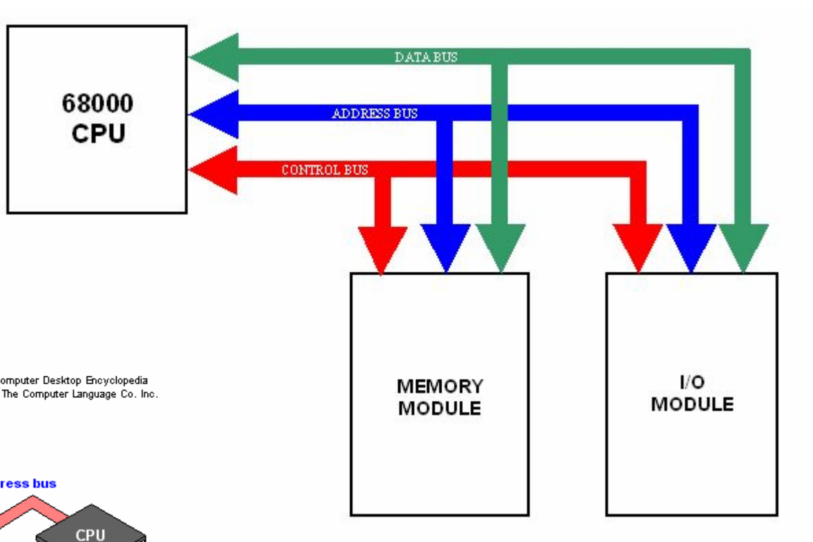


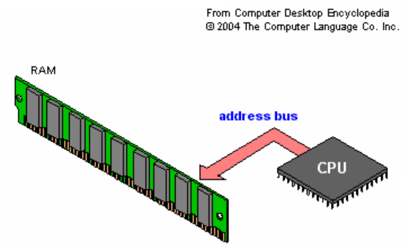




SIGNAL DESCIRPTION

- **1. ADDRESS BUS (A23–A1)**
  - **23-bit, unidirectional, three state bus**
  - capable of addressing 16 Mbytes of data.




From Computer Desktop Encyclopedia
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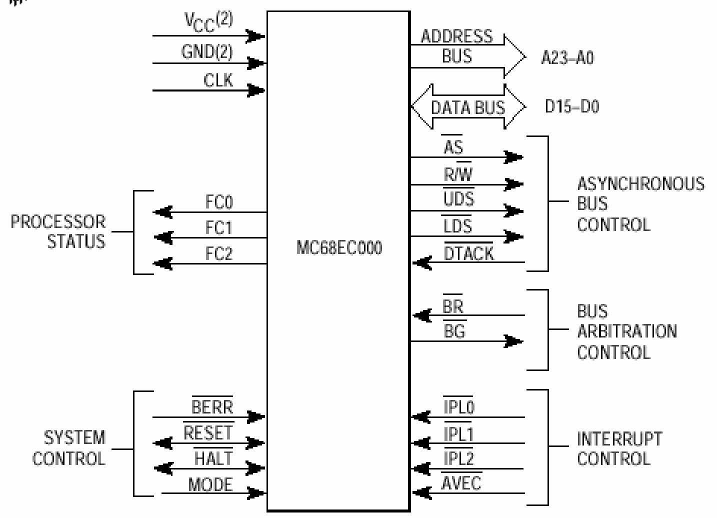
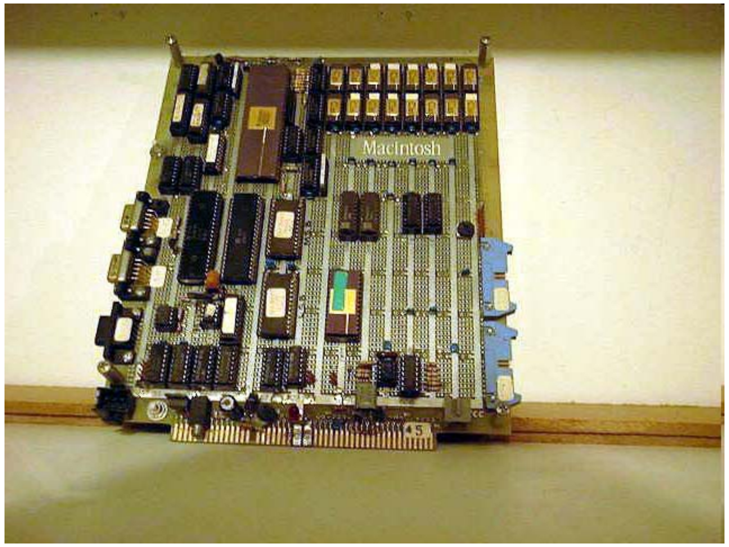
RAM
address bus
CPU

- **2. DATA BUS (D15–D0)**
  - **bidirectional, three-state bus**
  - general-purpose data path of 16 bits wide
  - transfer data of either word or byte length.



Apple Mac

- CPU: 8MHz Motorola 68000
- Introduced in 1984
- Memory: 128KB (512KB in later version) RAM, 64KB ROM
- 3.5” 400KB Floppy Disk
- Application: MacWrite and MacPaint
- Mouse
- 9” B&W Monitor
- Keyboard
- Serial Port (DB-9)
- Printer Port
- Addressing: 24-bit



Apple Mac Circuit Diagram

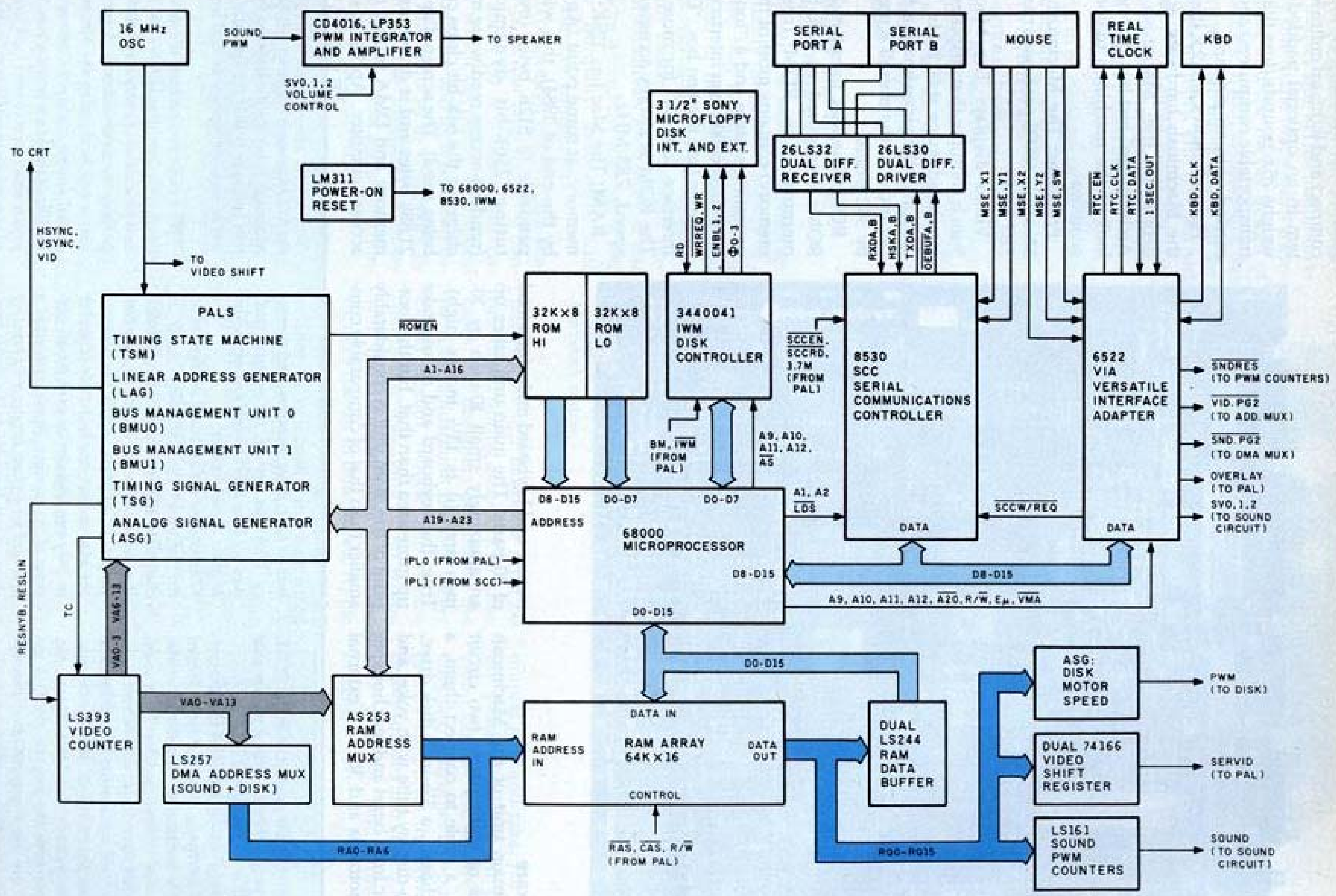
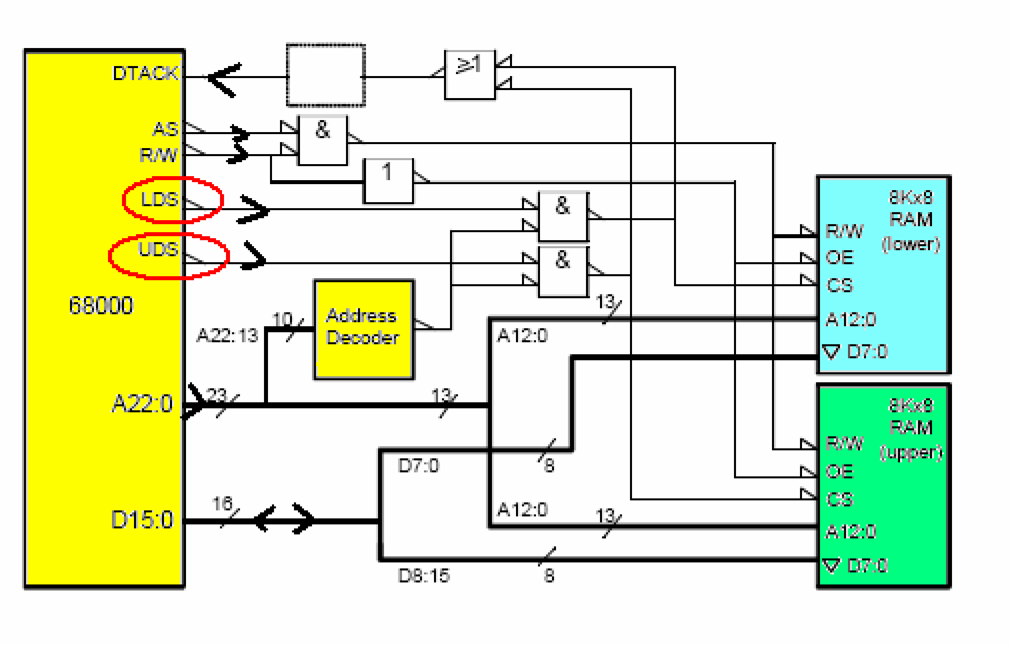


Figure 2: A block diagram of the Macintosh hardware. For more details, see the "Macintosh System Architecture" text box.

Signal Description

- **3. ASYNCHRONOUS BUS CONTROL**
  - **Address Strobe (~AS).**
    - This three-state signal indicates that the information on the address bus is a valid address.
  - **Read/Write (R/~W).**
    - This three-state signal defines the data bus transfer as a read or write cycle.
  - **Upper And Lower Data Strobes (~UDS, ~LDS).**
  - **Data Transfer Acknowledge (~DTACK).**
    - **This input signal indicates the completion of the data transfer.**

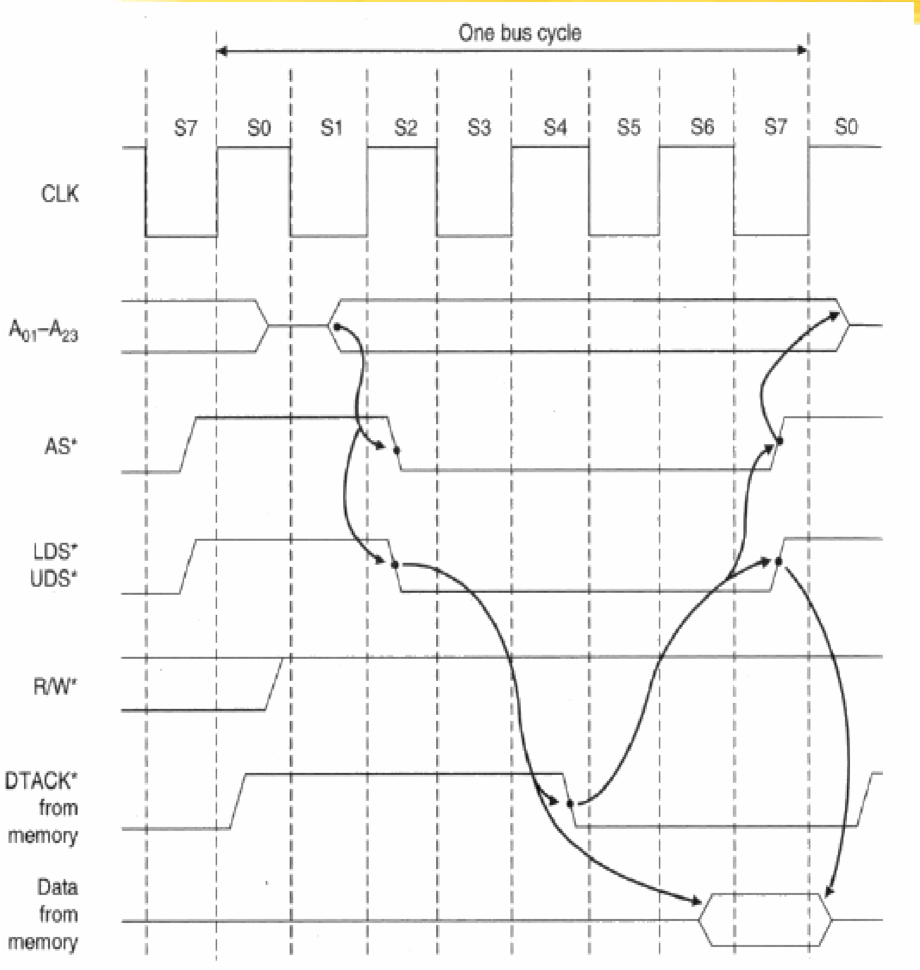
Strobe: a signal that is sent to validates data or other signals

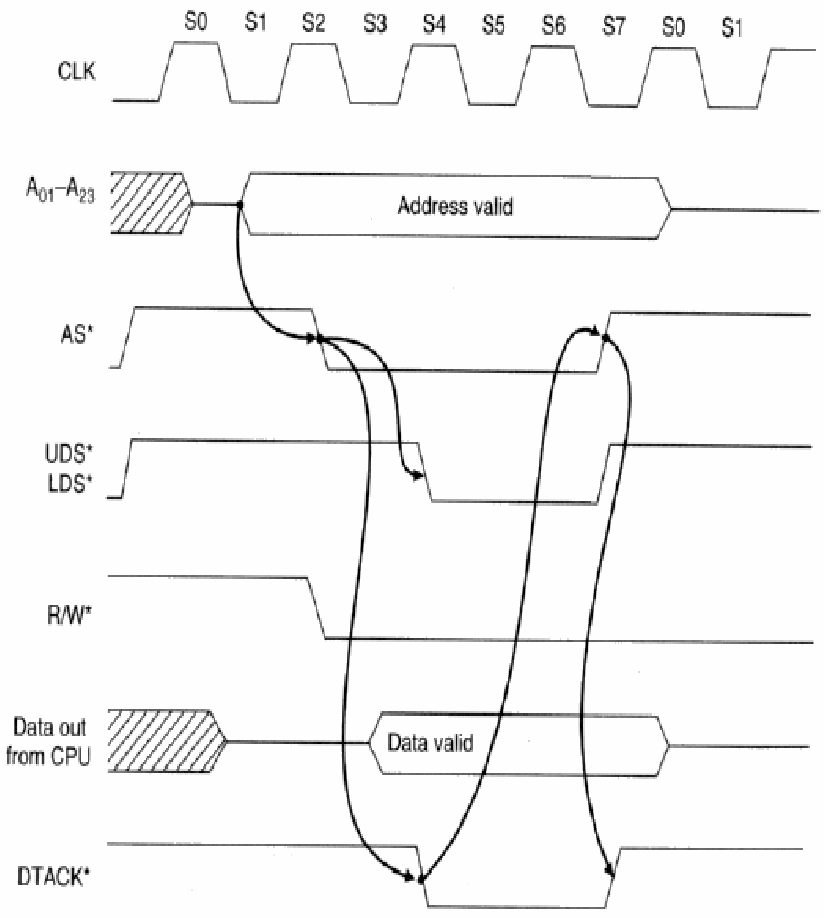


Memory Access Timing

- Read (to CPU) Cycle

Write (to Mem) Cycle



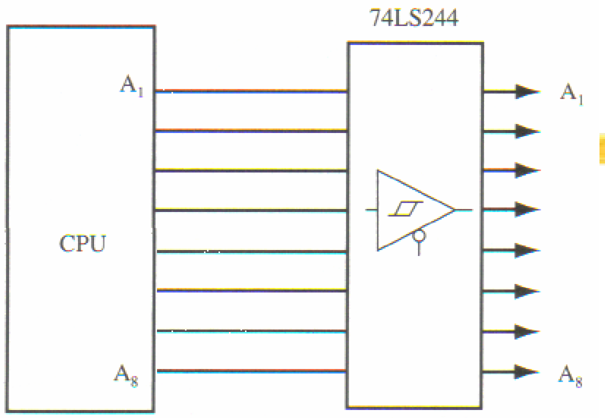


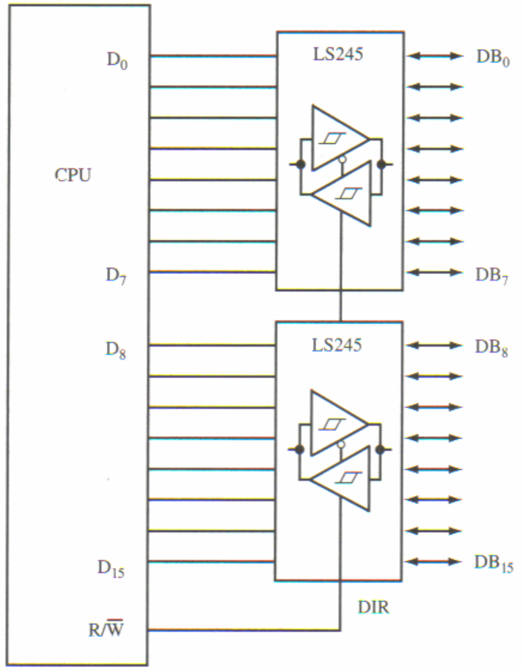
Other Signals

- **4. BUS ARBITRATION CONTROL**
  - **Bus Request (**~BR**)**
  - **Bus Grant (**~BG**)**
  - **Bus Grant Acknowledge (**~BGACK**)**
- **5. INTERRUPT CONTROL (**IPL0**,**IPL1**,**IPL2**)**
  - These input signals indicate the **encoded priority level of the device requesting** an interrupt.
  - **Level seven**, which cannot be masked, has the highest priority; level zero indicates that no interrupts are requested.
  - IPL0 is the least significant bit of the encoded level, and IPL2 is the most significant bit**.**
- **6. SYSTEM CONTROL**
  - **Bus Error (**~BERR**)**
  - **Reset (**~RESET**)**
    - The processor assertion of ~RESET (from executing a ~RESET instruction) **resets all external devices** of a system without affecting the internal state of the processor.
  - **Halt (**~HALT**)**
    - An input to this bidirectional signal causes the **processor to stop bus activity** at the completion of the current bus cycle.
- **7. M6800 PERIPHERAL CONTROL**
  - **Enable (E)**
  - **Valid Peripheral Address (**~VPA**)**
  - **Valid Memory Address (**~VMA**)**
- **8. PROCESSOR FUNCTION CODES (FC0, FC1, FC2)**
- **9. CLOCK (CLK): 8MHz**
- **10. POWER SUPPLY (V_{CC} and GND)**

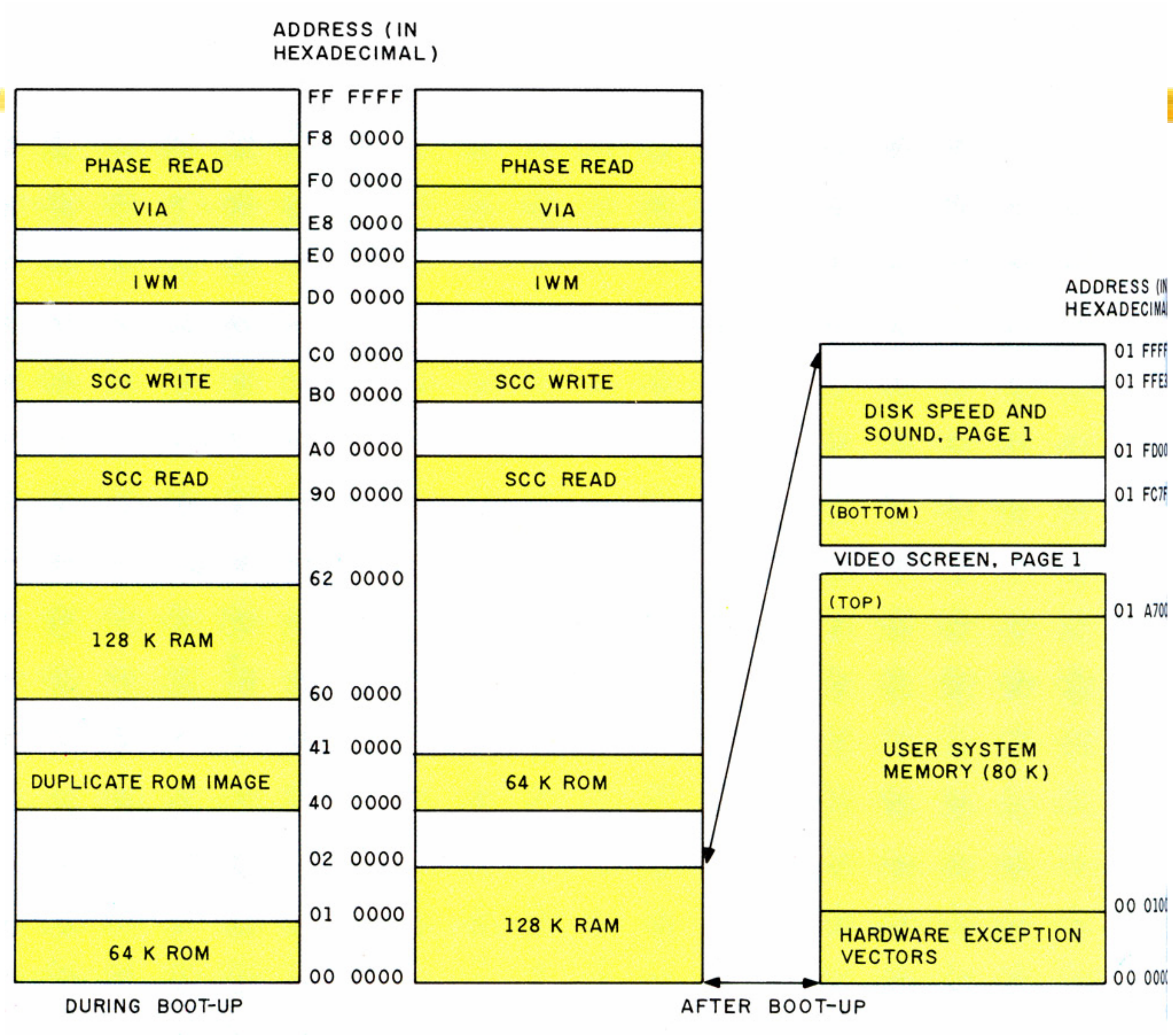
Memory Address Decoding

- Memory Bus
  - Control
  - Data (Bi-directional)
  - Address (Unidirectional)
- Address Bus Buffering
  - Fan Out
  - 74LS244 Octal line driver/receiver
- Data Bus Buffering
  - R/W for Direction
  - Fan Out
  - 74LS245 Octal Bus Transceiver



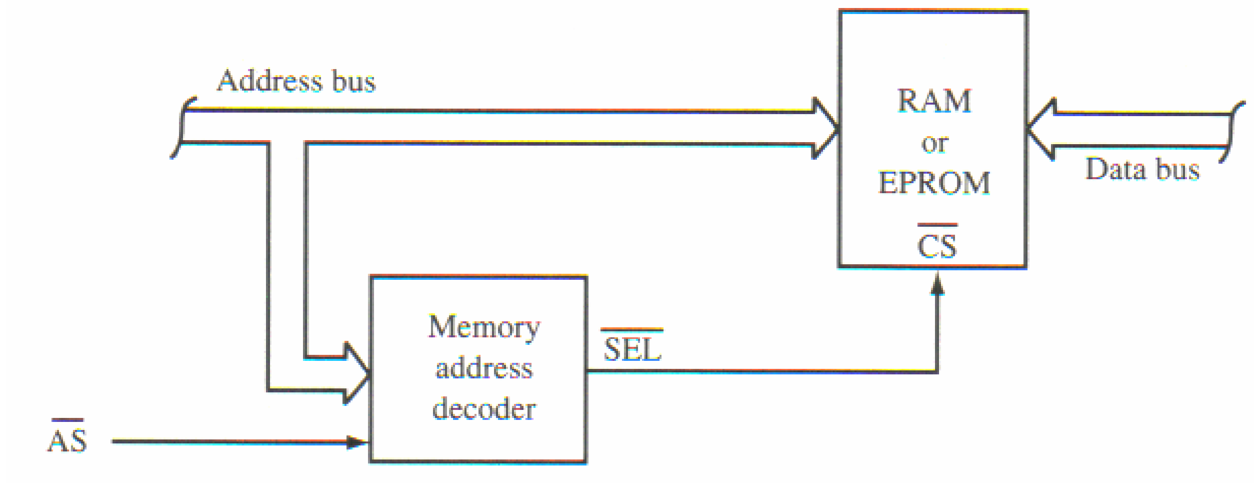


Memory Map (for Apple Mac)



Memory Address Decoding

- How Much Memory?
- How Many Address Lines?
- 1K → 10 lines
- 32K → 15 lines
- 23 ADDR lines → 8MB?

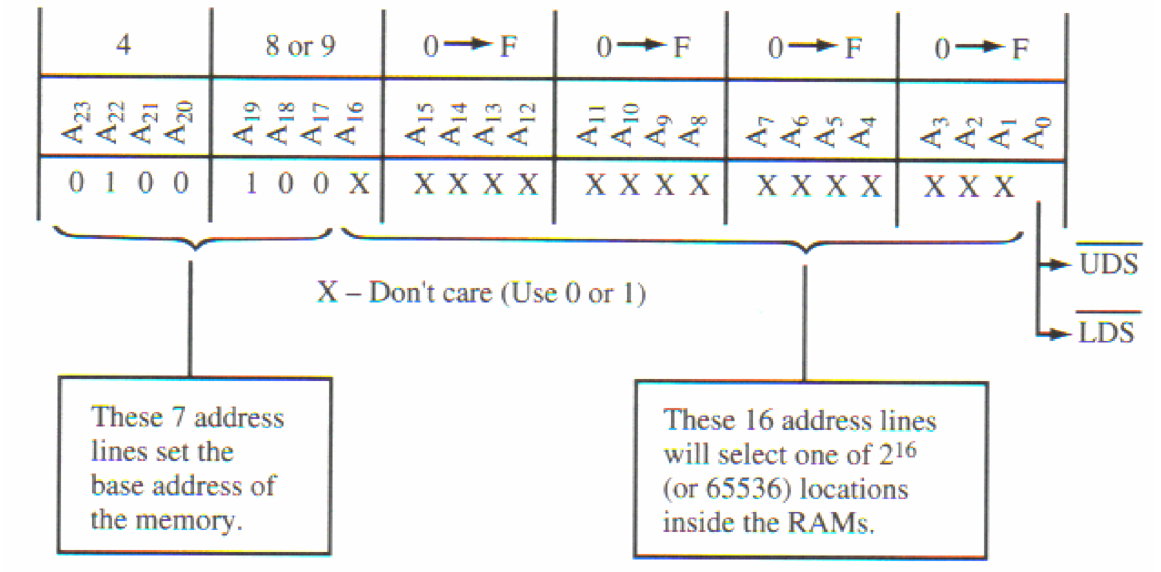


UDS and LDS

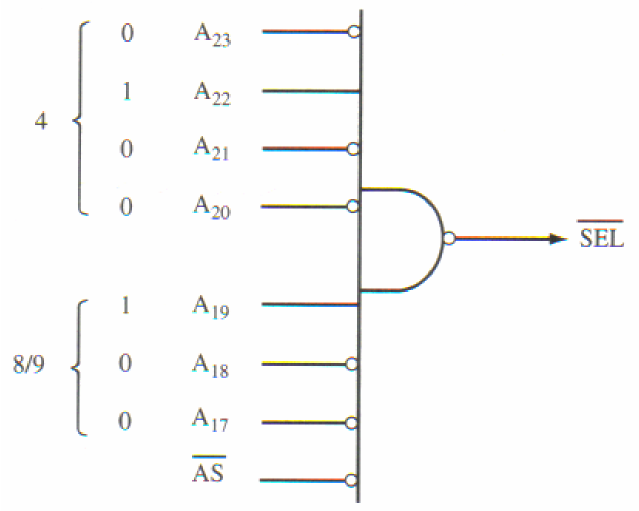
- Upper Data Strobe
  - For accessing upper byte of memory
  - D15 – D8 part of CPU
  - D7 – D0 part of memory
- Lower Data Strobe
  - For accessing lower byte of memory
  - D7-D0 part of CPU
  - D7 – D0 part of Memory
- Both together works as A0 line

Memory Decoding

- Q: 64K Word (or 128 KB) of RAM, with it’s starting address at $480000
- A: 128KB → 17 lines
  - Range: $480000 - $49FFFF
  - UDS and LDS for A_0 line.



4
8 or 9
0 → F
0 → F
0 → F
0 → F
A23 A22 A21 A20
A19 A18 A17 A16
A15 A14 A13 A12
A11 A10 A9 A8
A7 A6 A5 A4
A3 A2 A1 A0
0 1 0 0
1 0 0 X
X X X X
X X X X
X X X X
X X X
UDS
LDS
X – Don't care (Use 0 or 1)
These 7 address lines set the base address of the memory.
These 16 address lines will select one of 2^16 (or 65536) locations inside the RAMs.

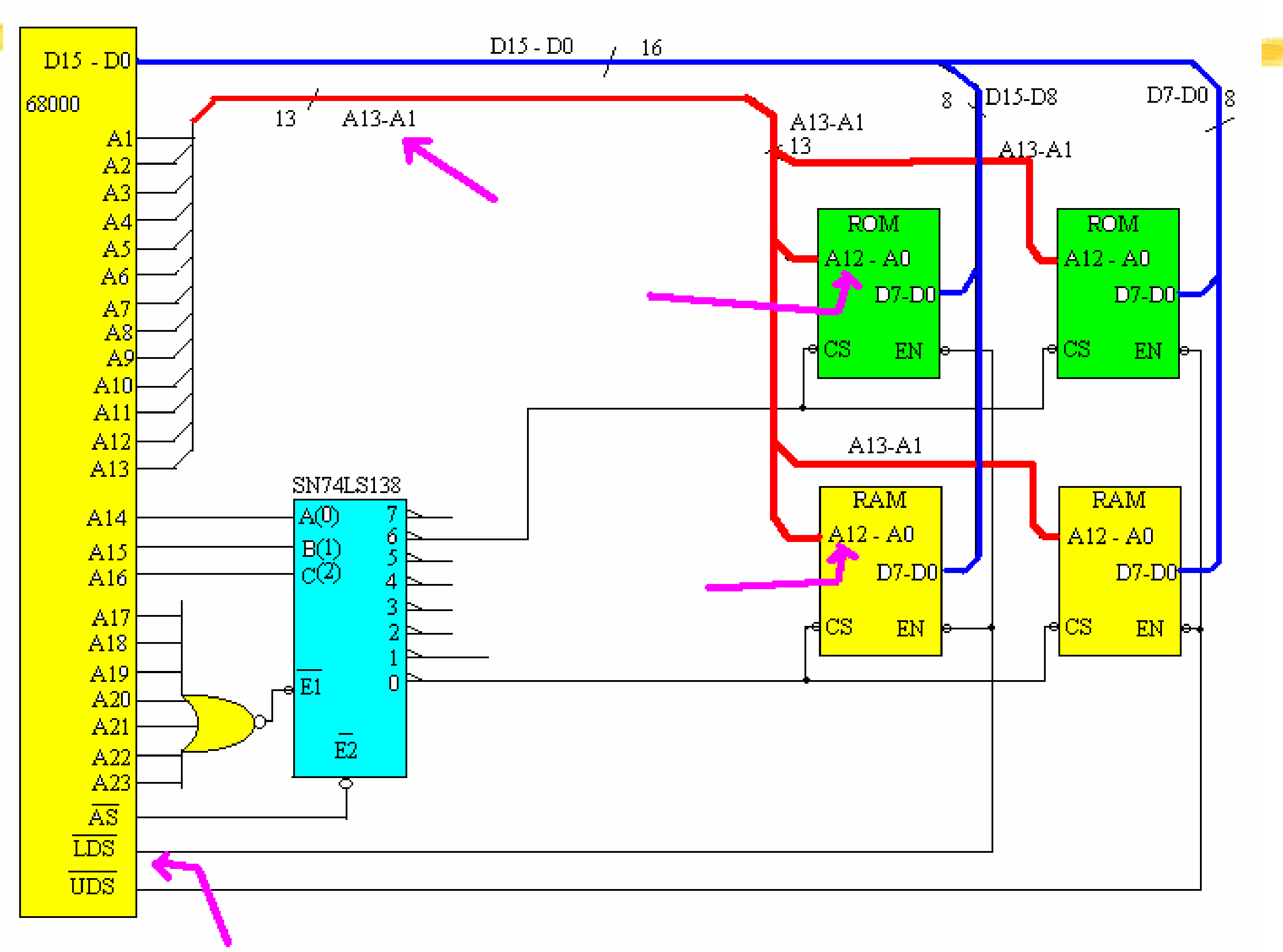


Memory Decoding Example

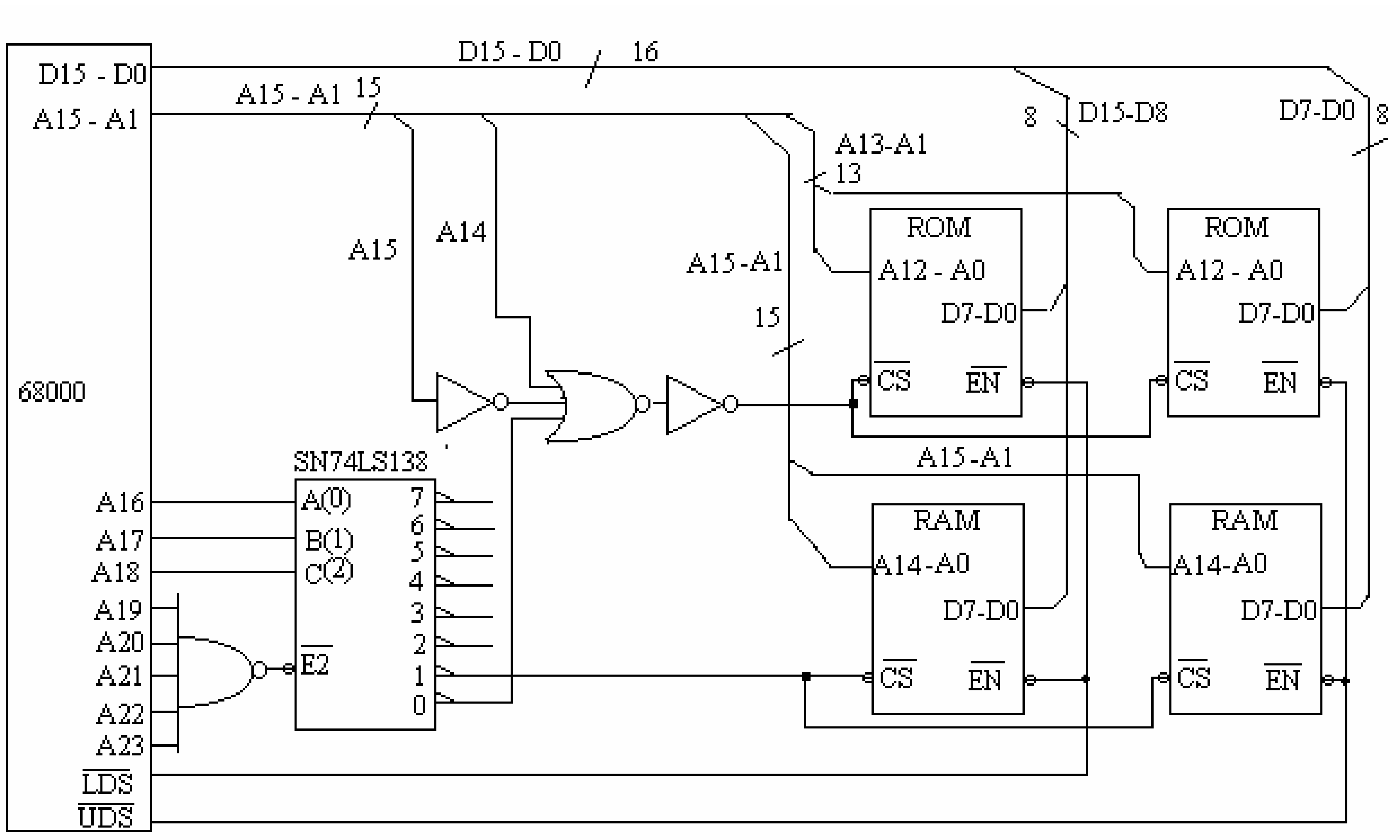
- Q: 16K Word ROM with starting address at $300000.
- A: 32KB → 15lines
  - $300000 - $307FFF

Memory Decoding with Byte/Word Access

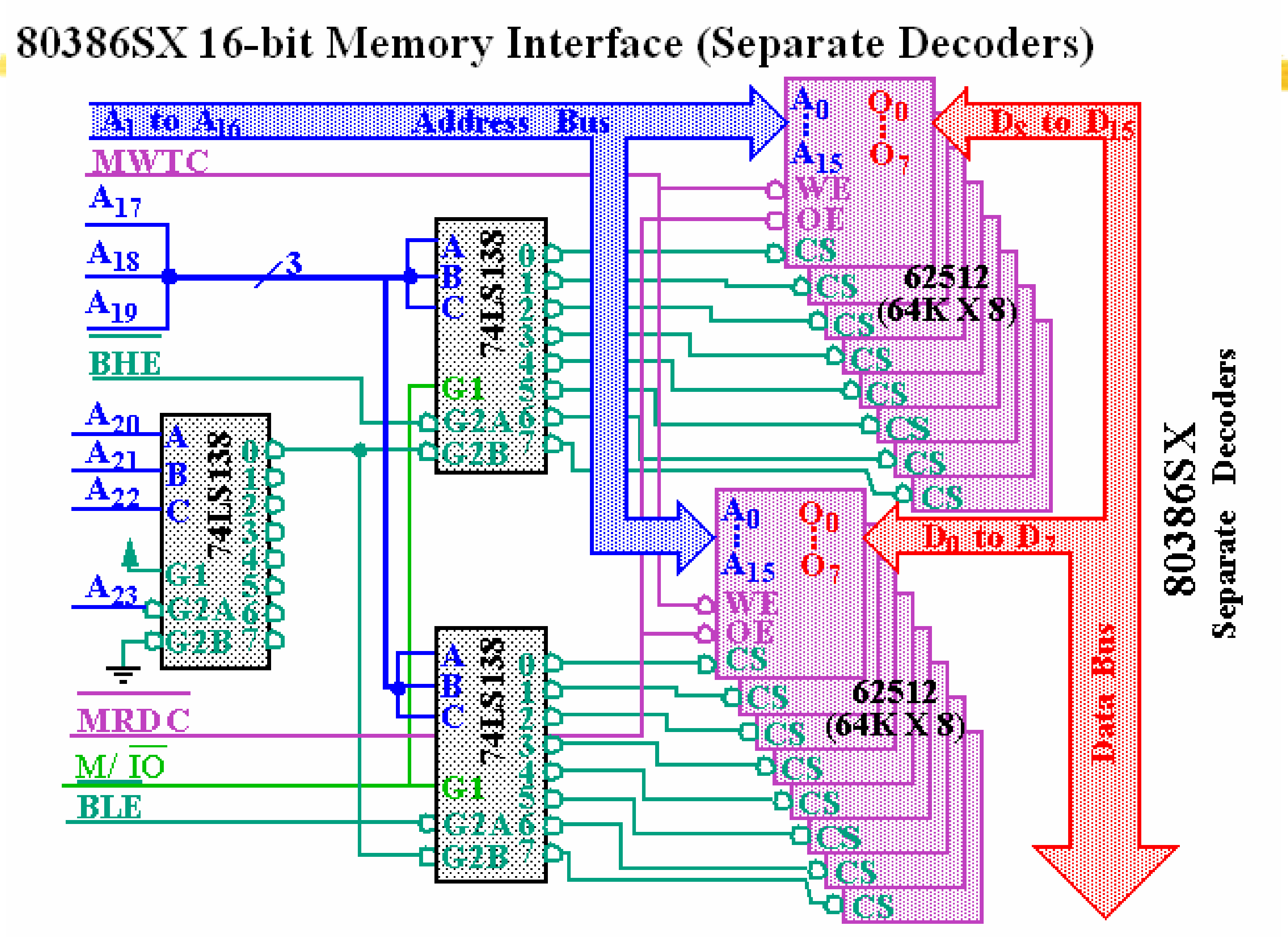
- Size of ROM
- Size of RAM
- Memory Map



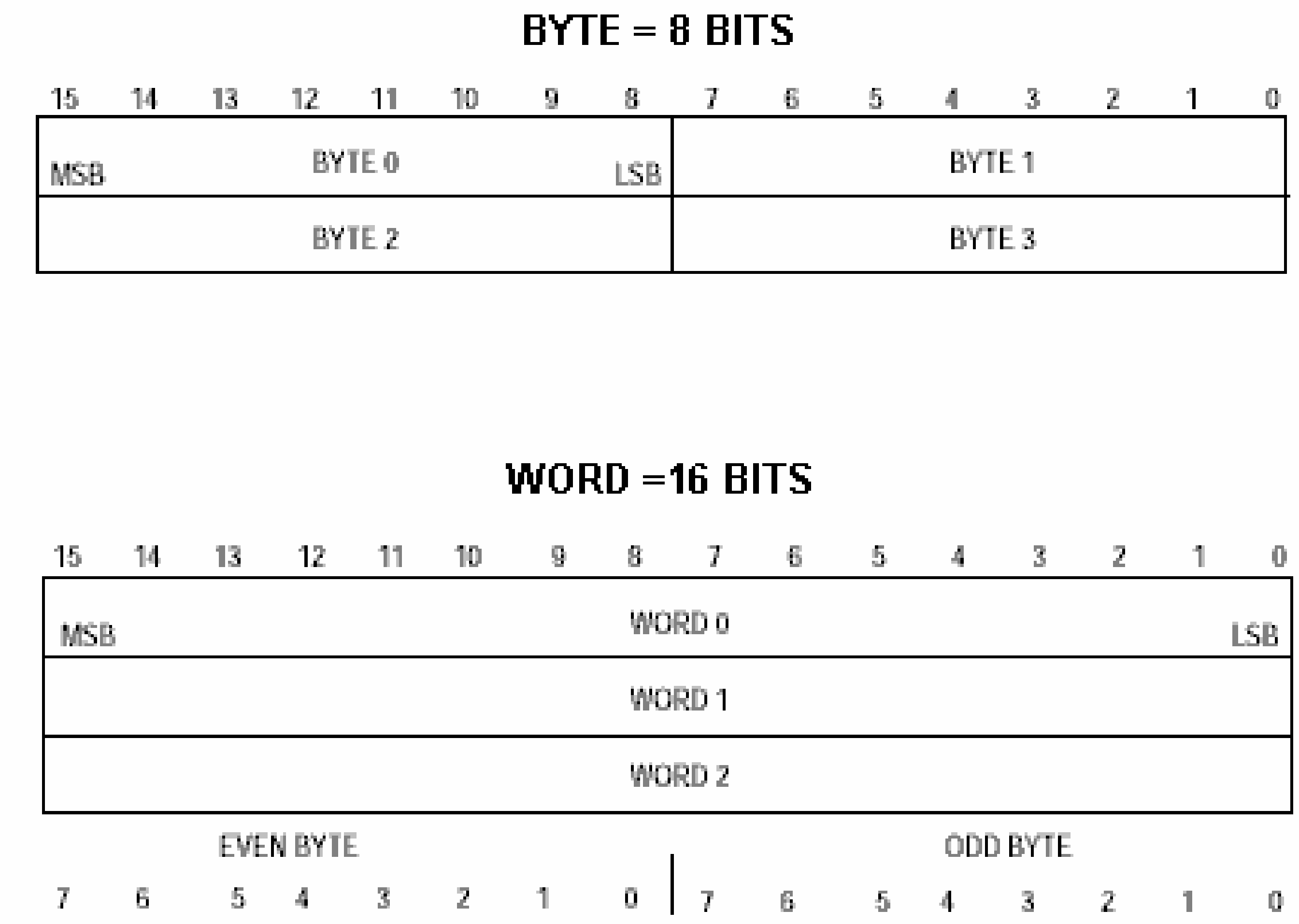
Can You Draw a Memory Map of this?



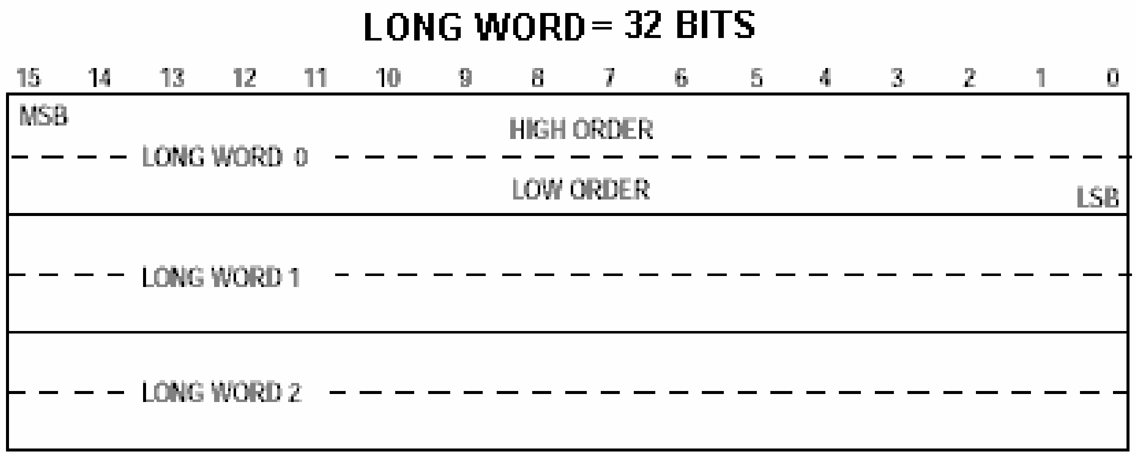
How about Intel 80386 case?

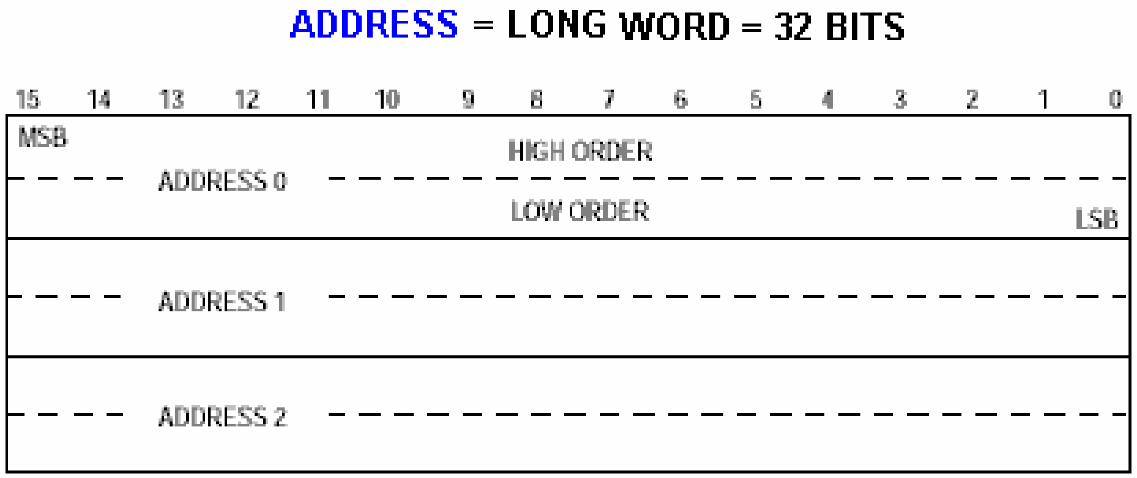


Data Organization in Memory



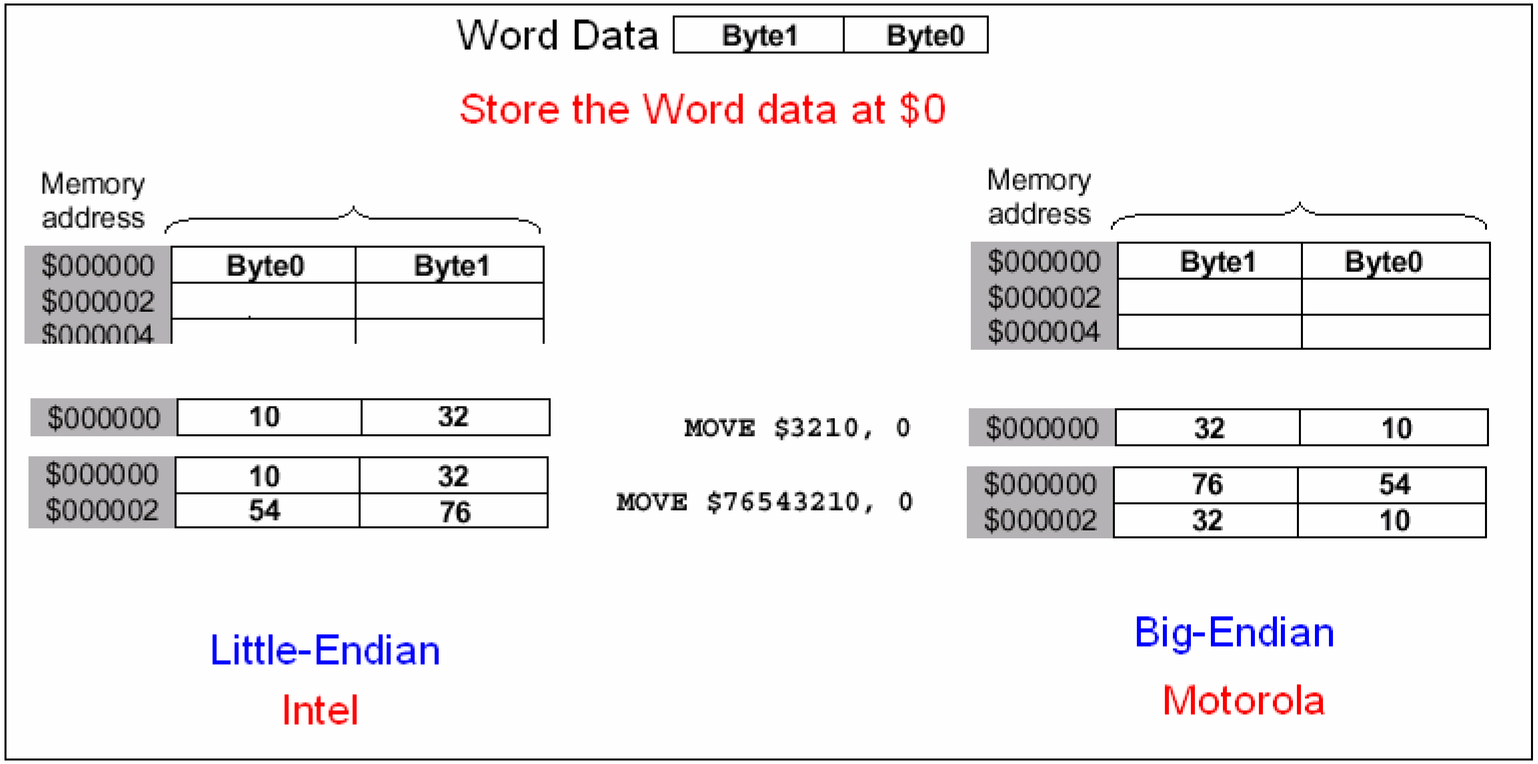
Data/Address Organization in Memory





Big-Endian

- Words are stored with the lower 8- bits in the higher of the two storage locations
- As opposed to little- endian (lower-order byte stored in the lowest addr) processors, like the Intel 80x86 family


Word Data
Byte1
Byte0
Store the Word data at $0
Memory address
$000000 Byte0 Byte1
$000002
$000004
Memory address
$000000 Byte1 Byte0
$000002
$000004
$000000 10 32
$000000 10 32
$000002 54 76
MOVE $3210, 0
MOVE $76543210, 0
$000000 32 10
$000000 76 54
$000002 32 10
Little-Endian
Intel
Big-Endian
Motorola