EECE416 Microcomputer Fundamentals

68000 Processor

1. Chip Signal Description

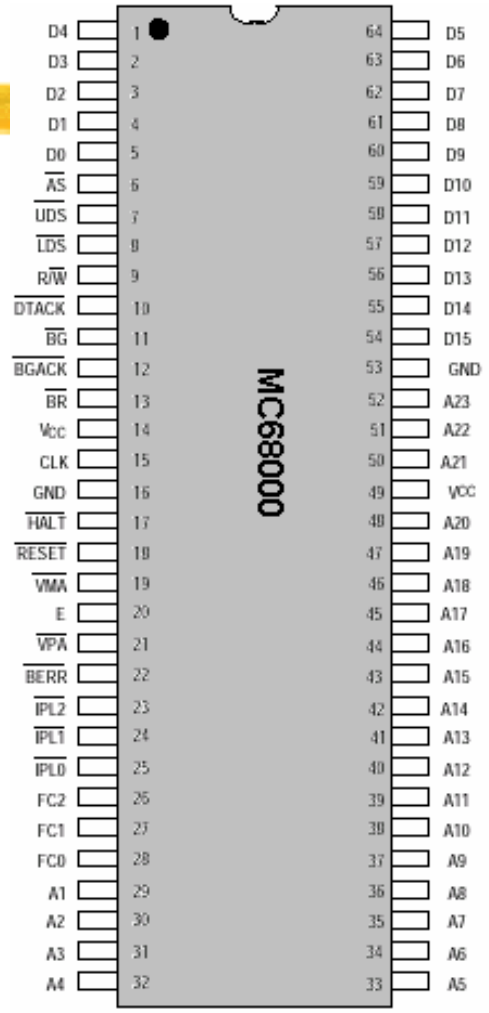
2. Instruction and Programming

Dr. Charles Kim

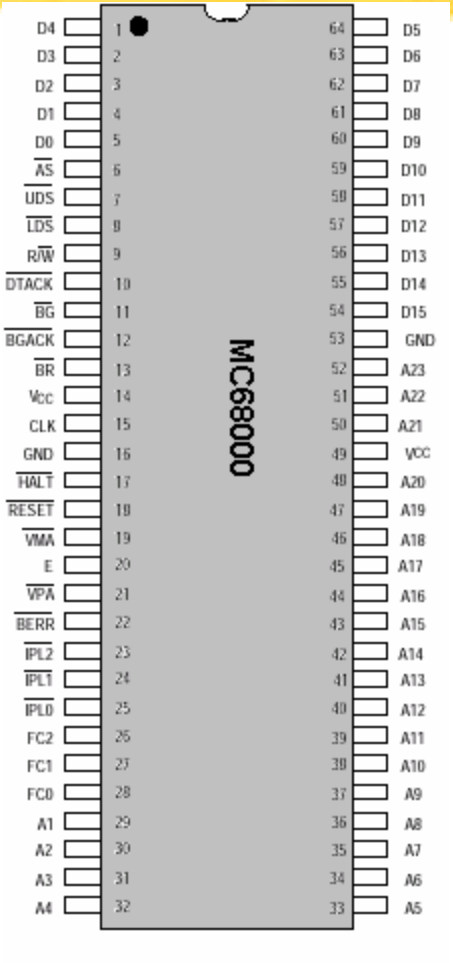
Howard University

68000 Microprocessor

- 64 pins
- 32- bit Data and Address Registers
- 16- bit Data Bus
- 24- bit Address Bus (16MB)
- 14 Addressing Modes
- Memory- Mapped Input/ Output
- Program Counter(PC)
- 5 Main Data Types- *L, W, B, b, BCD*
- 7 interrupt levels
- Clock speeds: 4MHz to 12.5MHz
- Synchronous and asynchronous data transfers

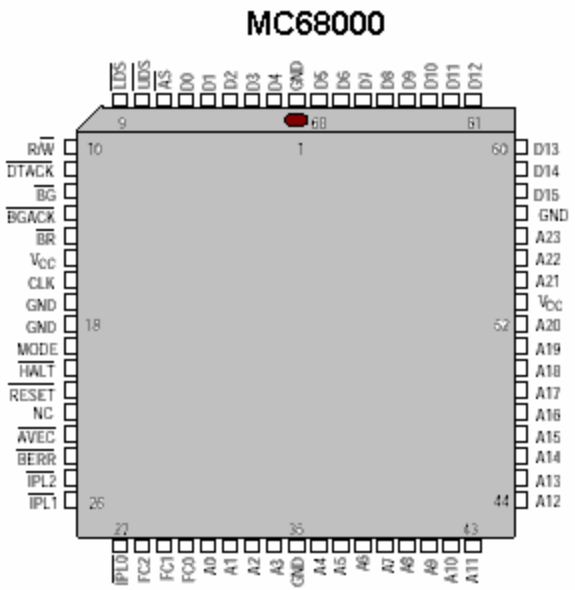


PIN and PACKAGE



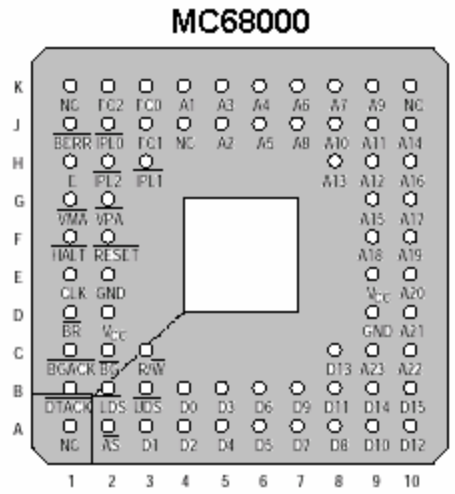
DIP

PLCC



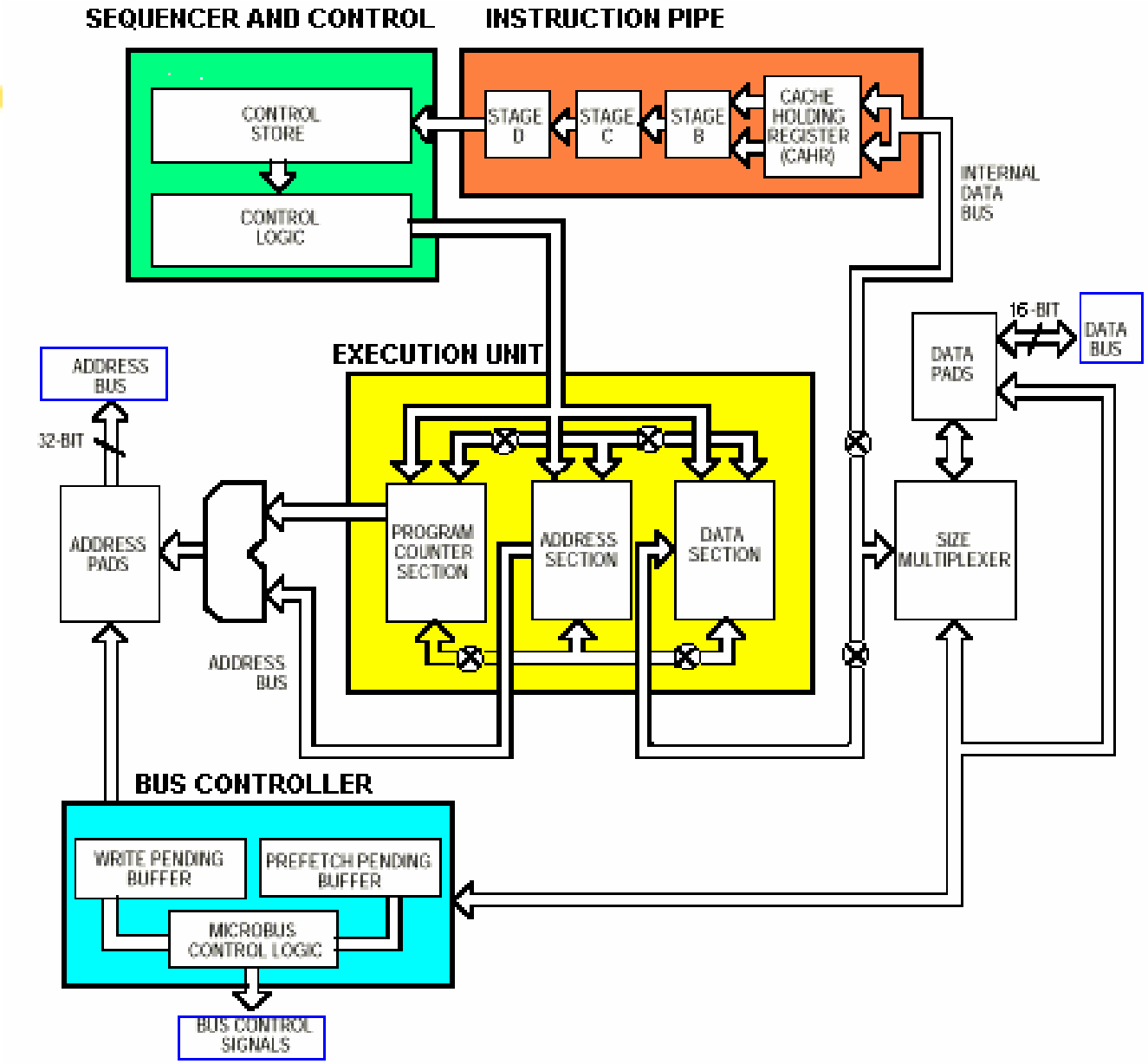
* Top View

PLCC Socket

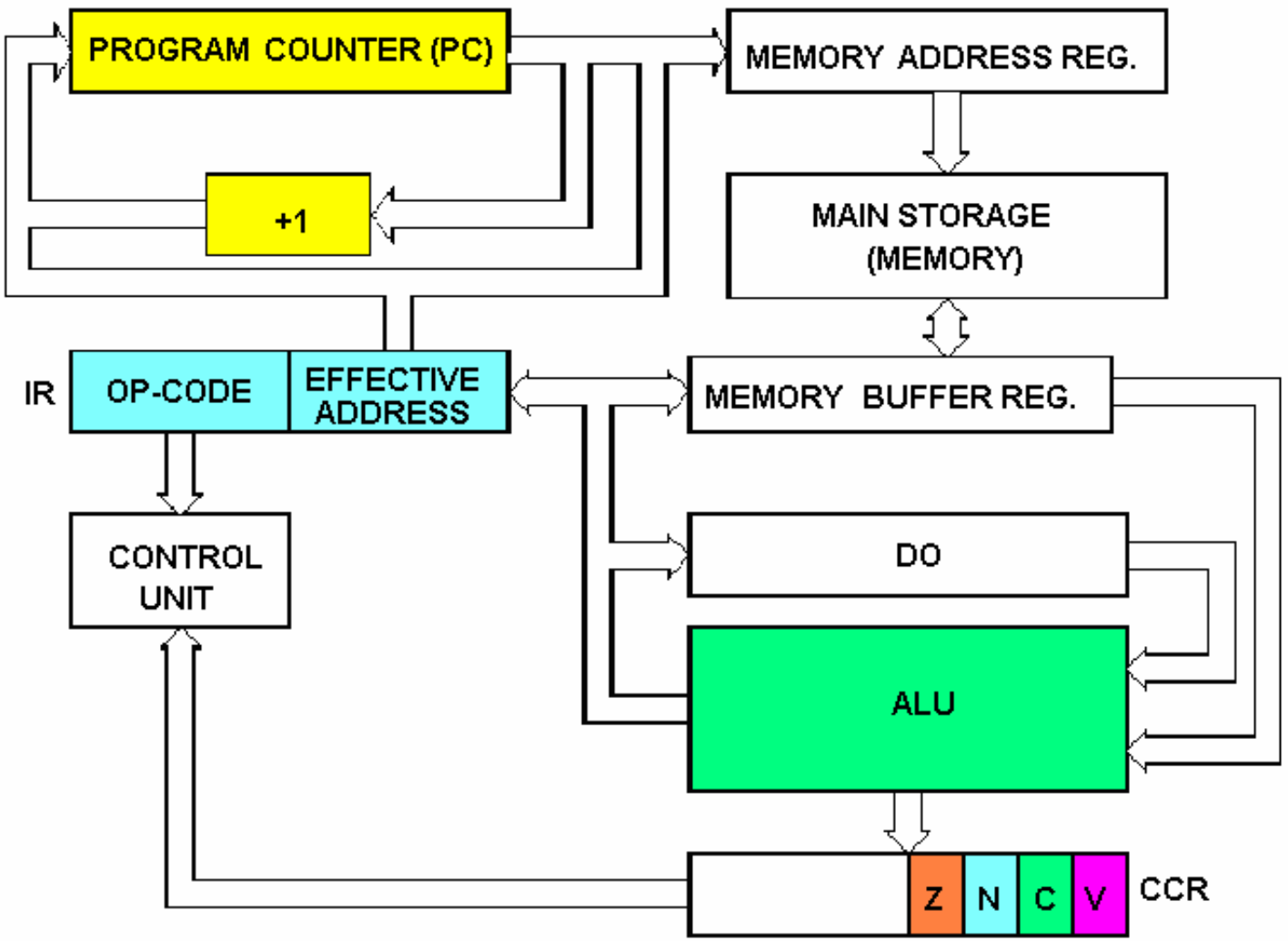


* Bottom View

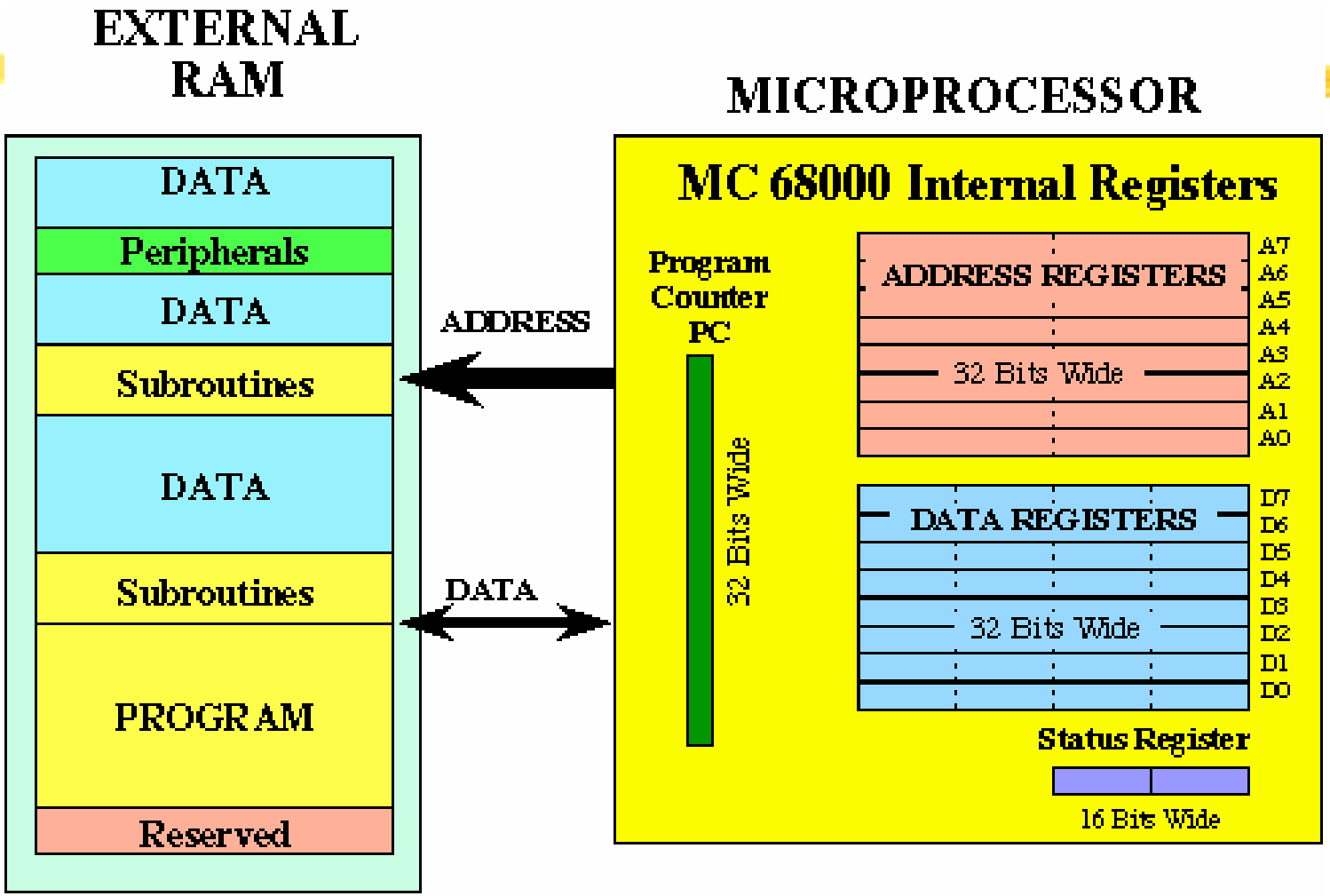
BLOCK Diagram



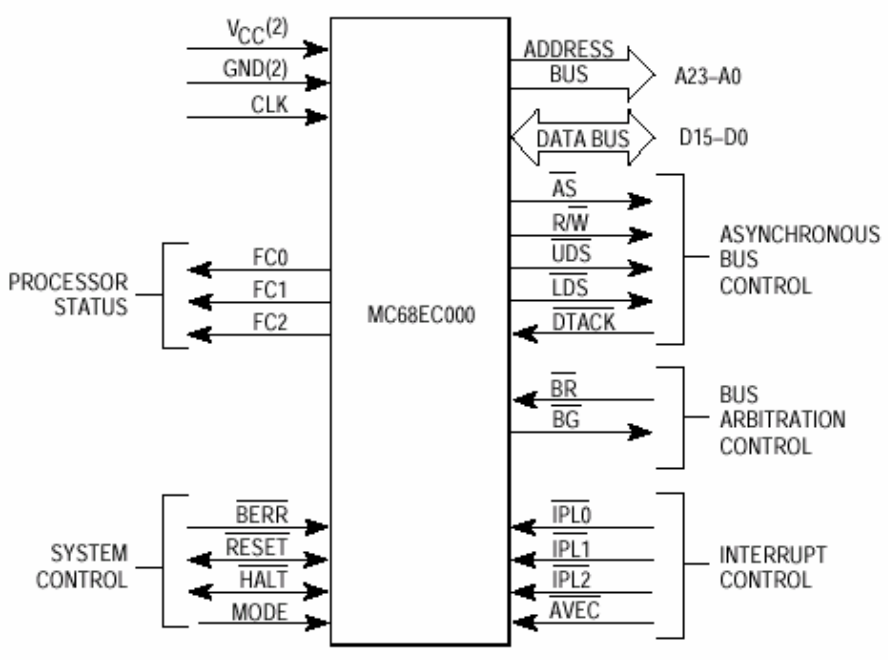
Core Structure

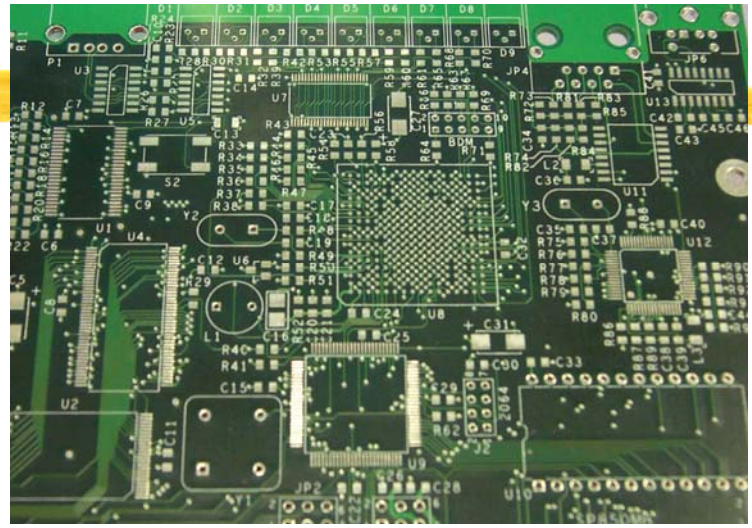


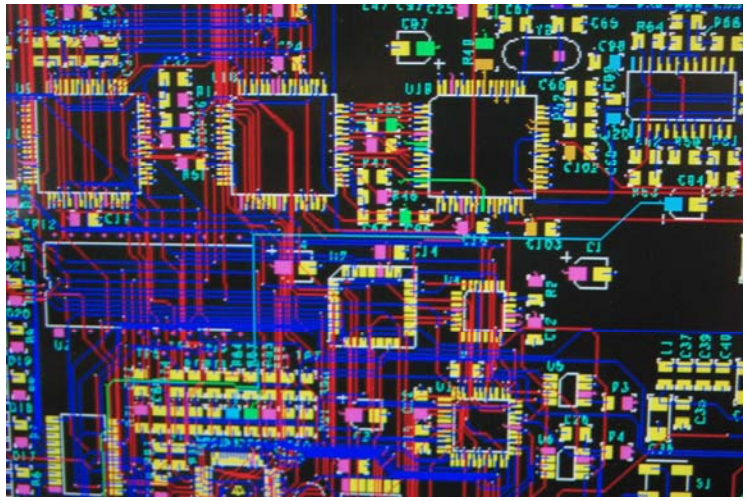
Internal Structure - Registers



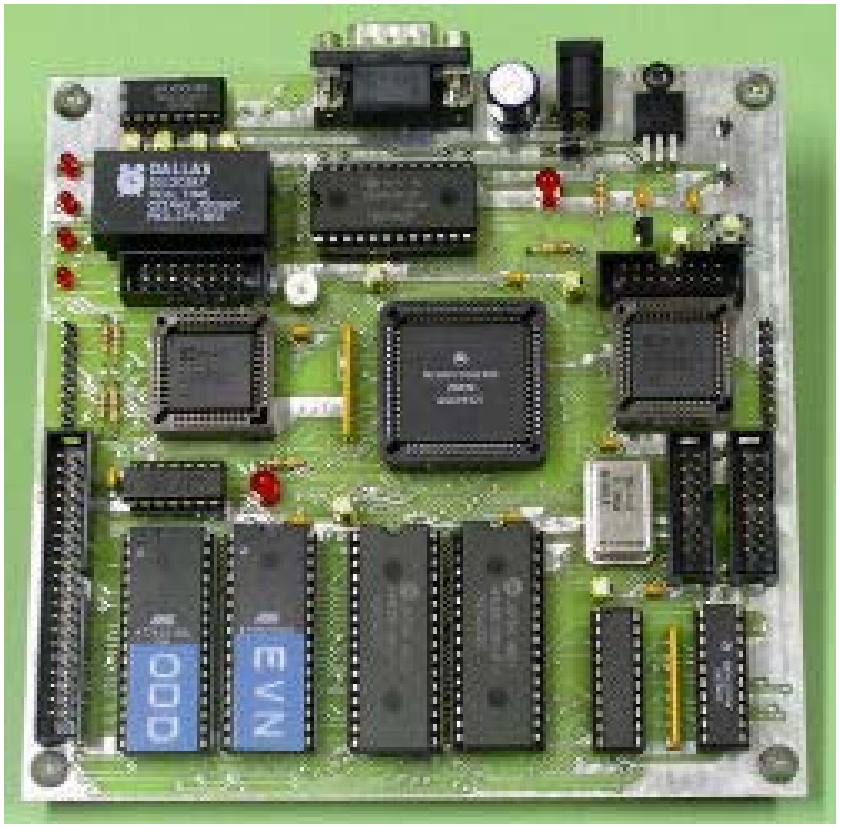
Connecting with Peripherals

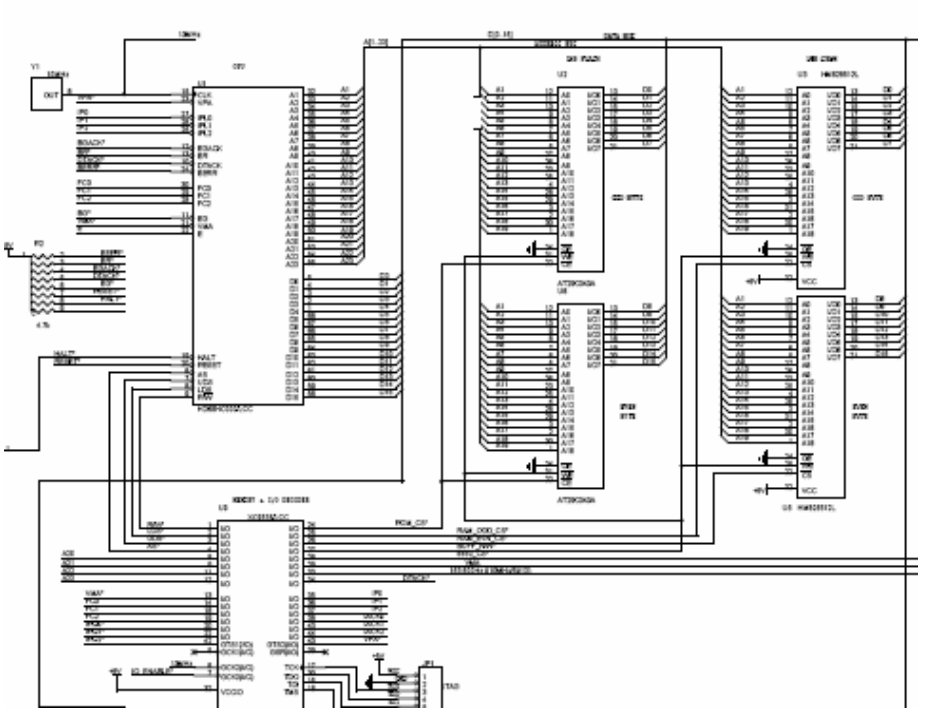




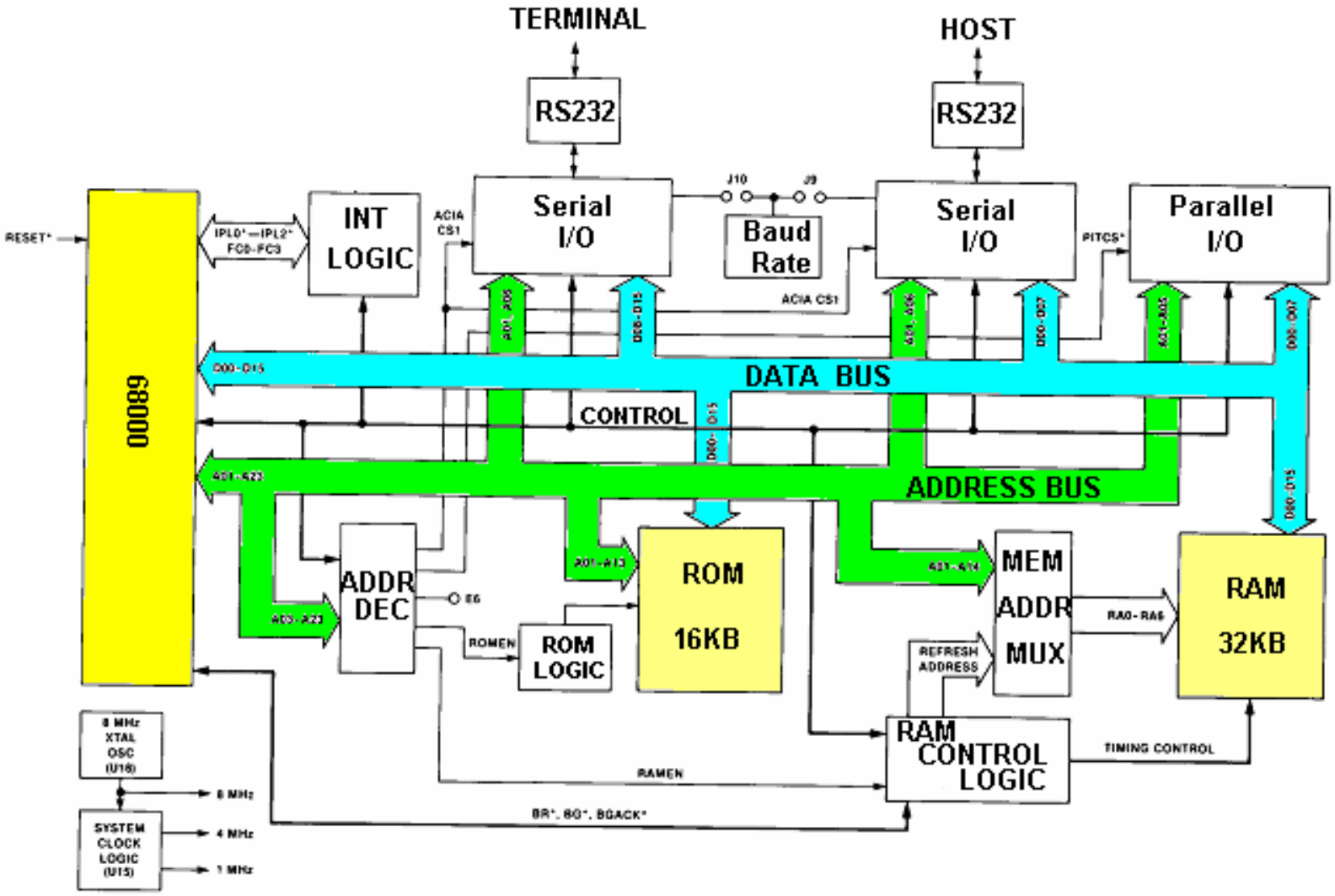


68000 Single Board Computer (SBC)



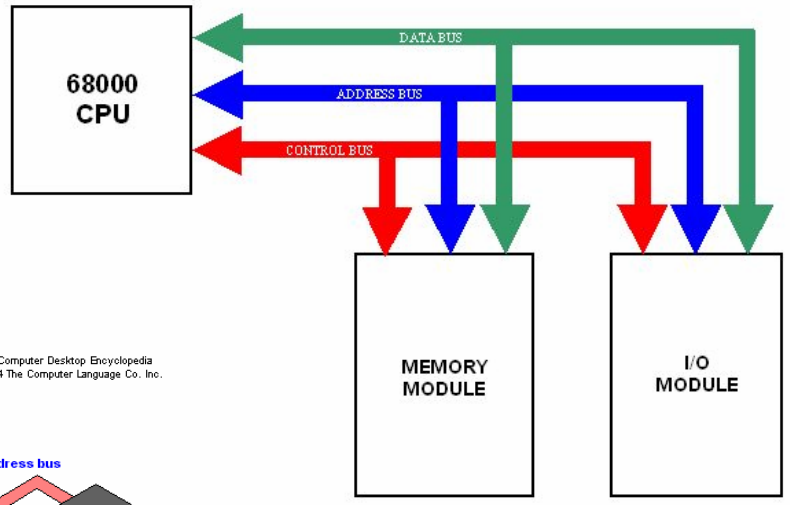


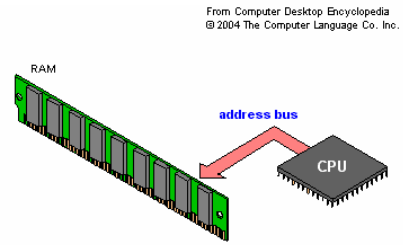
68000 Single Board Computer- block diagram



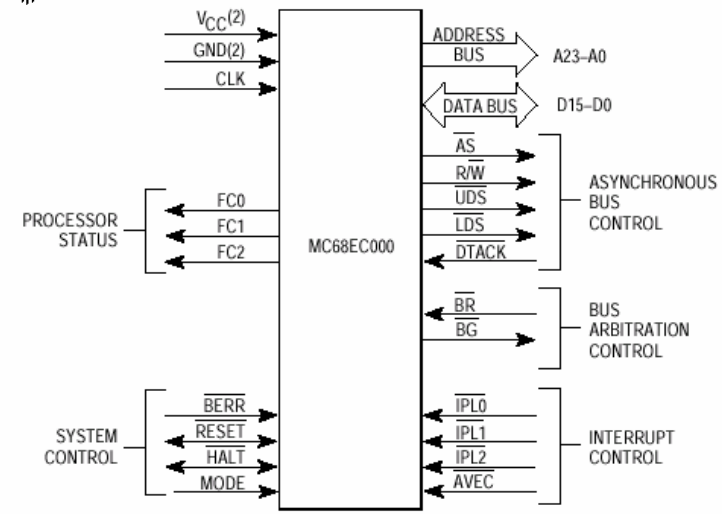
SIGNAL DESCIRPTION

- **1. ADDRESS BUS (A23–A1)**
  - **23-bit, unidirectional, three state bus**
  - capable of addressing 16 Mbytes of data.





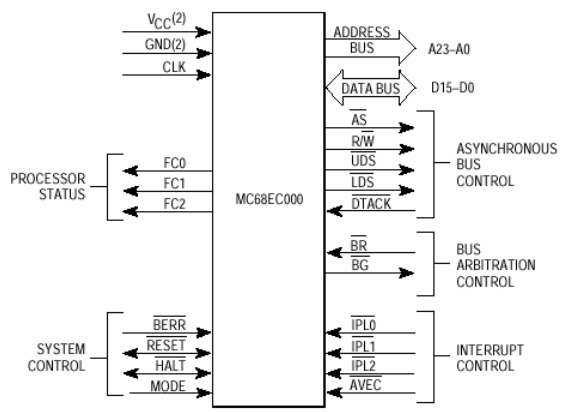
- **2. DATA BUS (D15–D0)**
  - **bidirectional, three-state bus**
  - general-purpose data path of 16 bits wide
  - transfer data of either word or byte length.

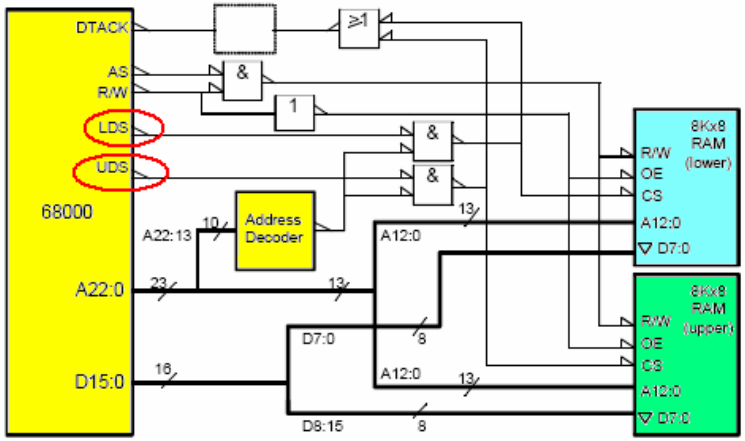


Signal Description

3. ASYNCHRONOUS BUS CONTROL

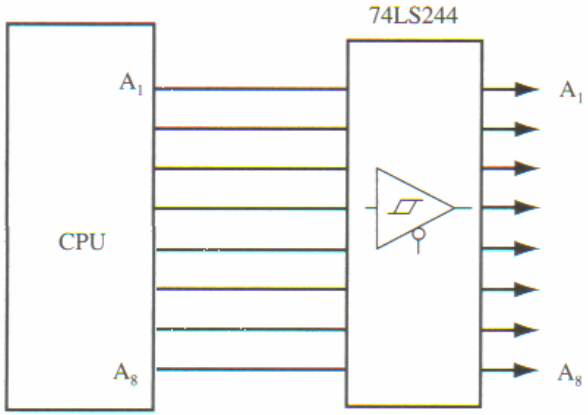
- **Address Strobe (~AS).**
  - This three-state signal indicates that the information on the address bus is a valid address.
- **Read/Write (R/~W).**
  - This three-state signal defines the data bus transfer as a read or write cycle.
- **Upper And Lower Data Strobes (~UDS, ~LDS).**
- **Data Transfer Acknowledge (~DTACK).**
  - **This input signal indicates the completion of the data transfer.**

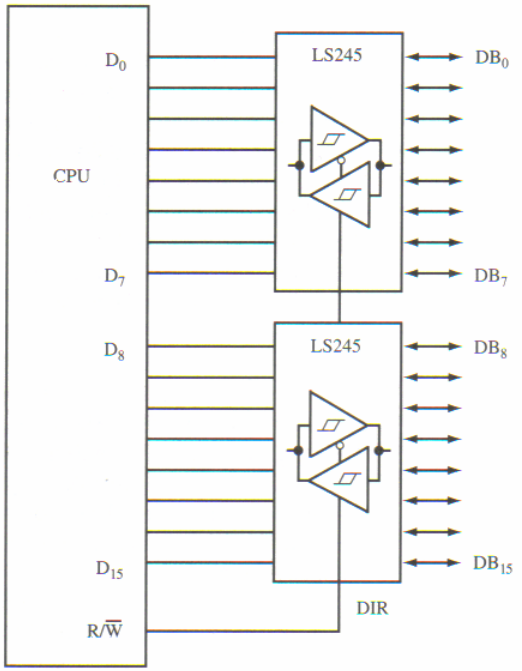




Memory Decoding

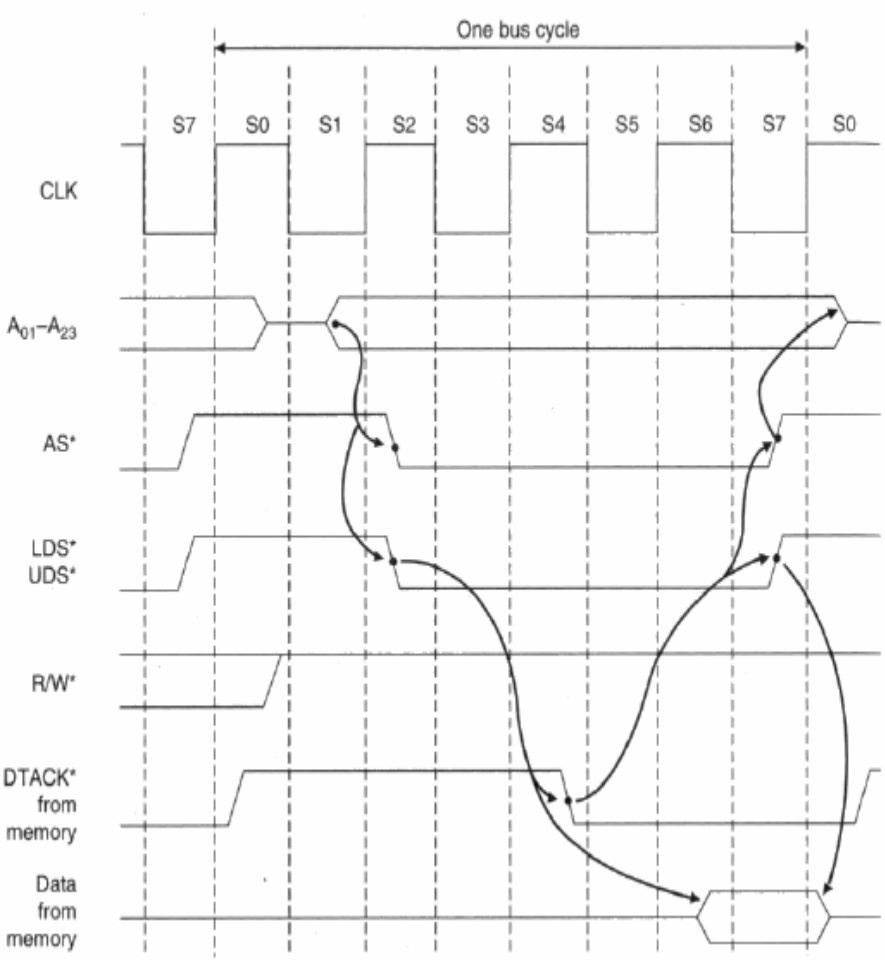
- Memory Bus
  - Control
  - Data (Bi-directional)
  - Address (Unidirectional)
- Address Bus Buffering
  - Fan Out
  - 74LS244 Octal line driver/receiver
- Data Bus Buffering
  - R/W for Direction
  - Fan Out
  - 74LS245 Octal Bus Transceiver

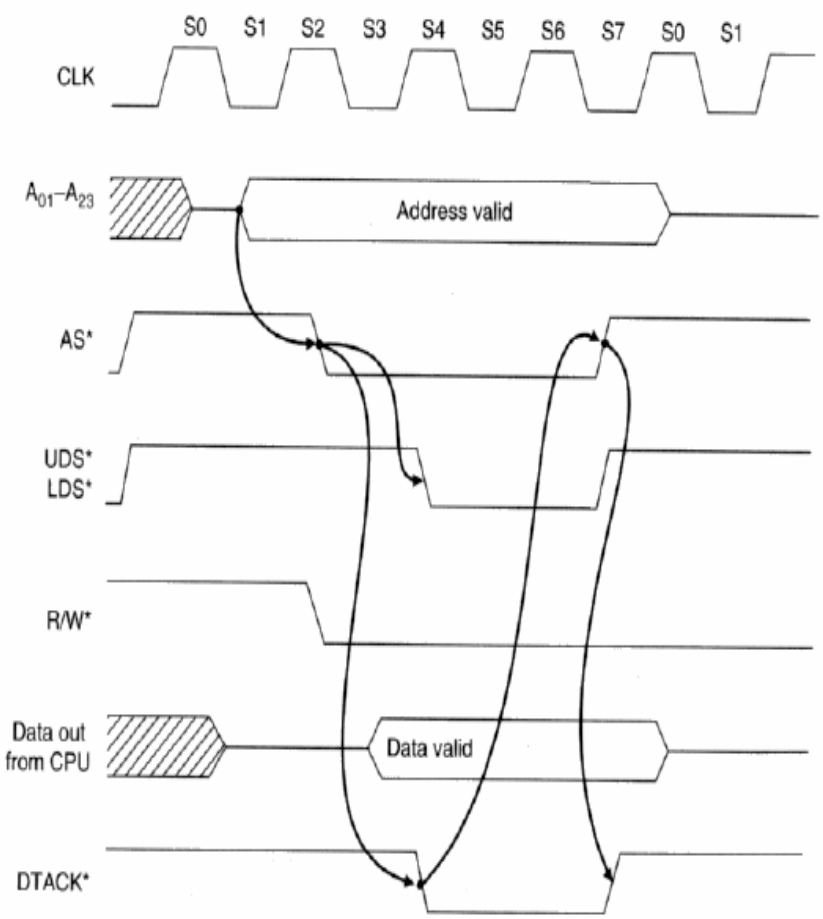




Memory Accessing

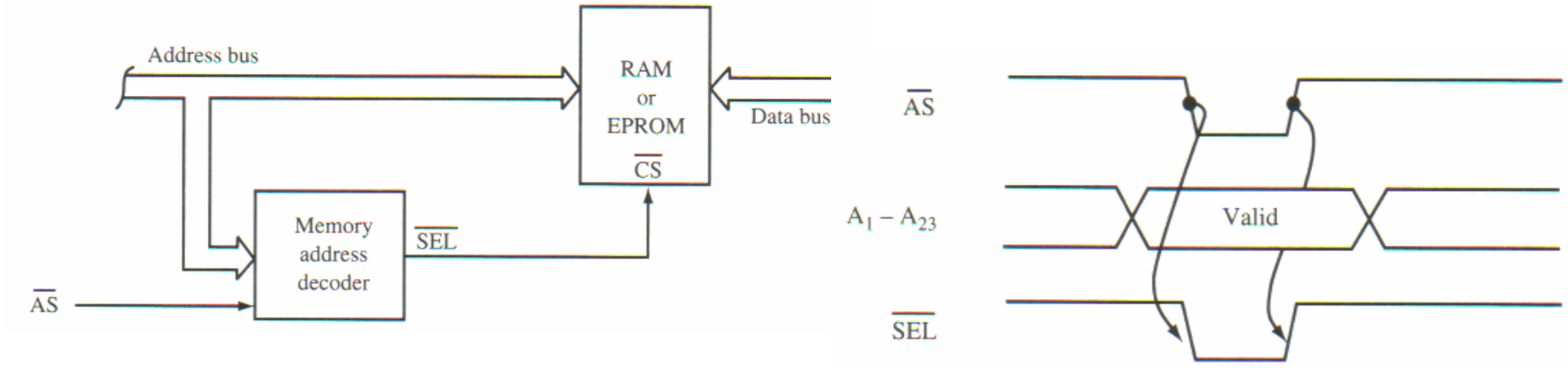
- READ AND WRITE CYCLE





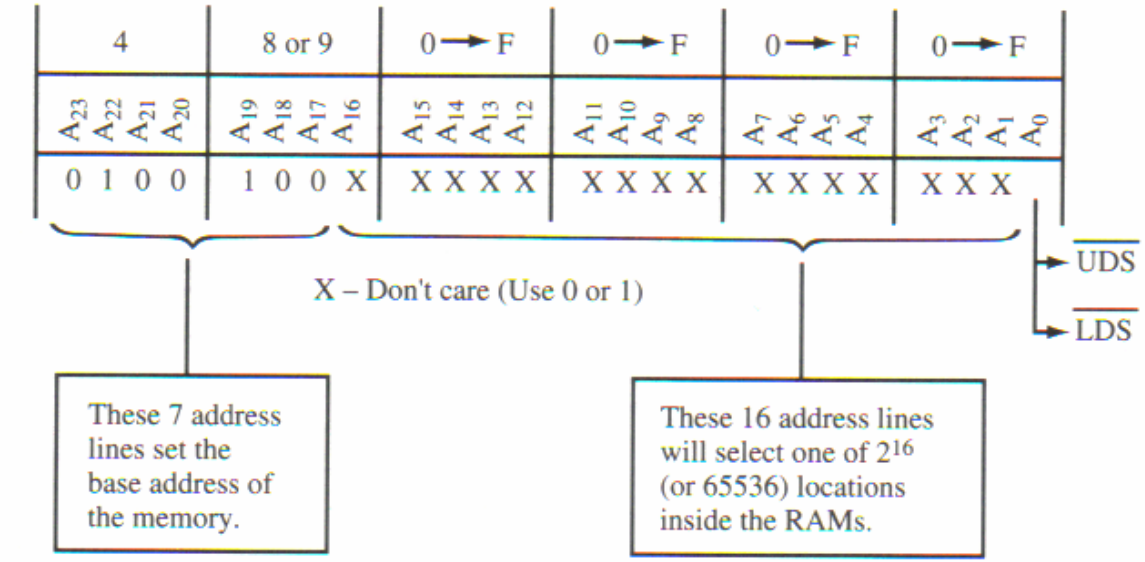
Memory Address Decoding

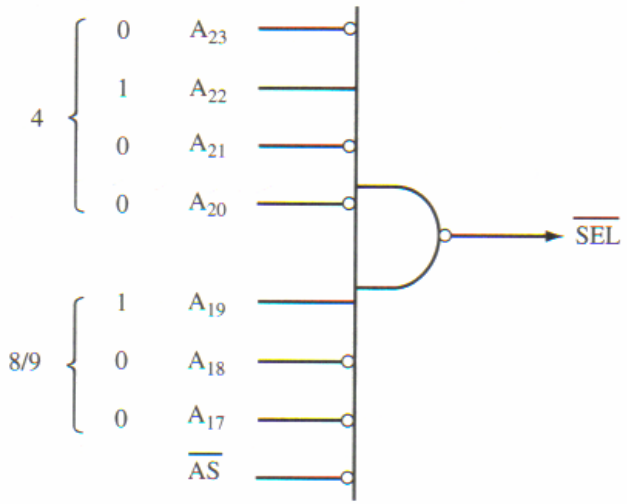
- How Much Memory?
- How Many Address Lines?
- 1K → 10 lines
- 32K → 15 lines



Memory Decoding

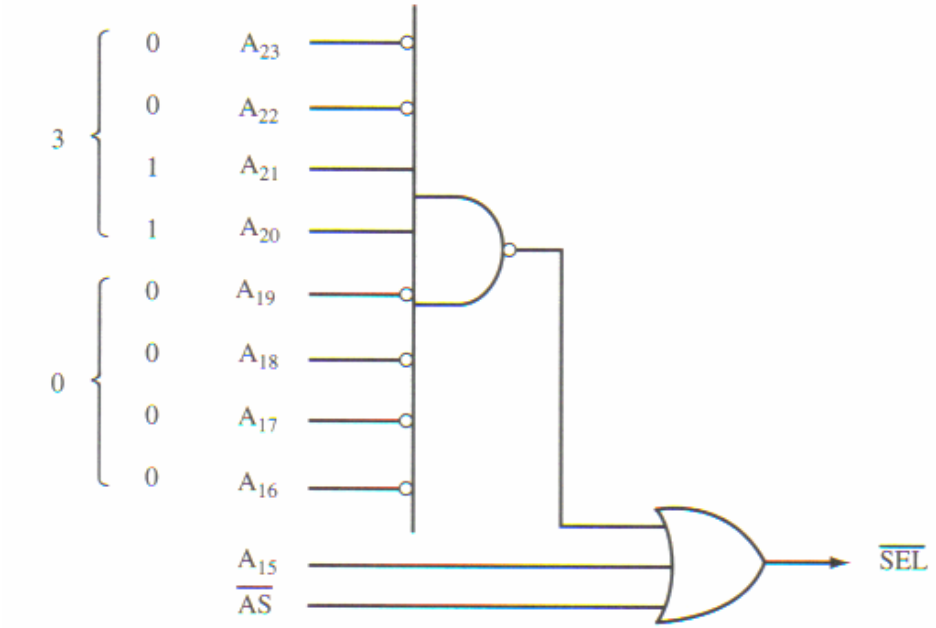
- Q: 64K Word (or 128 KB) of RAM, with it's starting address at $480000
- A: 128KB → 17 lines
  - Range: $480000 - $49FFFF
  - UDS and LDS for A_0 line.





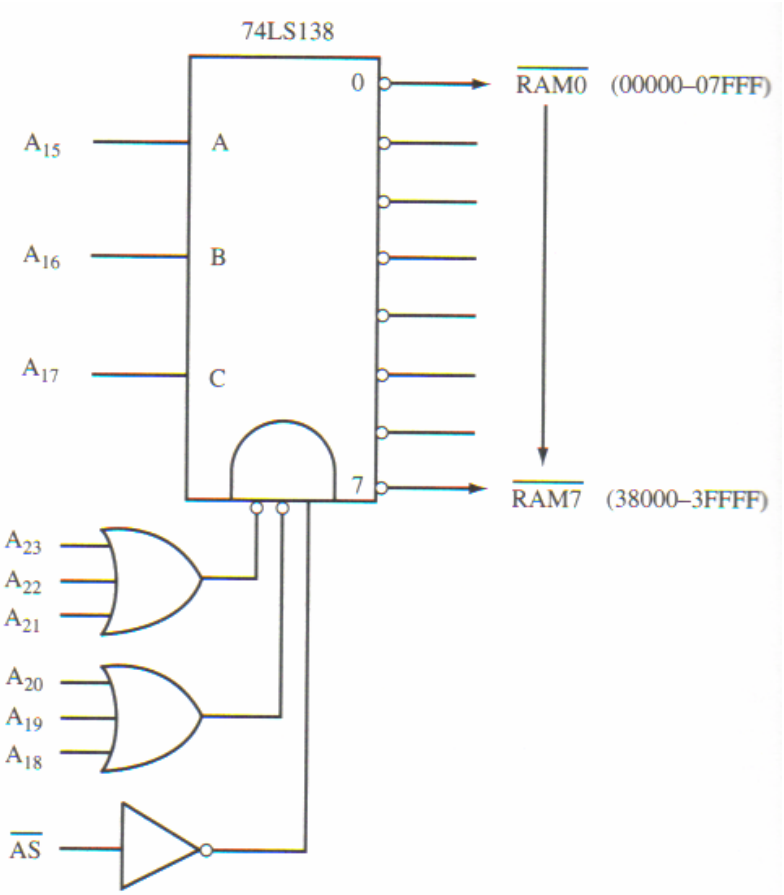
Memory Decoding Example

- Q: 16K Word EEPROM with starting address at $300000.
- A: 32KB → 15lines
  - $300000 - $307FFF



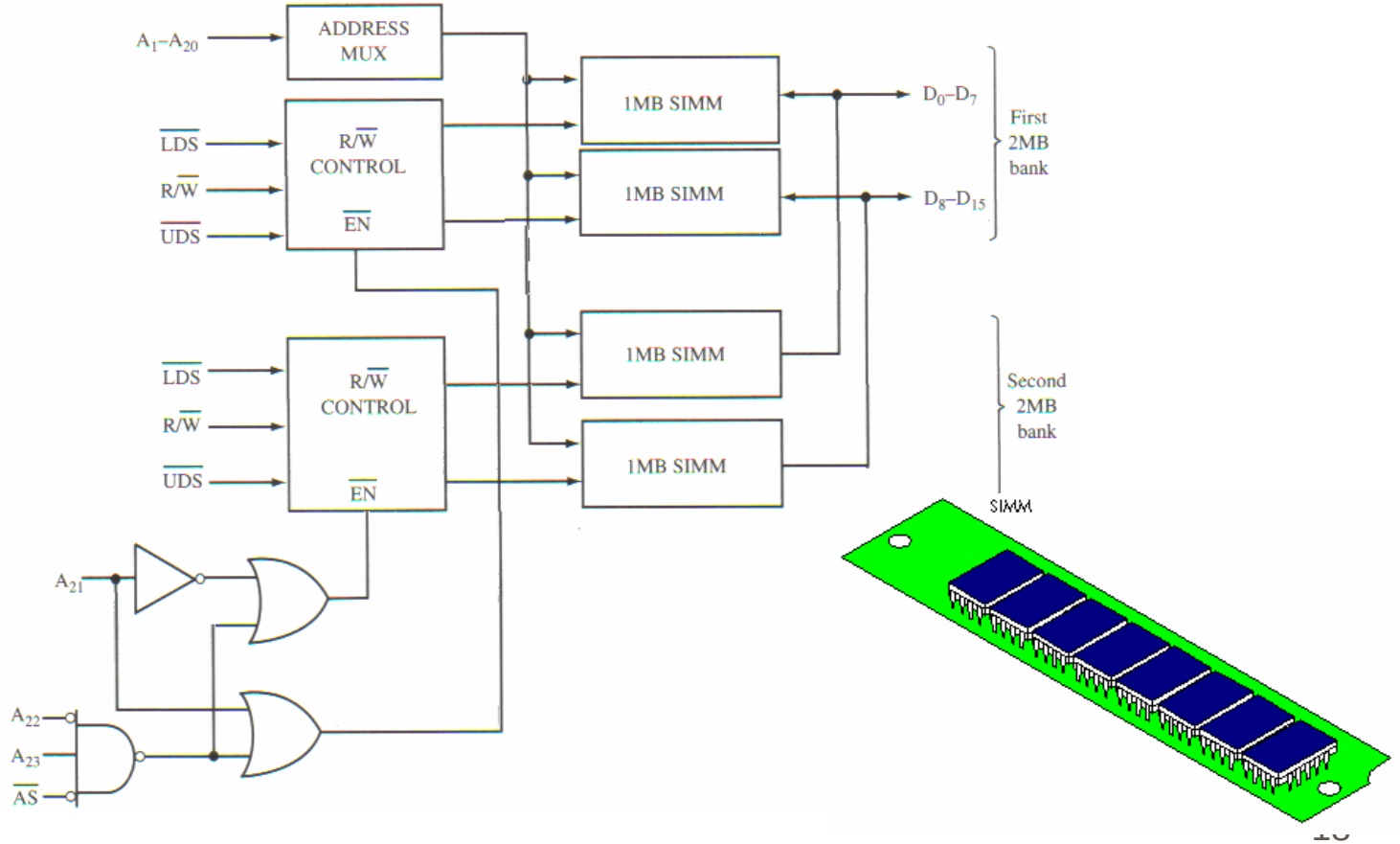
Memory Decoding - multibank

- Q: 256KB RAM composed of eight 32KB RAMs
- Address Range:
  - 00000 – 07FFF
  - 08000 – 0FFFF
  - 10000 – 17FFF
  - 18000 – 1FFFF
  - 20000 – 27FFF
  - 28000 – 2FFFF
  - 30000 – 37FFF
  - 38000 – 3FFFF

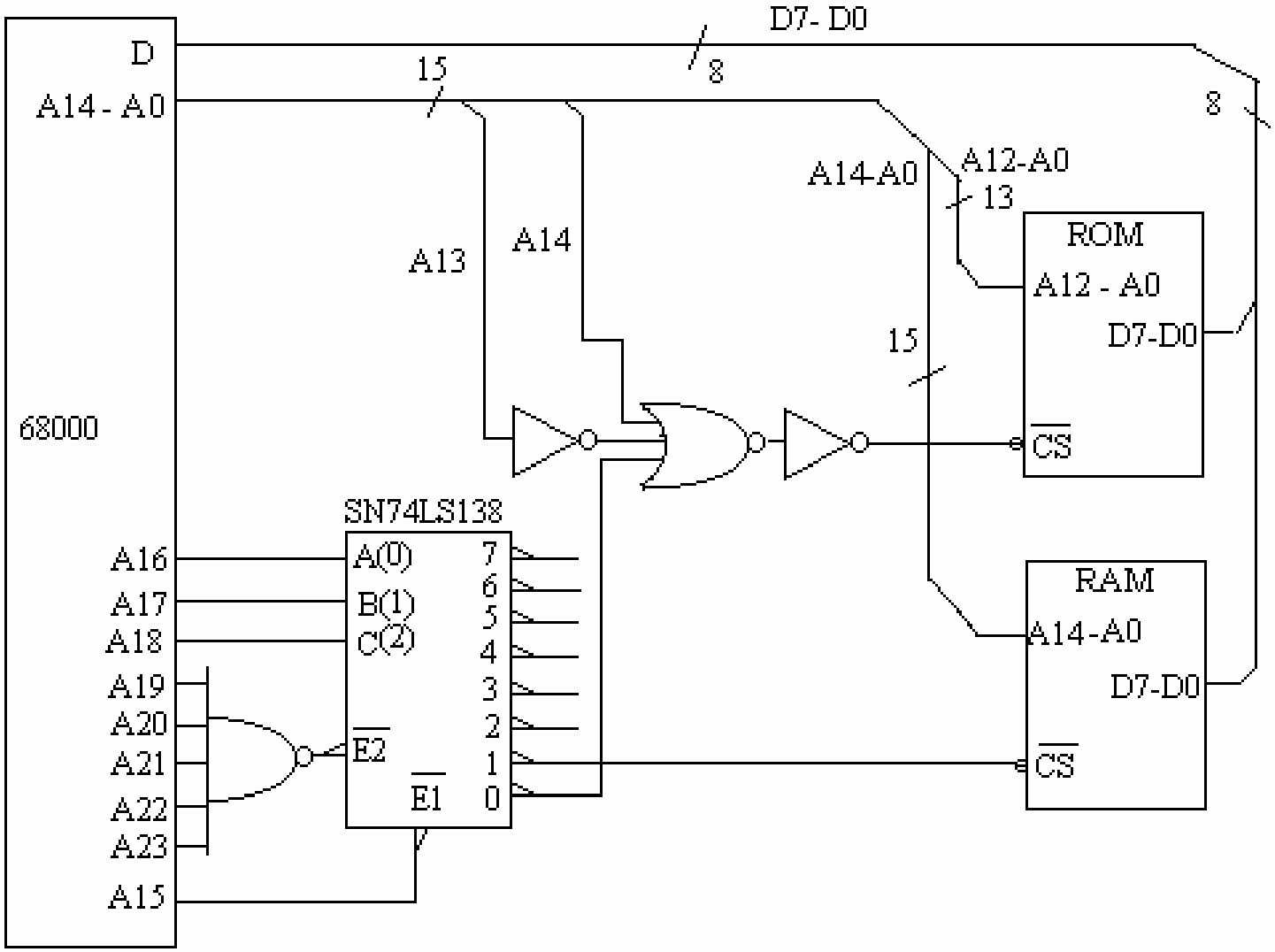


SIMM (*single in-line memory module*) Circuit of RAM

- 4MB Memory at the base address of 800000 using 1MB SIMMs

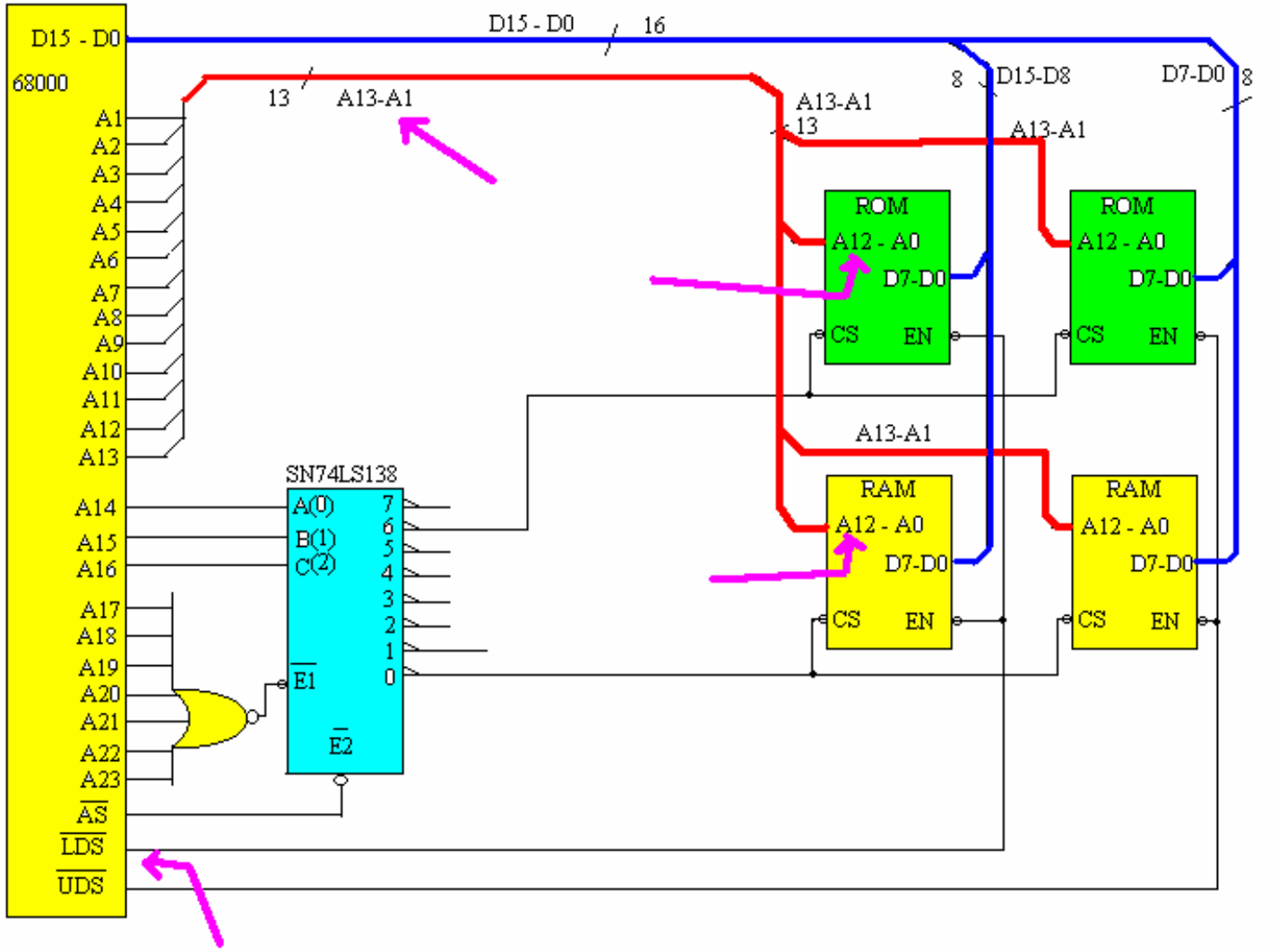


Memory Map for ROM and RAM

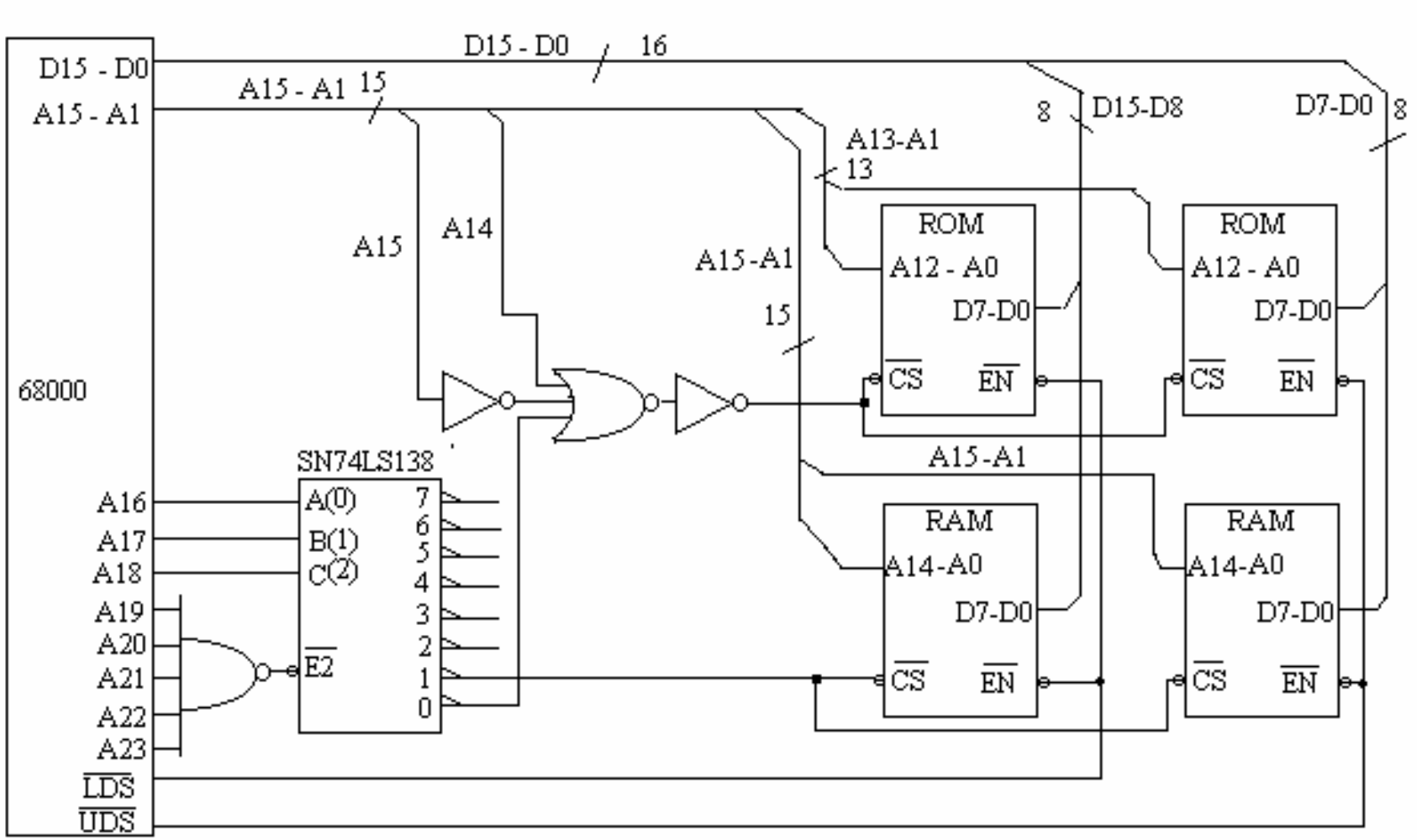


Memory Decoding with Byte/Word Access

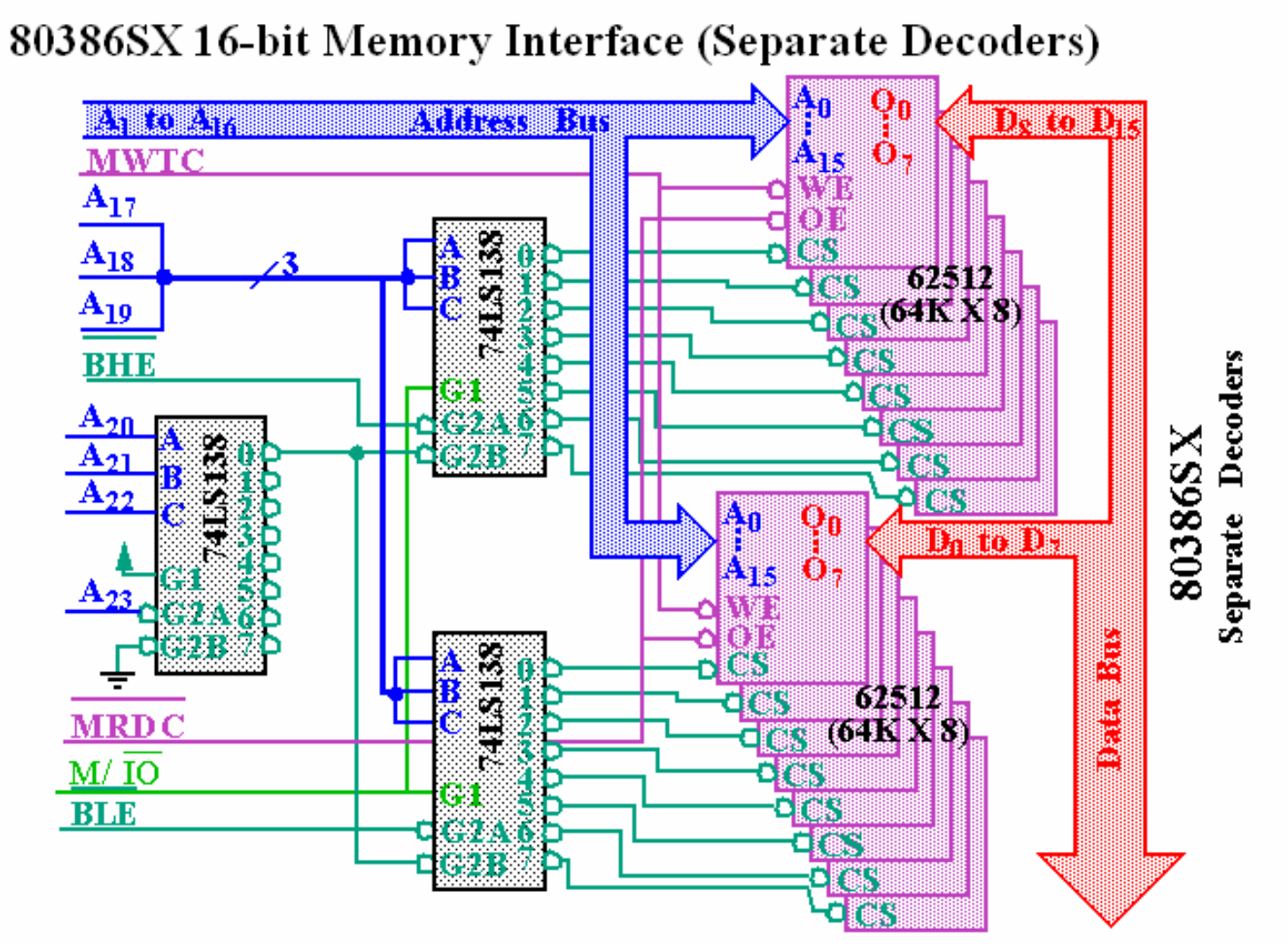
- Size of ROM
- Size of RAM
- Memory Map
- Byte/Word Access



Can You Draw a Memory Map of this?

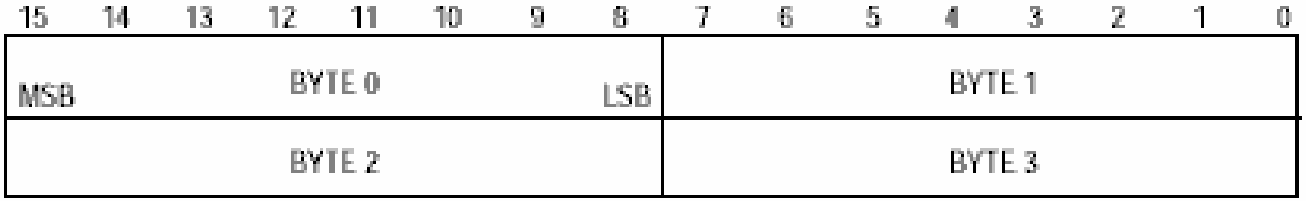


How about Intel 80386 case?

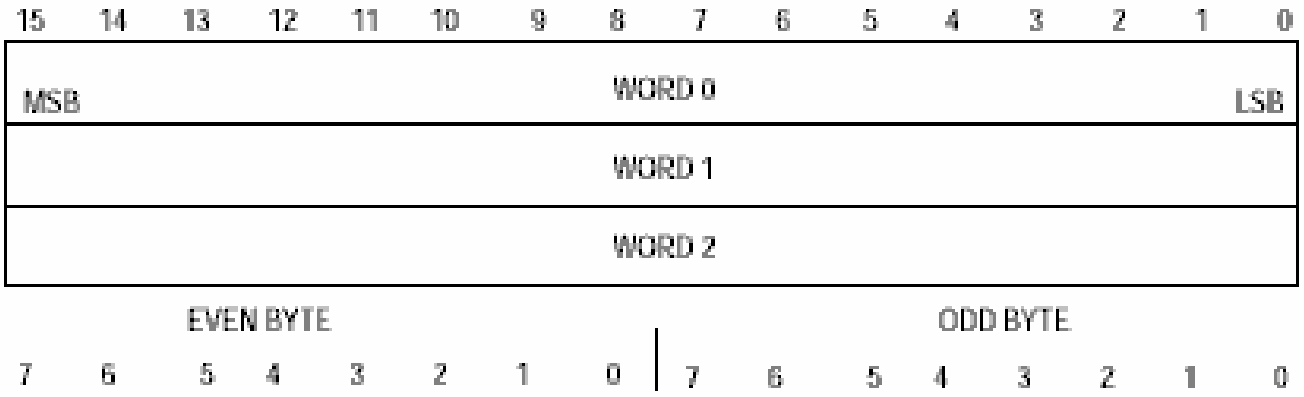


Data Organization in Memory

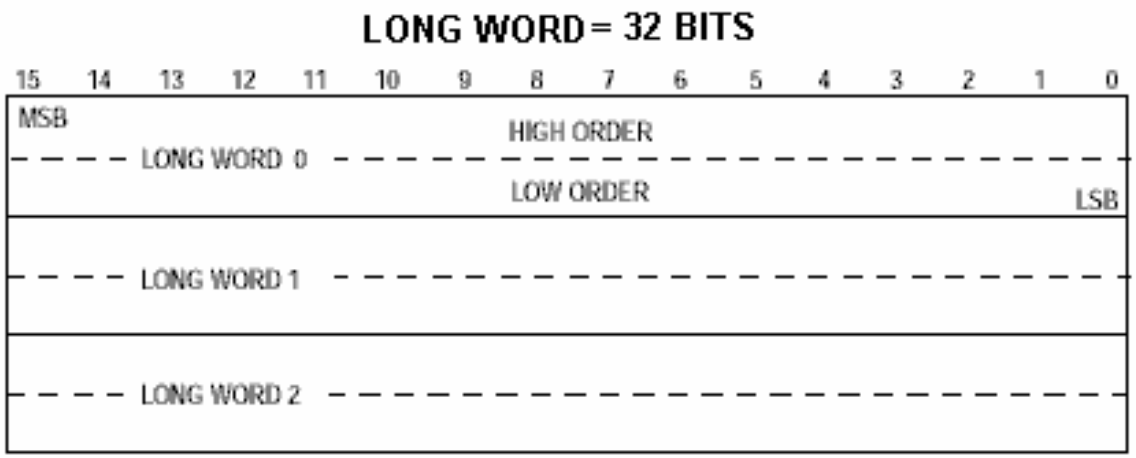
BYTE = 8 BITS

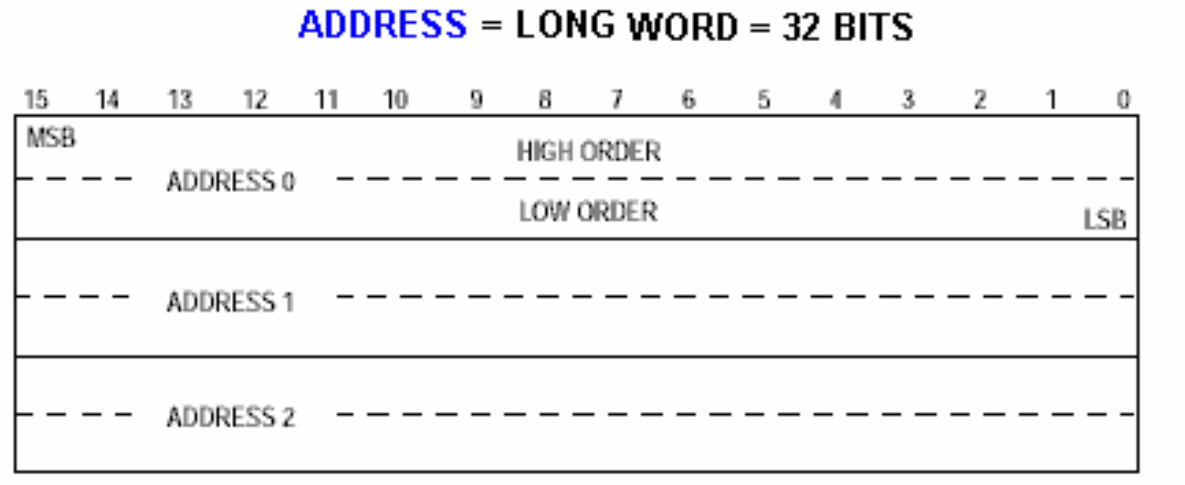


WORD =16 BITS



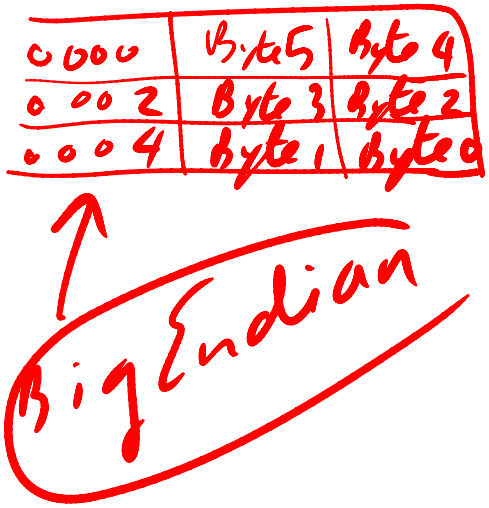
Data/Address Organization in Memory





Big-Endian

- Words are stored with the lower 8- bits in the higher of the two storage locations
- As opposed to little- endian (lower-order byte stored in the lowest addr) processors, like the Intel 80x86 family



Memory address

$000000	Byte0	Byte1
$000002	Byte2	Byte3
$000004	Byte4	Byte5

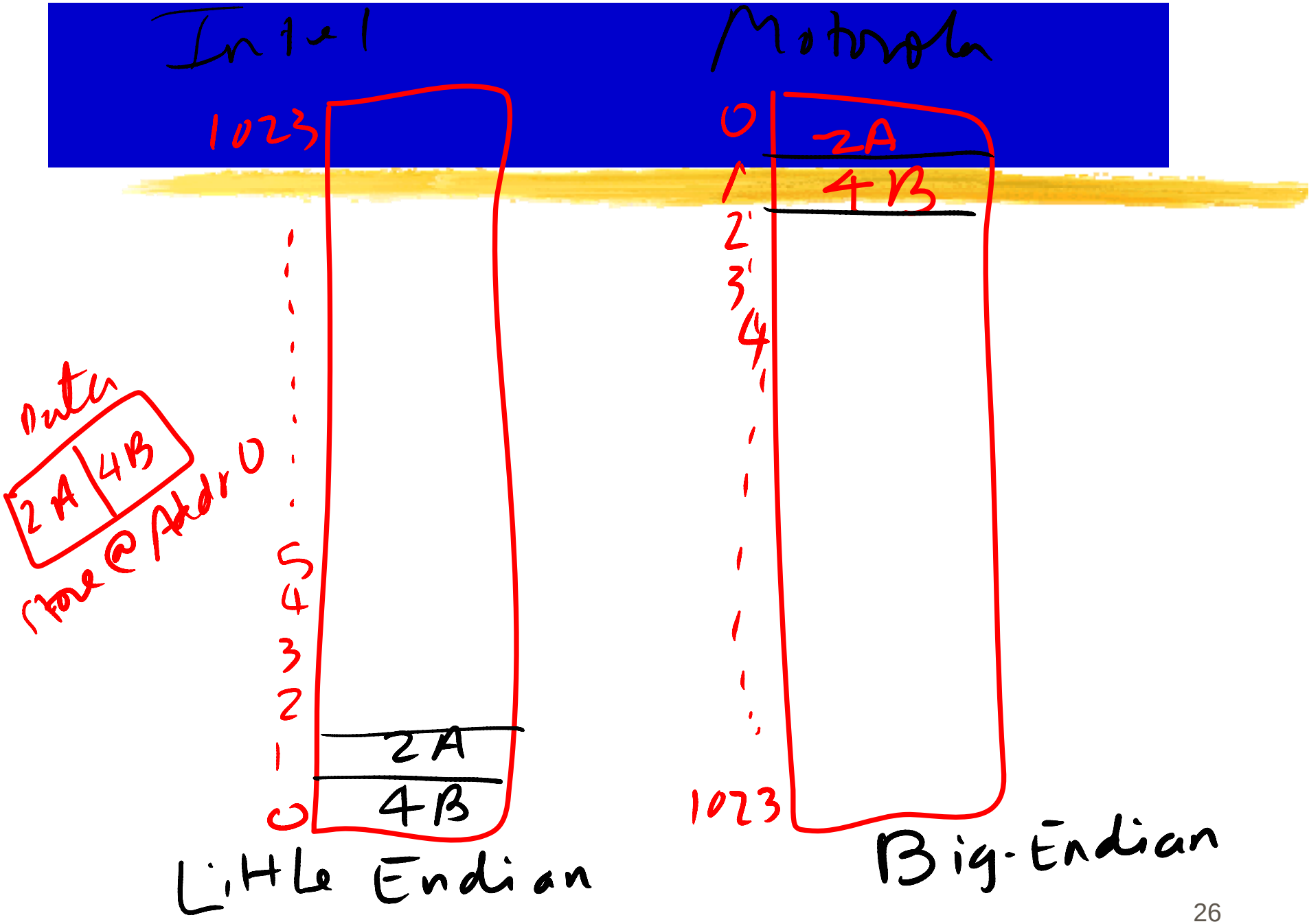
$000000	Longword 0 (MSW)
$000002	Longword 0 (LSW)
$000004	Longword 1 (MSW)
$000006	Longword 1 (LSW)

```
MOVE $3210, 0
```

$000000	32	10

```
MOVE $76543210, 0
```

$000000	76	54
$000002	32	10


Intel
Motorola
1023
0
2A
4B
1
2
3
4
5
4
3
2
1
0
2A
4B
1023
Little Endian
Big-Endian

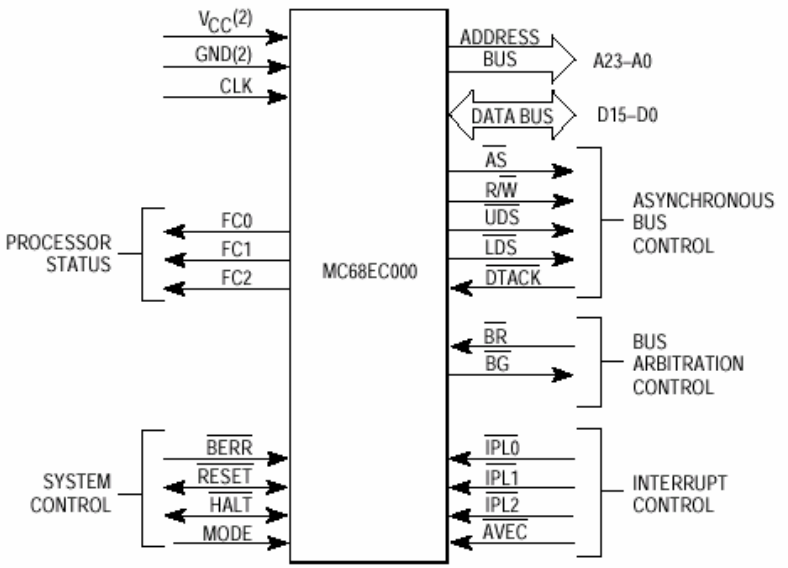
Common File Formats & Endian Order

Adobe Photoshop: Big
Bmp: Little
GIF: Little
JPEG: Big
MacPaint: Big
PC Paintbrush(pcx): Little

- William T. Verts Apr 1996
cs.umass.edu

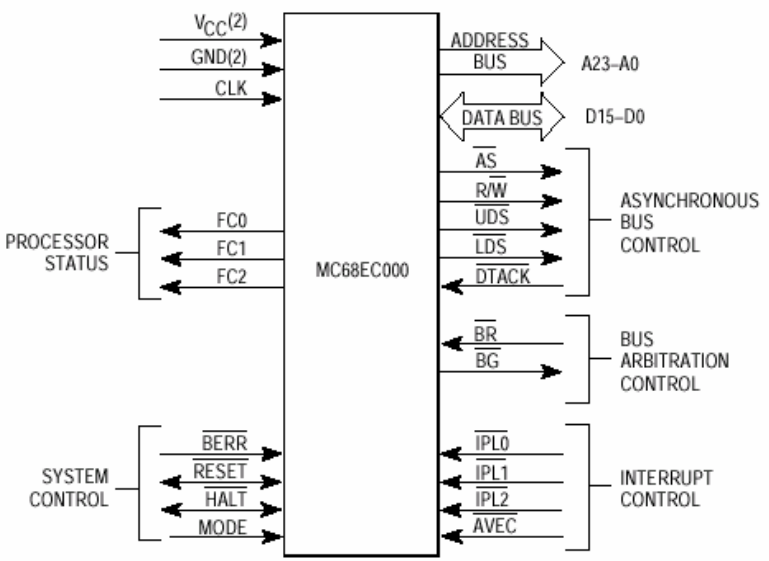
Signal Description

- **4. BUS ARBITRATION CONTROL**
  - **Bus Request (~BR)**
  - **Bus Grant (~BG)**
  - **Bus Grant Acknowledge (~BGACK)**



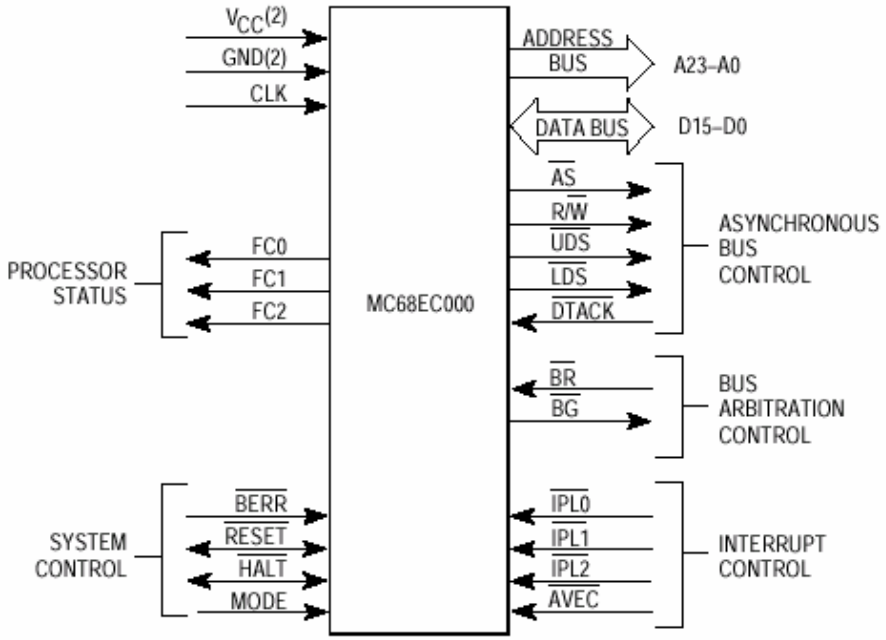
Signal Description

- **5. INTERRUPT CONTROL (**IPL0**,**IPL1**,**IPL2**)**
  - These input signals indicate the **encoded priority level of the device requesting** an interrupt.
  - **Level seven**, which cannot be masked, has the highest priority; level zero indicates that no interrupts are requested.
  - IPL0 is the least significant bit of the encoded level, and IPL2 is the most significant bit.



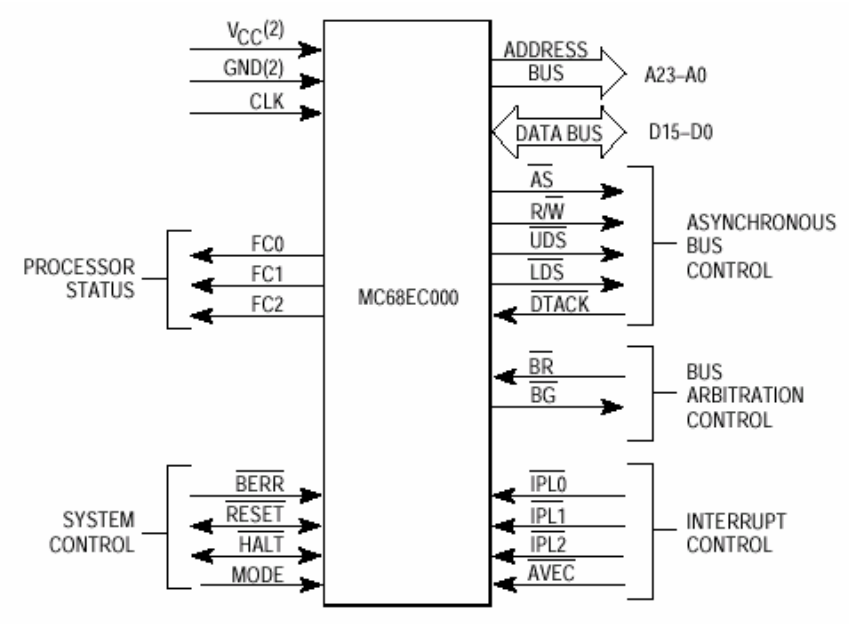
Signal Description

- **6. SYSTEM CONTROL**
  - **Bus Error (~BERR)**
  - **Reset (~RESET)**
    - The processor assertion of ~RESET (from executing a ~RESET instruction) **resets all external devices** of a system without affecting the internal state of the processor.
  - **Halt (~HALT)**
    - An input to this bidirectional signal causes the **processor to stop bus activity** at the completion of the current bus cycle.



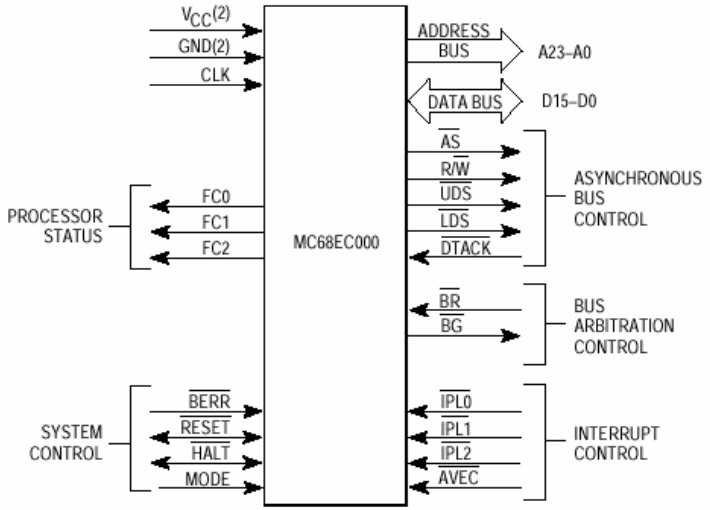
Signal Description

- **7. M6800 PERIPHERAL CONTROL**
  - **Enable (E)**
  - **Valid Peripheral Address (~VPA)**
  - **Valid Memory Address (~VMA)**



Signal Description

- **8. PROCESSOR FUNCTION CODES (FC0, FC1, FC2)**
- **9. CLOCK (CLK): 8MHz**
- **10. POWER SUPPLY (V_{CC} and GND)**



Function Code Output			
FC2	FC1	FC0	Address Space Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	CPU Space