EECE202 NETWORK ANALYSIS I Dr. Charles J. Kim

Class Note 19: Operational Amplifier (OP Amp)

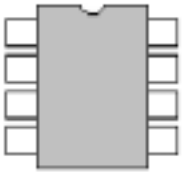
CHAPTER 5. The Operational Amplifier[1]

A. INTRODUCTION

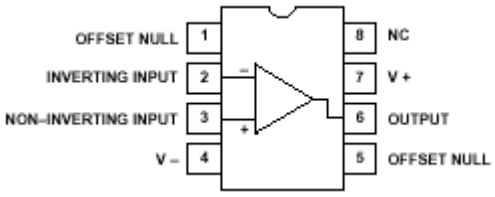
1. The *operational amplifier* or *op amp* for short, is a versatile circuit building block.
2. The *op amp* is an electronic unit that behaves like a voltage-controlled voltage source.
3. The *op amp* may also be regarded as a voltage amplifier with very high gain.
4. An op amp can sum signals, amplify a signal, integrate it, or differentiate it. The ability of the op amp to perform these mathematical operations is the main reason it is called an operational amplifier.
5. The term *operational amplifier* was introduced by John Regazzini and his colleagues, in their work on analog computers for the National Defense Research Council during World War II. The first op amps used vacuum tubes rather transistors.

B. OP AMP PACKAGE

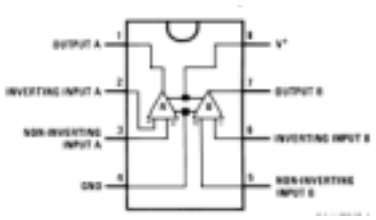
1. The op amp is an electronic device consisting of a complex arrangement of resistors, transistors, capacitors, and diodes.
2. Op amps are commercially available in integrated circuit (IC) packages in several forms. A typical one is the 8-pin single or dual in-line package (DIP) shown below.

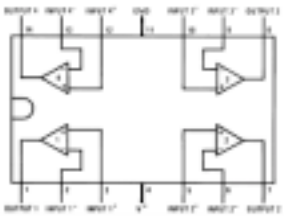


3. For a single DIP op amp (typically **uA741)**, pin or terminal 8 is unused (NC), and terminals 1 and 5 are of little concern to us.



4. For a dual DIP op amp (typically **LM348**), all 8 pins are used for two op amps [left]. A typical quad op amp (LM324) is displayed below right.



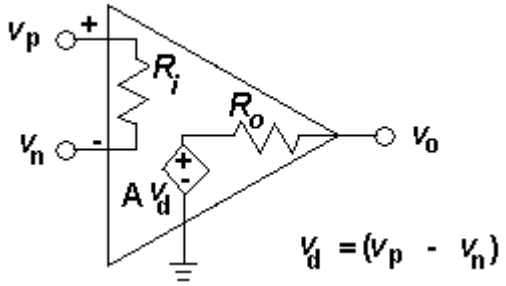


[1] The main goal of this chapter is to get student to be familiar with the node voltage method application when active elements are present in a circuit.

C. CIRCUIT SYMBOLS AND TERMINAL BEHAVIORS

1. The five important terminals in an op amp are:
   (a) Inverting input (-)
   (b) Noninverting input (+)
   (c) Output
   (d) Positive power supply, V+
   (e) Negative power supply, V-
2. The circuit symbol for the op amp is the triangle.
3. An input applied to the noninverting terminal appears with the same polarity at the output.
4. An input applied to the inverting terminal appears inverted at the output.
5. The op amp must be powered by a voltage supply.

6. The equivalent circuit model of an op amp is shown below. The output section consists of a voltage-controlled dependent voltage source in series with the output resistance R_o. The output resistance R_o is the Thevenin equivalent resistance seen at the output terminal. The input resistance R_i is the Thevenin equivalent resistance seen at the input terminals.



7. Therefore, according to above equivalent circuit of op amp, it can be said that the op amp senses the difference between the two inputs, multiplies it by the gain ***A***, and causes the resulting voltage to appear at the output.

8. The output voltage of the equivalent circuit then is given by, $v_o = A(v_p - v_n)$ where v_p is the voltage between the non inverting terminal and ground, and v_n is the voltage between the inverting terminals and ground. ***A*** is called the <u>open-loop voltage gain</u> since it is the gain of the op amp without any external feedback from output to input.

9. Typical values of voltage gain A, input resistance, output resistance, and supply voltage:

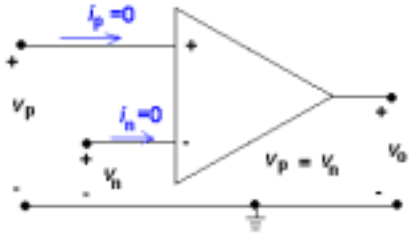
Parameters	Typical Range	Ideal Values
Open-loop gain, ***A***	10^5 - 10^8	∞
Input Resistance, R_i	10^6 - 10^{13} Ω	∞ Ω
Output Resistance, R_o	10 - 100 Ω	0 Ω
Supply Voltage, V_{cc}	5 – 24 V	

9. Output voltage limitation: The magnitude of the output voltage cannot exceed $|V_{cc}|$. Depending on the power supply voltage and the differential input voltage $v_d=v_p-v_n$, op amp can operate in three modes:
   (a) Positive saturation: $v_o = V_{cc}$
   (b) Linear region: $-V_{cc} \le v_o \le V_{cc}$
   (c) Negative saturation: $v_o = -V_{cc}$
10. The voltage transfer characteristics combine the three regions of mode.

$$v_o = \begin{cases} -V_{cc} & if \quad A(v_p - v_n) < -V_{cc} \\ A(v_p - v_n) & if \quad -V_{cc} \le A(v_p - v_n) \le +V_{cc} \\ +V_{cc} & if \quad A(v_p - v_n) > +V_{cc} \end{cases}$$

D. IDEAL OP AMP MODEL

1. An op amp is ideal if it has the following characteristics:
   (a) Infinite open-loop gain, i.e., A = ∞
   (b) Infinite input resistance, i.e., R_i=∞ Ω
   (c) Zero output resistance, i.e., R_o= 0 Ω
2. Two important characteristics of the ideal op amp for circuit analysis:
   (a) The current into both input terminals are zero, i.e., $\boldsymbol{i_p=i_n=0}$. This is due to infinite input resistance: an open circuit exists between two terminals and current cannot flow through.
   (b) The voltage across the input terminals is negligibly small, i.e., $\boldsymbol{v_p=v_n}$. This is due to infinite open-loop gain. In the linear region, the magnitude of the output voltage must be less than the supply power voltage, i.e., $-V_{cc} \le A(v_p - v_n) \le V_{cc}$. Even for a practical op amp, the gain A is about the 10^5, and the V_{cc} is just about 24V. Therefore, to satisfy the inequality for the linear region mode, $(v_p - v_n) \le \dfrac{24}{10^5} = 0.24 \times 10^{-3} = 0.24\,[\text{mV}]$.

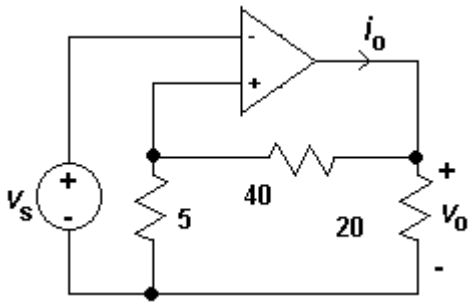


E. EXAMPLE of OP AMP CIRCUIT ANALYSIS

(using the ideal op amp model and the non-ideal op amp equivalent circuit model)

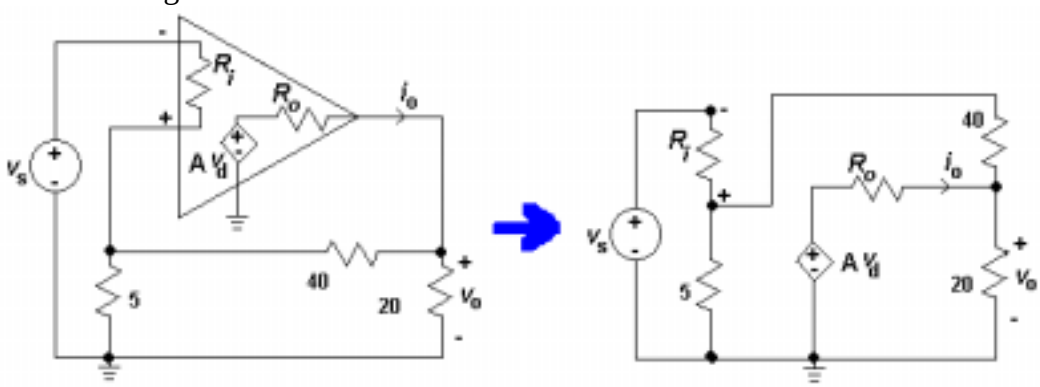
Q: Calculate the closed-loop gain (i.e., there *is* a feedback) $\frac{v_o}{v_s}$, and find i_o when $v_s = 1$[V].

(with R_i=2MΩ, R_0=50 Ω, and open-loop gain A=2x10^5.)

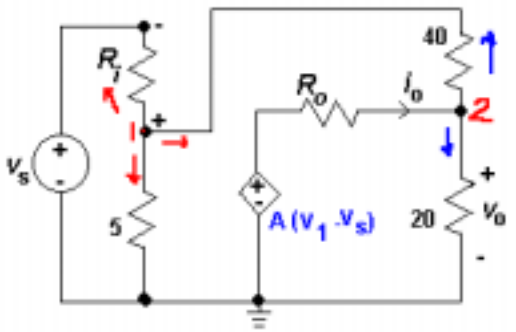


F. ANALYSIS A: using the exact (i.e., non-ideal) OP Amp model

(a) The circuit diagram and its redrawn circuit are shown below:



(b) Let's apply the node-voltage method to the right circuit.



(c) @ node 1: $\frac{V_1 - V_s}{R_i} + \frac{V_1}{5} + \frac{V_1 - V_o}{40} = 0$ (Since V_o=V_2). with V_s=1

---> $\frac{V_1 - 1}{2\times10^6} + \frac{V_1}{5} + \frac{V_1 - V_o}{40} = 0 \Rightarrow\Rightarrow (V_1 - 1) + 0.4\times10^5 V_1 + 0.05\times10^6 (V_1 - V_0) = 0$

---> $(1+0.4\times10^5+0.05\times10^6)V_1-0.05\times10^6V_0=1$ ----------(1)

(d) @ node 2: $\frac{V_o-V_1}{40}+\frac{V_2}{20}+\frac{V_0-A(V_1-V_s)}{R_o}=\frac{V_o-V_1}{40}+\frac{V_2}{20}+\frac{V_0-A(V_1-V_s)}{50}=0$

It simplifies to: $5V_0-5V_1+10V_2+4V_0-4AV_1+4AV_s=0$

Again, $19V_0-V_1(5+4A)+4AV_s=0 \Rightarrow\Rightarrow 19V_0-(5+8\times10^5)V_1+8\times10^5=0$

---> $-800005V_1+19V_0=-800000$ ----------(2)

From (1): $V_0=\frac{450001V_1-1}{50000}$

By substitution to (2): $V_1=0.9999$ and $V_0=8.999$

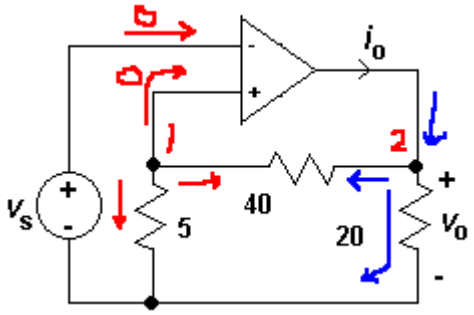
Therefore, $\frac{V_0}{V_s}=8.999$

(e) For the current i_o: applying KCL at node 2 yields:

$$i_o=\frac{V_o-V_1}{40}+\frac{V_o}{20}=\frac{3V_0-V_1}{40}=\frac{26.997-0.999}{40}=0.649\,[\text{A}]$$

F. ANALYSIS A: using the Ideal OP Amp model

(a) By the constraints of ideal op amp, $v_p=v_n$ and $i_p=i_n=0$, and node voltage method application:



(b) Constraints and hidden values: by the ideal op amp model, $V_1=V_s$ and $V_o=V_2$.

(c) @ node 1: $0+\frac{V_1-V_o}{40}+\frac{V_1}{5}=0$ ---> $V_o=9V_1=9V_s$

Therefore the closed-loop gain is: $\frac{v_o}{v_s}=9$

(d) @ node 2: $i_0=\frac{V_o-V_1}{40}+\frac{V_o}{20}=\frac{2V_o-V_s}{40}$ ---(with V_s=1)

----> $i_0=\frac{3(9V_s)-V_s}{40}=\frac{26}{40}=0.65\,[\text{A}]$