Group 1

EECE 202 (Network I) & EECE 208 (Lab)

Final Project

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Method summary

1. Analysis of the different resistor configurations
2. Binary encoding of the results gotten from 1. Above
3. Construction of a truth table from the inputs and outputs
4. Logical minimization of the anticipated circuit using karnaugh maps
5. Simulation of the circuit using PSpice
6. Conclusion

Analysis of the Resistor Configurations:

We analyzed the resistor arrangements provided in the problem statement in addition to other arrangements, and arrived at the following results:

Serial Number	Resistor Configuration	Potential Difference (V_{AB})	Output LED color
1	1-1-1	4.5	RED
2	0-2-1	9.0	X
3	1-2-0	0.0	X
4	2-0-1	3.0	GREEN
5	1-0-2	6.0	GREEN
6	0-1-2	9.0	X
7	0-0-3	9.0	YELLOW
8	3-0-0	0.0	YELLOW
9	0-3-0	0.0	X

The outputs marked X are those not covered by the initial problem statement

Table 1.1

Upon careful examination of the results above, it is evident that there exist sufficient unique V_{AB} values to establish different on conditions for each output.

N.B: Note that the V_{AB} values for the output cases marked X coincide with the values from the required outputs, so this makes it difficult to handle these other cases using this approach.

Binary Encoding of the V_{AB} Values/Construction of Truth table:

By constructing the circuit below using voltage comparators, we were able to convert the V_{AB} values into binary digits. This resulted in a 4-bit representation of each case. Let the 4-bits be A_3 A_2 A_1 A_0.

The summary of the encoding is shown in Table 2.1

Figure 2

A_3	A_2	A_1	A_0	R	G	Y	V_{AB}
0	0	0	0	0	0	1	0.0
0	0	0	1	0	1	0	3.0
0	0	1	1	1	0	0	4.5
0	1	1	1	0	1	0	6.0
1	1	1	1	0	0	1	9.0

Table 2.1

Logical Minimization of the anticipated circuit using Karnaugh maps:

RED case

A_1 A_0\ A_3 A_2	00	01	11	10
00	0	X	X	X
01	0	X	X	X
11	1	0	0	X
10	X	X	X	X

$R = A_2' A_1$

GREEN case

A_1 A_0\ A_3 A_2	00	01	11	10
00	0	X	X	X
01	1	X	X	X
11	0	1	0	X
10	X	X	X	X

$G = A_3' A_2 + A_1' A_0$

YELLOW case

$A_1 A_0 \backslash A_3 A_2$	00	01	11	10
00	1	X	X	X
01	0	X	X	X
11	0	0	1	X
10	X	X	X	X

$Y = A_3 + A_1' A_0'$

Simulation of the Circuit using PSpice:

We simulated the circuit and the schematic is shown below in figure 3.1

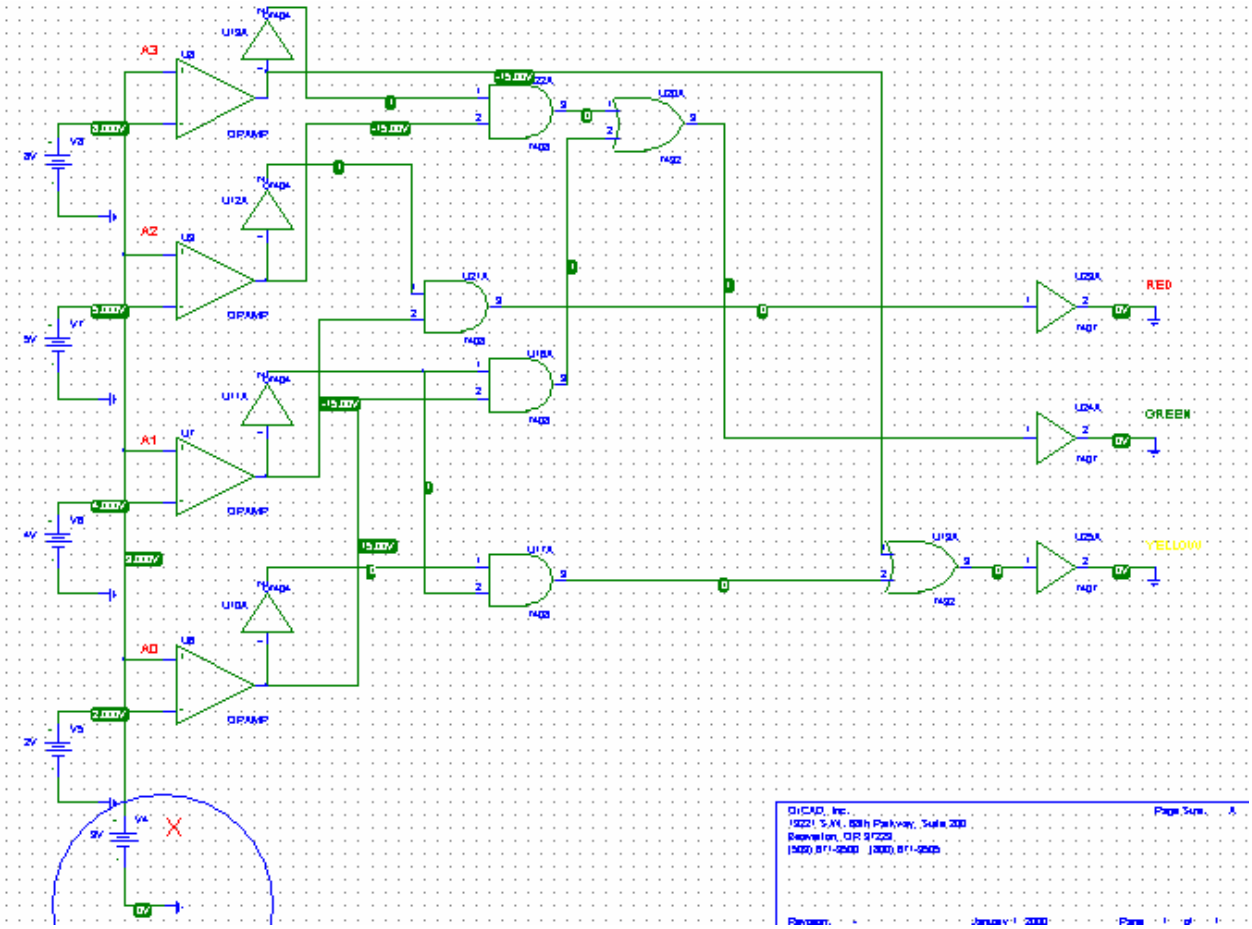

Figure 3.1 (X represents the input from the black-box circuit)

Constraints of the simulation

1. We assumed that the black box circuit was already constructed and hence utilized the output from the terminals of the black box circuit as input into our circuit. This input is denoted as X in the simulation
2. PSpice lacked the voltage comparator component, so we utilized the Op-amp instead. (This involved a minor modification to the circuit because of the operation of the amplifier, but the overall implementation was not altered)

Conclusion:

This circuit was an opportunity for us to leverage our circuit construction, Boolean logic and digital systems skills in a practical sense. We analyzed the problem, devised an intuitive approach and proceeded to simulate the circuit. The results obtained from the simulation correlated with our expected results and hence confirmed the validity of our approach. We ended up accommodating all the other resistor cases shown in table 1.1. However, their outputs could not be indicated by a separate LED (which we would have loved to do) because of the non-uniqueness of the voltage values. We realize that we may not have employed the most effective method, but hope that we can be advised on better ways of approaching similar problems.

Why we think our project is the best:

1. Design Methodology – We employed a top-down design process that allowed us to analyze the problem, brainstorm possible solutions and devise an effective solution. We devised a top level design that comprised block diagrams, and then we progressed to an intermediate level where we implemented the technique we had decided to employ and then we converted the design into low level logic gates.

2. Practical Experience - We utilized the knowledge we had garnered from the Network Analysis I class, specifically, voltage drop, resistor configurations, and voltage divider. Also we utilized the skills we had learnt from the Digital Systems class by representing the different resistor arrangements as binary coded decimals (BCD's) and then leveraged the techniques of Boolean algebra, Karnaugh maps, truth tables, logic minimization and combinational circuit design, to implement our solution.

3. Functionality - The design proved to be effective as it resulted in a minimized circuit which met all the requirements stated in the problem description. The designed allows for us to expand the functionality of the circuit to accommodate several other cases not required by this problem. Specifically, since we utilized 4 bits (word) to represent the 5 resistor arrangements, 4 bits allows us 2^4 (16) different numbers, so we can implement an additional 11 (16 – 5) cases effectively.

4. Reproducibility - We had no doubt that our circuit would work because of the approach we employed. And we can guarantee that if the design schematic is adhered-to, the circuit can be constructed anywhere in the world. We entertained no guesses or knacks but followed good circuit design.

5. Comments – We are truly impressed with ourselves, the design lets us conclude that our semester has not been in vain. We are now circuit lawyers, we are just waiting for our Professor to call us to the bar.