Chapter 14. SSP Module and I²C bus for External EEPROM Access

This chapter deals with serial peripheral interface (SPI) and Inter-IC (I^2C) bus operation using the Master Synchronous Serial Port (MSSP) module of 16F877. We only brief the SPI, and concentrate our focus on I^2C operation and its application to serial EEPROM access.

1. SSP Module and SPI Operation

The Master Synchronous Serial Port (MSSP) module of PIC 16F877 is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, display drivers, or external A/D converters. The MSSP module can operate in one of two modes: Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I^2C) bus operation. In the operation, there are two operational modes: Master and Slave modes.

The SPI mode is for transmitting and receiving 8-bits of data simultaneously. All four modes of SPI (i.e., SPI master mode, SPI slave mode, I^2C master mode, and I^2C slave mode) are supported. In SPI mode, typically three pins are used: Serial Data Out (SDO), Serial Data In (SDI), and Serial Clock (SCK). Additionally a fourth pin may be used when in a slave mode of operation: Slave Select (SS).

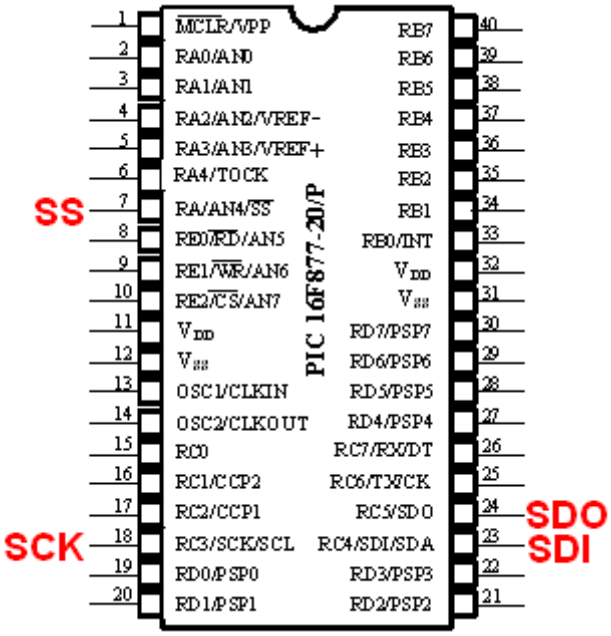

Fig. 86 SS, SCK, SDO and SDI pins of PIC 16F887

The SSP consists of a transmit/receive Shift Register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSB first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit, BF (SSPSTAT<0>), and the interrupt flag bit, SSPIF, are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be

ignored, and the write collision detect bit, WCOL (SSPCON1<7>), will be set. Our code should handle this to clear the WCOL bit so that it can be determined if the following write to the SSPBUF register completed successfully.

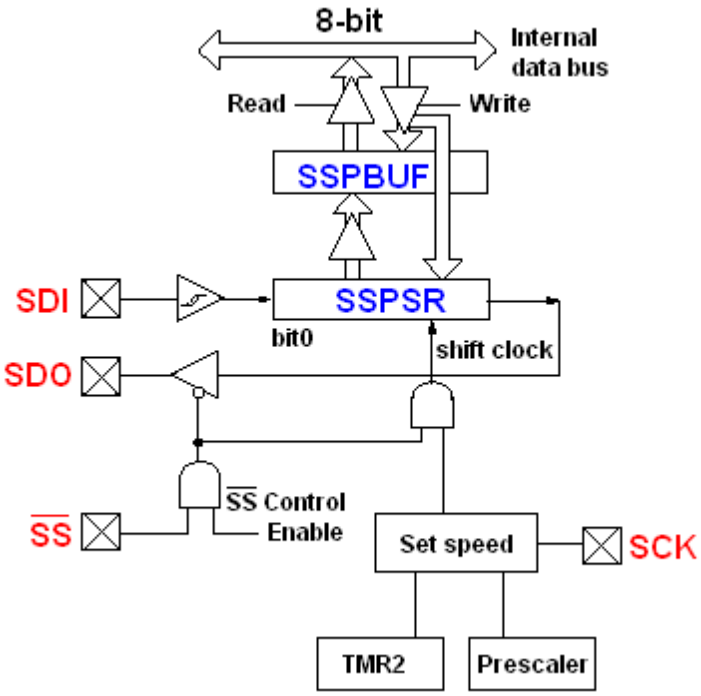

Fig. 87 Synchronous Serial Port (SSP)

When our code is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit, BF (SSPSTAT<0>), indicates when SSPBUF has been loaded with the received data (transmission is complete).
When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

Details of the SPI operation including mater and slave modes can be found in the manuals published from Microchip Technology.

2. I²C Bus Operation

A. I²C Bus-Overview

This section is greatly indebted to several publications on I²C bus from Phillips Semiconductor Co. I am merely summarizing otherwise very rich documentation on the subject. If there is any error or discrepancy between the overview here and the original documentation, it's all because of my misunderstanding or mistakes.

In consumer electronics, telecommunications and industrial electronics, there are often many similarities between seemingly unrelated designs. For example, nearly every system includes: