Chapter 12. Internal EEPROM Access

1. FLASH Memory and EEPROM

As discussed in Chapter 2 of the PIC 16F877 architecture, there is 8K Word of FLASH program memory and 256 bytes of EEPROM (Electrically Erasable Programmable Read Only Memory). EEPROM is a convenient memory which can be re-written almost indefinitely by again and again without using any external device. Since the RAM area where your filer register and variables are stored in your code is erased once power to the PIC board is turned on, this EEPROM can be a valuable storage space if you application needs a permanent data storage so that power turn-off does not affect your code. One example is storing telephone numbers into EEPROM so that it keeps the numbers even when power is lost.

FLASH memory is where your code resides and EEPROM can be access by your code.

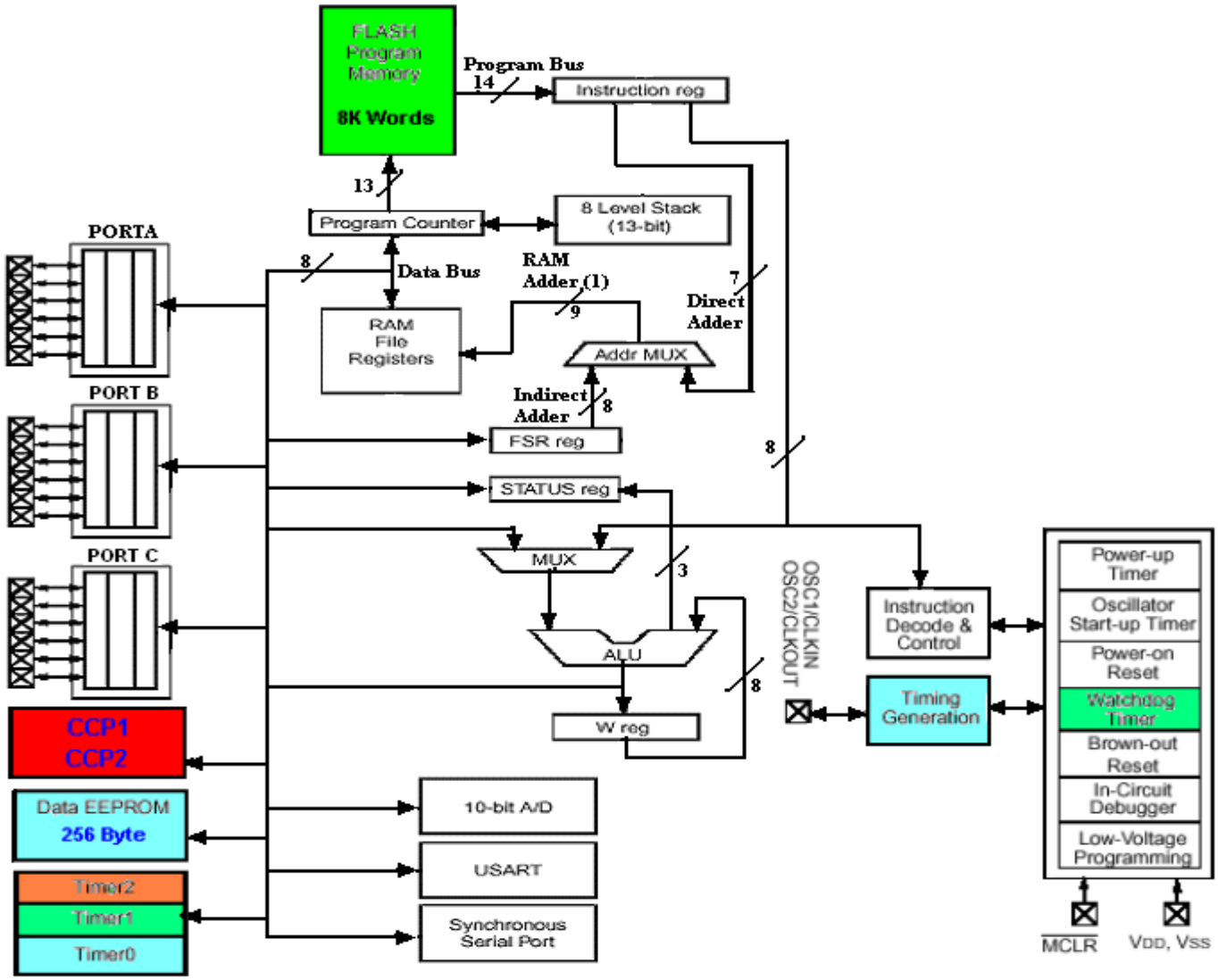

Fig. 84 FLASH memory and EEPROM

By the way, FLASH memory is a type of EEPROM chip. It has a grid of columns and rows with a cell that has two transistors at each intersection. The two transistors are separated from each other by a thin oxide layer. One of transistors is known as a floating gate and the other one is the control gate. The floating gate's only link to the row, or wordline, is through the control gate. As long as this link is in place, the cell has a value of "1". To change the value to a "0" requires a curious process called Fowler-Nordheim tunneling. Tunneling is used to alter the placement of electrons in the floating gate. An electrical charge, usually 10-13 volts, is applied to the floating gate. The charge comes from the column, or bitline, enters the floating gate and drains to a ground.

This charge causes the floating gate transistor to act like an electron gun. The excited electrons are pushed through and trapped on other side of the thin oxide layer, giving it a negative charge. These negatively charged electrons act as a barrier between the control gate and the floating gate. A special device called a cell sensor monitors the level of the charge passing through the floating gate. If the flow through the gate is greater than fifty percent of the charge, it has a value of "1". When the charge passing through drops below the fifty percent threshold, the value changes to "0". Flash memory uses in-circuit wiring to apply the electric field to the entire chip, or to predetermined sections known as blocks. This erases the targeted area of the chip, which can then be rewritten. Flash memory works much faster than traditional EEPROMs because instead of erasing one byte at a time, it erases a block or the entire chip, and then rewrites it.

This chapter discusses how we write and rewrite to EEPROM.

2. EEPROM Access

EEPROM is readable and writable in the normal operation of the code. As we saw (or could not see) from the File Register Map, there is no EEPROM space in the filer register area. This is not surprising since filer register area is with RAM not with EEPROM. This causes some problem in accessing EEPROM, since our access to I/O ports in particular is done by reading from or writing to file registers such as PORTB, TRISB, etc. The access to EEPROM is done through the following 4 file registers: EECON1 (address at 0x18C), EECON2 (not a physically implemented register), EEADR (address at 0x10C), and EEDATA (address at 0x10D).

EECON1 register controls reading and writing of EEPROM. As illustrated in the figure, the EEPGD bit is for selecting FLASH memory or EEPROM access. Apparently, for EEPROM access, the EEPGD bit must be cleared. Other bits are discussed as we move on the read and write processes.