

FPGA-based controllers and SLAM processors for autonomous navigation and task completion.

Synopsis:

This research directly addresses the ever increasing technology gap between demand for real-time computation and standard processor performance by designing application-specific, Field Programmable Gate Array (FPGA)-based processors to tackle the Simultaneous Localization and Mapping (SLAM) problem for autonomous platforms in unknown, and often hazardous, environments, SLAM requires real-time 3-D modeling for path-planning and real-time complex controllers to account for non-holonomicity, pose, and movement.

This huge computational burden requires larger processors and more power than is available, given that size, weight, and power are limiting factors in autonomous platforms. The standard solution is to trade off precision for processing-speed by simplifying control algorithms, discarding detailed sensor information, or limiting/removing feedback-loops, resulting in limited autonomy and motion.

This research takes a completely different approach, using a unique, patented, architecture to design low-power, light-weight, FPGA-based autonomous controllers and SLAM processors capable of real-time processing, analyzing, and fusing of data from a diverse array of sensors to generate 3-D maps, and also control 3-dimensional position (pose), N-degrees of freedom orientation information (pitch, roll angle, and yaw), and reactive forces between the platform and the environment. In addition, the proposed designs incorporate hardware-based cybersecurity, AI, and machine learning techniques to facilitate autonomous task completion, decision-making, swarm, and team behavior for modular robotic platforms. Moreover, FPGAs are in-situ, reconfigurable, on-the-fly, so the same platforms can be configured for a range of diverse purposes and tasks.

2018 Goals: Students will design and build a COTs based autonomous wheeled platform with Bang Bang control, PID controller, and sensor arrays (IR Rangers, Scanless Lidars), using DSPACE and HIL (hardware in the loop). Final product must be capable of autonomous navigation and establish a baseline for FPGA-based implementation.

