WWW.MWFTR.COM

NOTE: The full presentation of this abridged pdf file is located at http://140.113.144.123/Digital%2520Circuit%2520System

/Lecture/Quartus%2520II%2520Training%2520.ppt



### **Quartus II Basic Training**

## **Programmable Logic Families**

#### Low-Cost FPGAs

- Cyclone II & Cyclone
- Embedded Processor Solutions
  - Nios II
- Configuration Devices
  - Serial (EPCS) & Enhanced (EPC)





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### What is Nios II?

Altera's Second Generation Soft-Core 32 Bit RISC Microprocessor

- Nios II Plus All Peripherals Written In HDL
- Can Be Targeted For All Altera FPGAs
- Synthesis Using Quartus II Integrated Synthesis





## **Nios II Processor Architecture**

#### Classic Pipelined RISC Machine

- 32 General Purpose Registers
- 3 Instruction Formats
- 32-Bit Instructions
- 32-Bit Data Path
- Flat Register File
- Separate Instruction and Data Cache (configurable sizes)
- Tightly-Coupled Memory Options
- Branch Prediction
- 32 Prioritized Interrupts
- On-Chip Hardware (Multiply, Shift, Rotate)
- Custom Instructions
- JTAG-Based Hardware Debug Unit





Solution: Replace External Devices Copyright © 2005 Altera Corporation

### System On A Programmable Chip (SOPC) <u>Problem</u>: Reduce Cost, Complexity & Power



#### CPU is a Critical Control Function Required for System-Level Integration



## Licensing

#### Nios II Delivered As Encrypted Megacore

- Licensed Via Feature Line In Existing Quartus II License File
- Consistent With General Altera Megacore Delivery Mechanism
- Enables Detection Of Nios II In Customer Designs (Talkback)

#### No Nios II Feature Line (OpenCore Plus Mode)

- System Runs If Tethered To Host PC
- System Times Out If Disconnected from PC After ~ 1 hr
- Nios II Feature Line (Active Subscriber)
  - Subscription and New Dev Kit Customers Obtain Licenses From <u>www.altera.com</u>
  - Nios II CPU RTL Remains Encrypted
- Nios II Source License
  - Available Upon Request On Case-By-Case Basis
  - Included With Purchase Of Nios II ASIC License





### **Quartus II Basic Training**

#### Quartus II Development System Feature Overview

## **Software & Development Tools**



#### Quartus II

- All Stratix, Cyclone & Hardcopy Devices
- APEX II, APEX 20K/E/C, Excalibur, & Mercury Devices
- FLEX 10K/A/E, ACEX 1K, FLEX 6000 Devices
- MAX II, MAX 7000S/AE/B, MAX 3000A Devices

#### Quartus II Web Edition

- Free Version
- Not All Features & Devices Included
  - See <u>www.altera.com</u> for Feature Comparison



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## **Quartus II Development System**

### Fully-Integrated Design Tool

- Multiple Design Entry Methods
- Logic Synthesis
- Place & Route
- Simulation
- Timing & Power Analysis
- Device Programming



## **Typical PLD Design Flow**



## **Typical PLD Design Flow**





## **Design Entry Methods**



- EDIF
- HDL
- VQM

#### Mixing & Matching Design Files Allowed





#### Quartus II Basic Training Quartus II Quick Start LAB1

## **Objectives**

#### Create a project using the New Project Wizard

- Name the project
- Add design files
- Pick a device



## Step 1 (Setup Project for QII5\_1)

Under File, Select **New Project Wizard**.... A new window appears. If an Introduction screen appears, click Next.







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## Step 2 (Setup Project for QII5\_1)

Page 1 of the wizard should be completed with the following

working directory for this project	<pre><lab_install_directory> \Dsp_7_segment\</lab_install_directory></pre>	
name of project	Dsp_7_segment	
top-level design entity	Dsp_7_segment	

New Project Wizard: Directory, Name, Top-Lev	el Entity [page 1 of 5	]	×
What is the working directory for this projec	t?		
D:\Dsp_7_segment			
What is the name of this project?			
Dsp_7_segment			
What is the name of the top-level design er and must exactly match the entity name in	ntity for this project? T the design file.	his name is case se	ensitive
Dsp_7_segment			
Use Existing Project Settings			
		1	T-20
<u> </u>	k Next>	Finish	

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### Copy "state\_machine.v" and past in Dsp\_7\_segment

Click Next to advance to the Project Wizard: Add Files [page 2 of 5].



# Step 3 (Setup Project for QII5\_1)

Using the browse button, select state\_machine.v Add to the project. Click Next.

New Project Wizard: Add Files [page 2 of 5] Select the design files you want to include in the project in the project directory to the project. Note: you can a later. <u>F</u> ile name:	ect. Click Add All to . always add design fil	add all design files es to the project <u>A</u> dd	<
File name state_machine.v	Type Verilog H	Add A <u>I</u> <u>R</u> emove Properties Up Down	
Specify the path names of any non-default libraries.	Uger Librarie Next > F	s inish 取消	



## Step 4 (Setup Project for QII5\_1)

On page 3, select Stratix as the Family. Also, in the Filters section, set Package to FBFA, Pin count to 780, and Speed grade to 5. Select the EP1S25F780C5 device from the Available devices: window. Click Next.

Eamily:	Stratix			•		
– Target d	evice			_		
C <u>A</u> uto	device selected	by the Fitter from	the 'Ava	ailable devices' lis	st	
• <u>S</u> pe	cific device selec	ted in 'Available (	devices' l	list		
Available <u>o</u> Leonadoro	levices:			- Filters		
EP1S258 EP1S25F	67207 67206			Package:	Any	-
EP1S25F	672C7			Discount	A mu	
EP1S25F	67217 57200			Pin <u>c</u> ount:	Any	
EP1525F	780C5			Speed grade:	Any	-
EP1S25F	780C6			Core voltage:	1.5V	
EPIS25F	78016 780C7			🔽 S <u>h</u> ow Adva	anced Devices	
EP1S25F	1020C5					
EP1S25F	1020C6 1020I6			Companion de	vice	
EP1S25F	102007			HardCopy II:		~
EP1S25F	672C6_HARDCO	PY_FPGA_PRO	TO	🔽 Limit DSP	& RAM to HardO	Copy II
EPISZ5F	572U7_HARDUU	PY_FPGA_PRU	<sup>10</sup> – I	device res	ource	



# Step 5 (Setup Project for QII5\_1)

On page 4, you can specify any third party EDA tools you may be using along with Quartus II. Since these exercises will be done entirely within Quartus II, click **Next.** 

New Project Wizard: EDA Tool Se	ttings [page 4 of 5]	×
Specify the other EDA tools	in addition to the Quartus II software used with the project.	
EDA design entry / synthesis tool:	Not available	
EDA <u>s</u> imulation tool:	Not available	
EDA <u>t</u> iming analysis tool:	Not available	
	<back next=""> Finish 取消</back>	



# **Step 6 (Setup Project for QII5\_1)**

The summary screen appears as shown. Click Finish. The project is now created.

New Project Wizard: Summary [page	5 of 5]
When you click Finish, the project	ct will be created with the following settings:
Project directory: D:/交大Training/sam_test/D Project name:	)sp_7_segment/ Dsp_7_segment
Top-level design entity:	Dsp_7_segment
Number of files added:	1
Number of user libraries added:	0
Device assignments:	
Family name:	Stratix
Device:	EP1S25F780C6
EDA tools:	
Design entry/synthesis:	<none></none>
Simulation:	<none></none>
Timing analysis:	<none></none>
	< Back Next > Finish 取消





### Quartus II Basic Training Quartus II Quick Start LAB2

### **Objectives**

#### Create a counter using the MegaWizard Plug-in Manager

- Build a design using the schematic editor
- Analyze and elaborate the design to check for errors



### **Step 1** Create schematic file

Select File  $\Rightarrow$  New and select Block Diagram/Schematic File. Click OK. Select File  $\Rightarrow$  Save As and save the file as

<lab\_install\_directory> \Dsp\_7\_segment\ Dsp\_7\_segment.bdf





### Step 2 Build an 23 bits counter using the MegaWizard Plug-in Manager

1.Choose Tools ⇒ MegaWizard Plug-In Manager. In the window that appears, select Create a new custom megafunction variation. Click on Next.

2.On page 2a of the MegaWizard expand the arithmetic folder and select LPM\_COUNTER.

3.Choose Verilog HDL output For the name of the output file, type timer\_1s. Click on Next





- 1. Set the output bus to **27** bits. For the remaining settings in this window, use the defaults that appear .. Select **next**
- 2. .Turn on "Modulus , with a count modulus of "and key in 79999999
- 3. Select finish

MegaWizard Plug-In Manager - LPM_COUNTER [page 3 of 6]		
How wide should the 'q' output bus be?    27       timer 1a    What should the counter direction be?      Clock    up counter      Q(26.0)    Own only      Create an 'updown' input port to allow me to do both (1 counts up; 0 counts down)      Resource Estimate    Documentation      Cancel    < Back	Megs With and Plug-In Manager - LPM_COUNTER [page 4 of 6]         Which type of counter do you want?      Plain binary      Plain binary      Modulus, with a count modulus of 99999      Do you want any optional additional ports?      Clock Enable      Carry-in      Count Enable      Carry-out      Resource Estimate      Documentation      Cancel < Back Next >	<u>×</u> <u>Finish</u>





In the Graphic Editor, double-click in the screen so that the Symbol Window appears. Inside the symbol window, click on + to expand the symbols defined in the Project folder. Double-click on timer\_1s. Click the left mouse button to put down the symbol inside the schematic file.. The symbol for "timer\_1s" now appears in the schematic.



- 1. From the **File** menu, **open** the file **state\_machine.v**
- From the File menu, go the Create/Update menu option and select Create Symbol Files for Current File. Click Yes to save changes to Dsp\_7\_segment.bdf.
- 3. Once **Quartus II** is finished creating the symbol, click **OK**. Close the **state\_machine.v** file
- 4. In the **Graphic Editor**, **double-click** in the screen so that the **Symbol** Window appears again. **Double-click** on **state\_machine** in the **Project** folder. **Click OK.**.. *The symbol for* **state\_machine** *now appears in the schematic.*



## **Step 6 Add Pins to the Design**

Input	Output
sys_clk	7_out[60]
reset	Dig1

For each of the pins listed in left Table , you must insert a pin and change its name



- 1. To place pins in the schematic file, go to  $Edit \Rightarrow Insert \Rightarrow Symbol OR$ double-click in any empty location of the Graphic Editor.
- 2. Browse to **libraries** ⇒ **primitives** ⇒ **pin** folder. **Double-click** on **input** or **output** *Hint: To insert multiple pins select* **Repeat** *Insert Mode*.
- 3. To rename the pins double-click on the pin name after it has been inserted.
- 4. Type the name in the Pin name(s) field and Click OK



#### **Step 7** Connect the Pins and Blocks in the Schematic

- 1. In the left hand tool bar click on button to draw a wire and button to draw a bus. <u>Another</u> way to draw wires and busses is to place the cursor next to the port of any symbol. When you do this, the wire or bus tool will automatically appear.
- 2. Connect all of the pins and blocks as shown in the figure below





### **Step 8 Save and check the schematic**

- 1. Click on the **Save** button in the toolbar **I** to save the schematic.
- From the Project menu, select Add/Remove Files in Project.
  Click on the browse button to make sure the Dsp\_7\_segment.bdf, timer\_1s and state\_machine are added to the project.
- 3. From the **Processing** menu, select **Start**  $\Rightarrow$  **Start Analysis & Elaboration**.

Analysis and elaboration checks that all the design files are present and connections have been made correctly.

4. Click **OK** when analysis and elaboration is completed





### Quartus II Basic Training Quartus II Quick Start LAB3

## **Objectives**

- Pin assignment
- Perform full compilation Build a design using the schematic editor
- How to Download programming file



- 1. Choose **Assignments**  $\Rightarrow$  Assignment editor.
- 2. From the View menu, select Show All Know Pin Names.
- 3. Please click **Pin** in **Category**

	То	Location	I/O Bank	I/O Standard	General Function	Spi
1	🐼 7_out			LVTTL		
2	💿 7_out[0]			LVTTL		
3	💿 7_out[1]			LVTTL		
4	💿 7_out[2]			LVTTL		
5	💿 7_out[3]			LVTTL		
6	💿 7_out[4]			LVTTL		
7	💿 7_out[5]			LVTTL		
8	💿 7_out[6]			LVTTL		
9	iiiPreset			LVTTL		
10	iii ∎sys_clk			LVTTL		
11	< <new>&gt;</new>	< <new>&gt;</new>				



- 1. Pls install DSP Development Kit Stratix edtion CD
- 2. Open ds\_stratix\_dsp\_bd.pdf from C:\megacore\stratix\_dsp\_kit-v1.1.0\Doc
- Check clk , pushbotton and seven segment display pin location from ds\_stratix\_dsp\_bd.pdf
- 4. Key your pin number in location
- 5. Click on the **Save** button in the toolbar
- 6. From Assignments, select Device. Click Device & Pin options. Click Unused pins .Select As input tri-stated from Reserve all unused pins
- 7. From the Processing menu, select Start Compilation

	То	Location
1	7_out[0]	PIN_L18
2	7_out[1]	PIN_D24
3	7_out[2]	PIN_L23
4	💿 7_out[3]	PIN_L24
5	💿 7_out[4]	PIN_L22
6	💿 7_out[5]	PIN_L20
7	💿 7_out[6]	PIN_L19
8	🗩 reset	PIN_F24
9	iii ∎>sys_clk	PIN_K17
10	🗃 7_out	



- 1. From the **Tools** menu, select **programmer**
- 2. Click on Add File. Select Dsp\_7\_segment.sof.
- 3. Check Hardware Setup. Select your download cable on Currently selected hardware(ByteBlasterII)
- 4. Select **JTAG** from **Mode**

🛓 🔔 Hardware Setup	USB-Blaster [USB-0]				
Mode:	JTAG				
Progress:			100 %		
🔲 Enable real-time IS	P to allow background program	aming (for MAX II devic	es)		
🏓 Start	File	Device	Checksum	Usercode	Program/ Configure
🖬 Stop	Dsp_7_segment.sof	EP1S25F780	002BC2E7	FFFFFFF	
🙀 Auto Detect					
🗙 Delete					
🍰 Add File					
👺 Change File					
🖺 Save File					
🗳 Add Device					
The Up					

andware Kup Hardware Settings JTAG Setting Select a programming hardware hardware setup applies only to t	s   setup to use whe he current progra	n programming de mmer window.	vices. This programming
Currently selected hardware:	USB-Blaster [L	ISB-0]	•
Hardware USB-Blaster ByteBlasterII	Server Local Local	Port USB-0 LPT1	Add Hardware Remove Hardware
			Close



- 1. Turn on **Program/configure. Or see figure below**
- 2. Click Start
- 3. See 7-segment status

USB-Blaster [USB-0]						Mode: JTAG			Progre	Progress: 0%	
Enable real-time ISP to allow background programming (for MAX II devices)											
File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
Dsp_7_segment.sof	EP1S25F780	002BB067	FFFFFFF	<ul><li>✓</li></ul>							
	USB-Blaster [USB-0] P to allow background program File Dsp_7_segment.sof	USB-Blaster [USB-0] P to allow background programming (for MAX II devia File Device Dsp_7_segment.sof EP1S25F780	USB-Blaster [USB-0]      IP to allow background programming (for MAX II devices)      File    Device    Checksum      Dsp_7_segment.sof    EP1S25F780    002BB067	USB-Blaster [USB-0]      IP to allow background programming (for MAX II devices)      File    Device    Checksum    Usercode      Dsp_7_segment.sof    EP1S25F780    002BB067    FFFFFFFF	USB-Blaster [USB-0] IP to allow background programming (for MAX II devices) File Device Checksum Usercode Program/ Configure Dsp_7_segment.sof EP1S25F780 002BB067 FFFFFFFF ✓	USB-Blaster [USB-0]    Mc      IP to allow background programming (for MAX II devices)    File    Device    Checksum    Usercode    Program/ Configure    Verify      Dsp_7_segment.sof    EP1S25F780    002BB067    FFFFFFFF    ✓	USB-Blaster [USB-0] Mode: JTAG P to allow background programming (for MAX II devices) File Device Checksum Usercode Program/ Verify Blank- Configure Verify Check Dsp_7_segment.sof EP1S25F780 002BB067 FFFFFFFF ✓	USB-Blaster [USB-0] Mode: JTAG Programming (for MAX II devices) File Device Checksum Usercode Program/ Verify Blank- Dsp_7_segment.sof EP1S25F780 002BB067 FFFFFFFF ✓	USB-Blaster [USB-0] Mode: JTAG P to allow background programming (for MAX II devices) File Device Checksum Usercode Program/ Verify Blank- Configure Check Examine Security Bit Dsp_7_segment.sof EP1S25F780 002BB067 FFFFFFF	USB-Blaster [USB-0] Mode: JTAG ▼ Progre Pr to allow background programming (for MAX II devices) File Device Checksum Usercode Program/ Verify Blank- Configure Verify Blank- Check Examine Security Erase Dsp_7_segment.sof EP1S25F780 002BB067 FFFFFFFF ▼	. USB-Blaster [USB-0] Mode: JTAG ♥ Progress: P to allow background programming (for MAX II devices) File Device Checksum Usercode Program/ Verify Blank- Dsp_7_segment.sof EP1S25F780 002BB067 FFFFFFF ♥ ●



### **Thank You**

