

VERILOG OR SCHEMATICS

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EECE494 Computer Bus and SoC Interfacing
Electrical and Computer Engineering
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I WILL SHOW YOU HOW TO DO BOTH

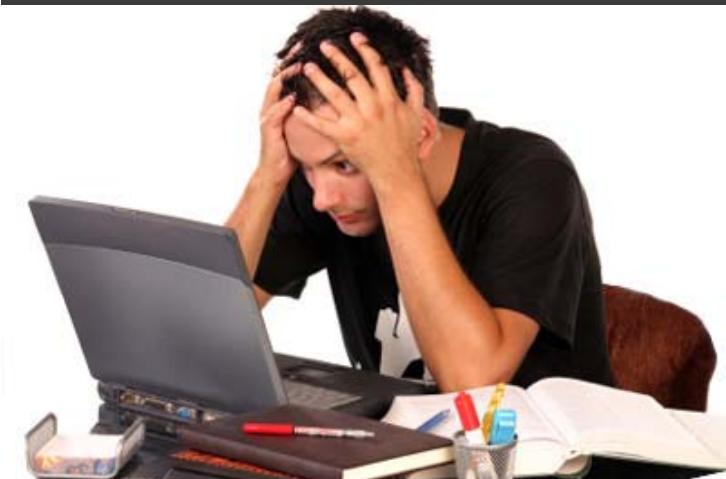
memegenerator.net



Steps



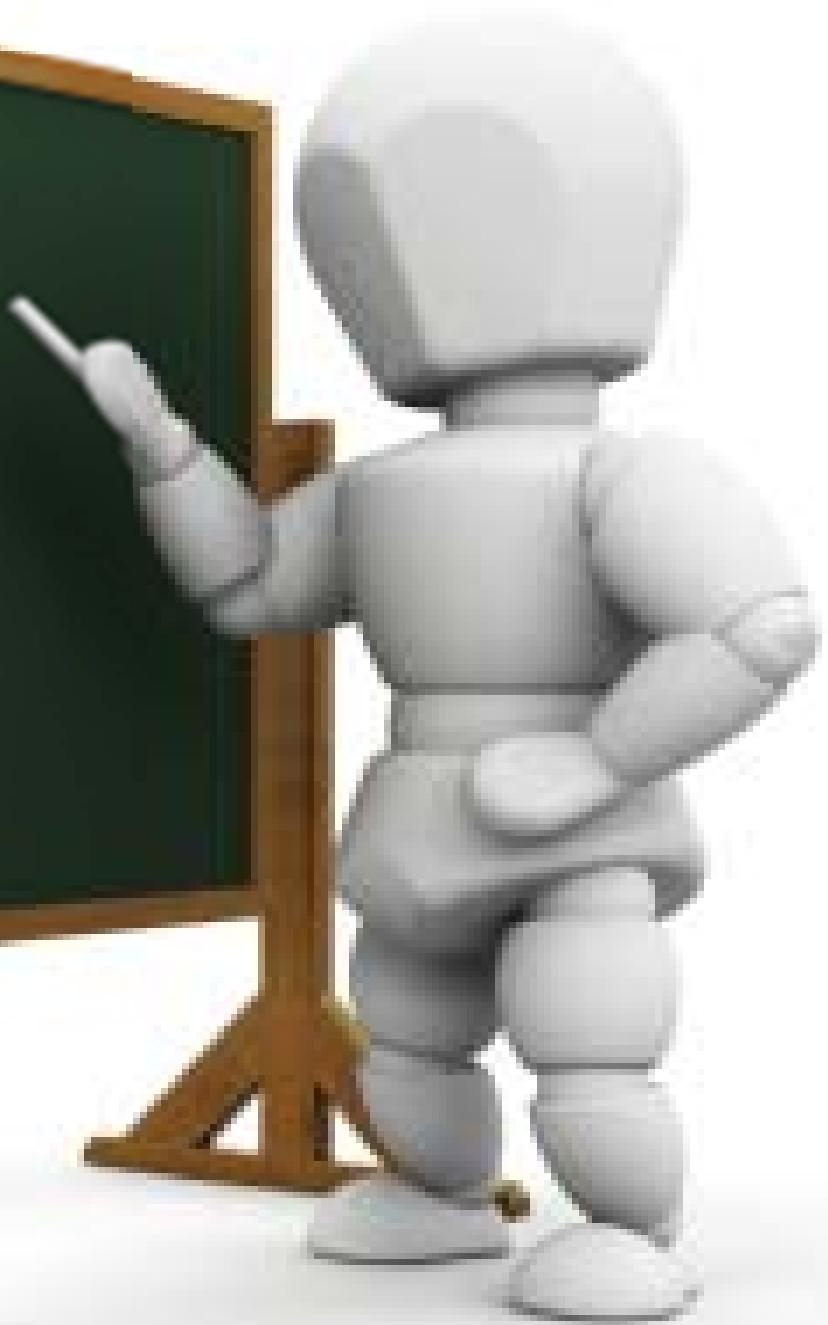
1. Aim: To create display on 7 segment display
2. Tools: What will I need
3. Research
4. Code

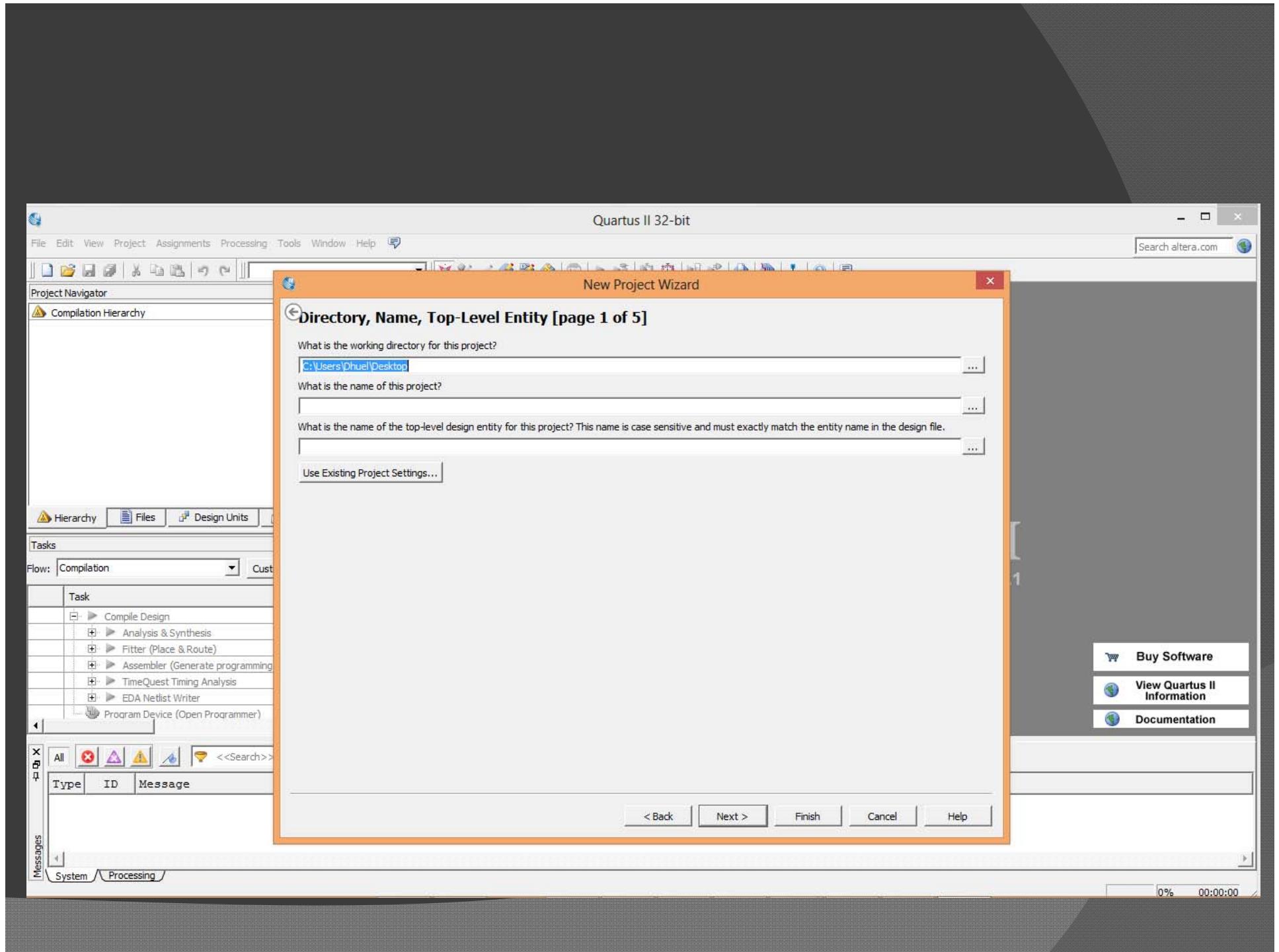


Starting Quartus

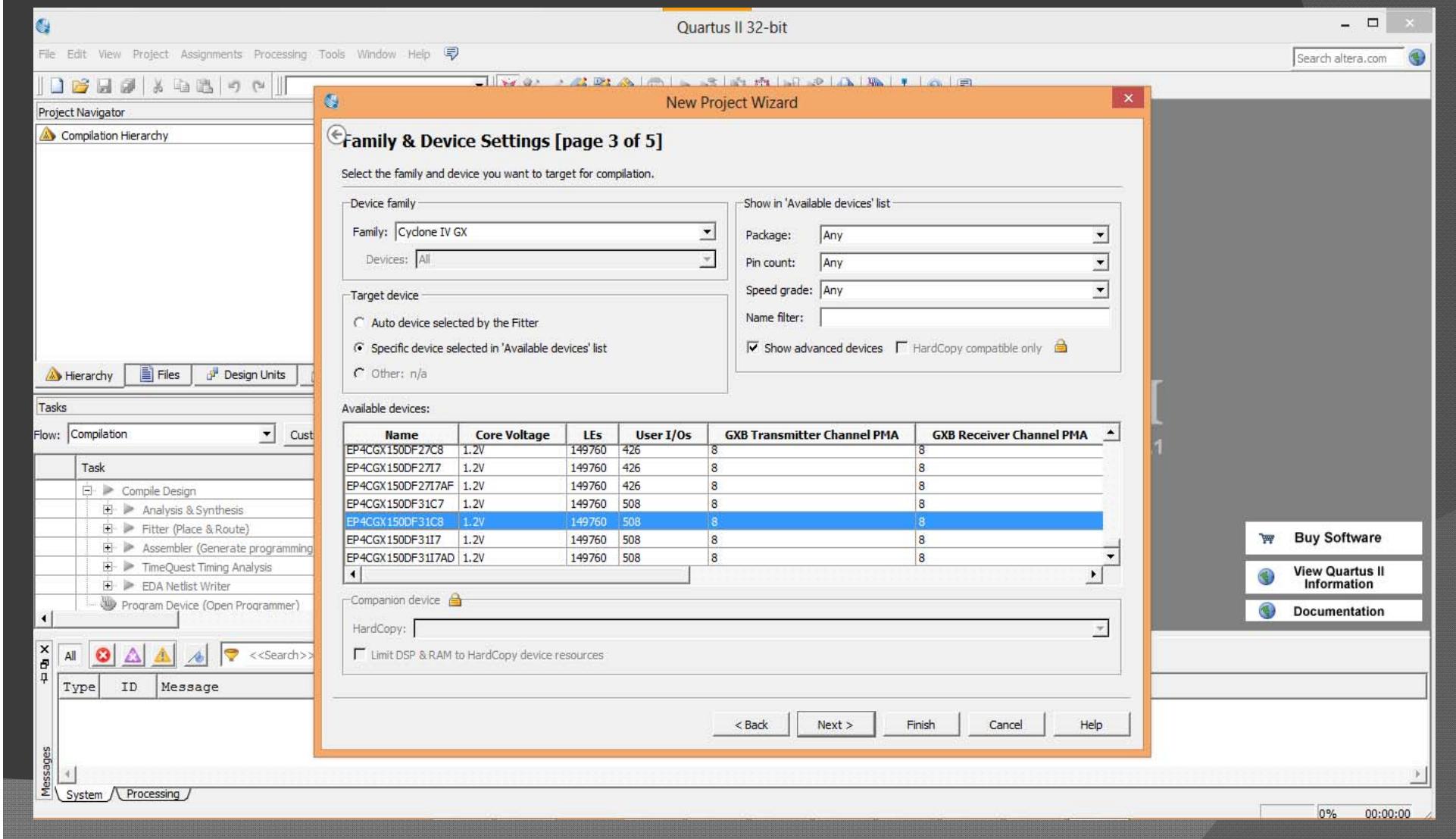


Create
New
Project

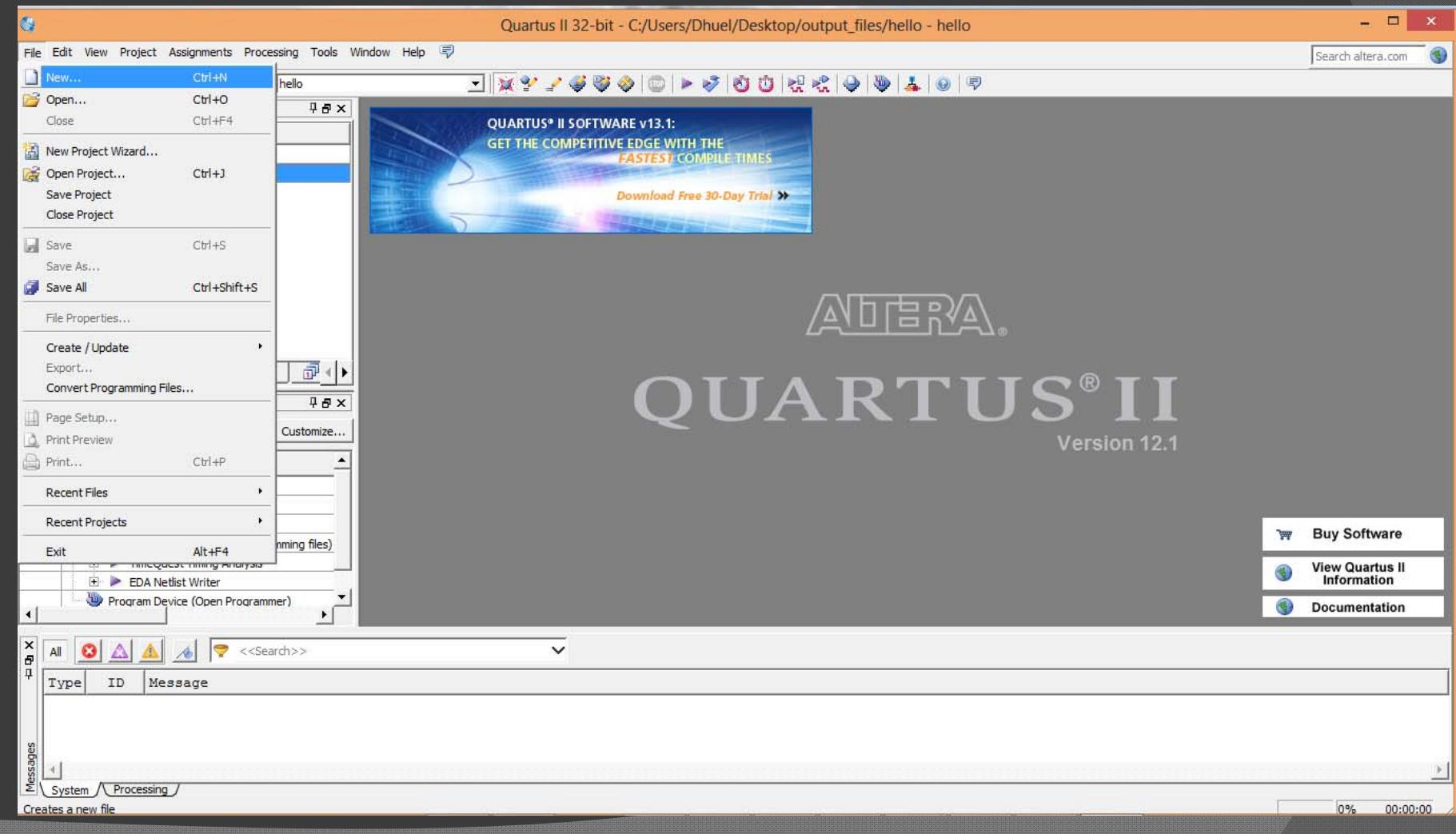




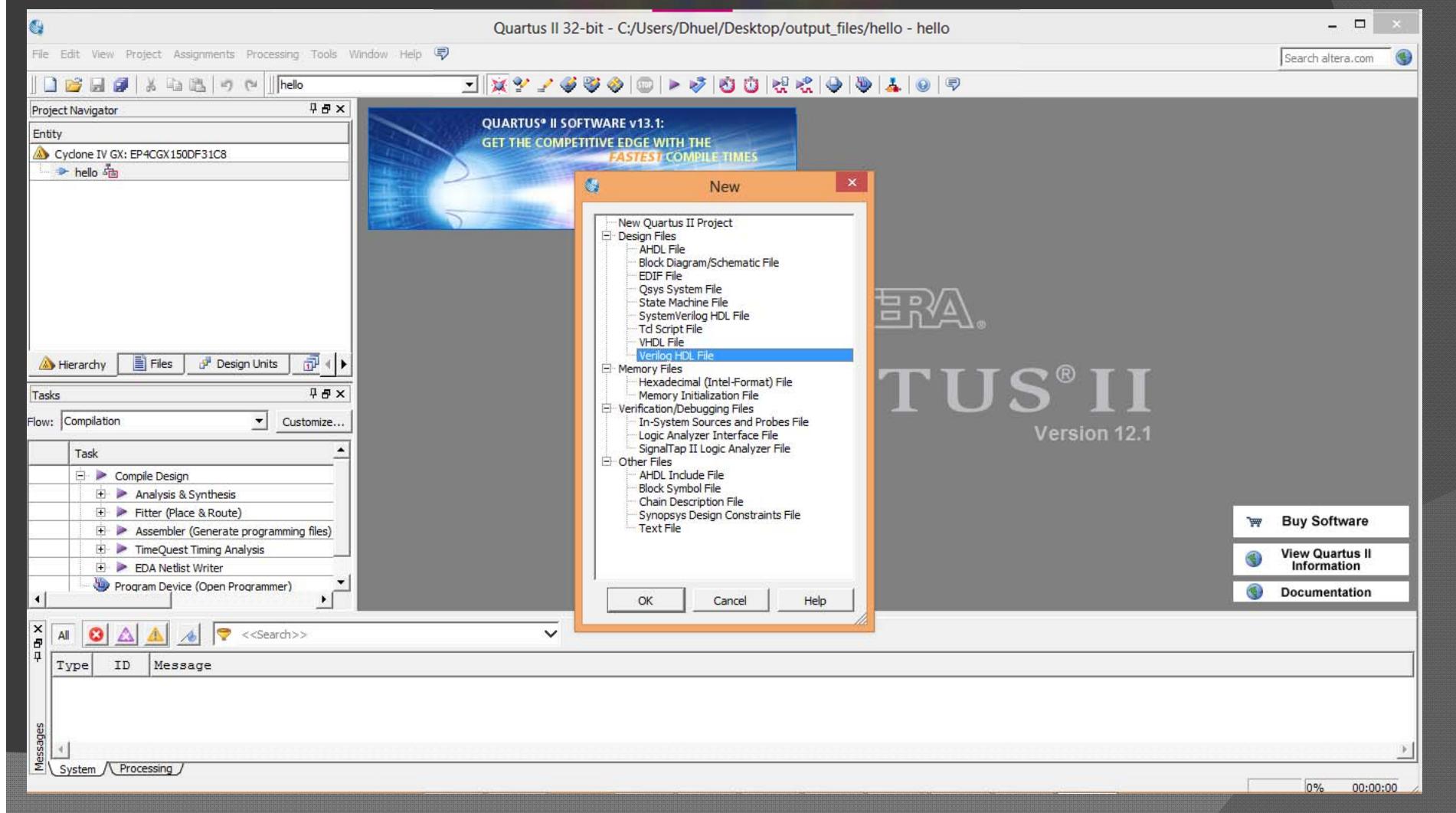
Choose Correct Device



Now, We Begin.



Verilog is FUN



Time to C-C-C-C-code



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 hello

Verilog1.v

Hierarchy Files Design Units

Tasks Flow: Compilation Customize...

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

All <<Search>>

Type	ID	Message
System / Processing		

0% 00:00:00

This screenshot shows the Quartus II software interface. The title bar indicates it's running on a 32-bit system with project 'hello' open. The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons for file operations and design tasks. The Project Navigator panel shows an entity named 'hello' for a Cyclone IV GX device (EP4CGX150DF31C8). The main workspace displays a Verilog file named 'Verilog1.v'. On the left, there are tabs for Hierarchy, Files, and Design Units. Below the workspace is a Tasks panel with a 'Compilation' flow and a list of tasks: Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming files), TimeQuest Timing Analysis, EDA Netlist Writer, and Program Device (Open Programmer). At the bottom, there is a messages panel showing 'All' logs, a search bar, and a table for messages with columns Type, ID, and Message. The status bar at the bottom right shows '0%' and '00:00:00'.

List inputs and outputs



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help Search altera.com

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 hello

..//hello.v Start Compilation Compilation Report - hello

```
1 module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2   output LED;
3   input clk;
4   reg [23:0] count;
5   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
6   endmodule
```

Hierarchy Files Design Units

Tasks Flow: Compilation Customize...

Task	Progress
Compile Design	20%
Analysis & Synthesis	0%
Fitter (Place & Route)	0%
Assembler (Generate programming files)	0%
TimeQuest Timing Analysis	0%
EDA Netlist Writer	0%
Program Device (Open Programmer)	0%

All <<Search>>

Type	ID	Message
Info	21077	Core supply voltage is 1.2V
Info	21077	Low junction temperature is 0 degrees C
Info	21077	High junction temperature is 85 degrees C

Messages System Processing (24) Starts a new compilation 20% 00:00:10

This screenshot shows the Quartus II software interface. The main window displays a Verilog code snippet for a module named 'hello'. The code defines a module with an input 'clk' and an output 'LED', and contains a register 'count' of width 23 bits. It also has four output ports: 'ssOut', 'ssOut2', 'ssOut3', and 'ssOut4', each of width 6 bits. The 'Project Navigator' panel on the left shows the project is targeting a Cyclone IV GX device (EP4CGX150DF31C8) and includes a file named 'hello'. The 'Tasks' panel indicates the compilation process is 20% complete, with 'Compile Design' being the primary task. The 'Messages' panel at the bottom shows three informational messages related to core supply voltage and junction temperatures.

Save and Compile



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 abd hello

Entity

Start Compilation Compilation Report - hello

.../hello.v

```
1 module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2   output LED;
3   input clk;
4   reg [23:0] count;
5   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
6   endmodule
```

Hierarchy Files Design Units

Tasks Flow: Compilation Customize...

Task

20% □ ► Compile Design

✓ □ ► Analysis & Synthesis

0% □ ► Fitter (Place & Route)

0% □ ► Assembler (Generate programming files)

0% □ ► TimeQuest Timing Analysis

0% □ ► EDA Netlist Writer

Program Device (Open Programmer)

All X A ! ? <<Search>>

Type ID Message

21077 Core supply voltage is 1.2V

21077 Low junction temperature is 0 degrees C

21077 High junction temperature is 85 degrees C

Messages System Processing (24)

Starts a new compilation.

20% 00:00:10



All hail google

Go to [Google](#)

and see what happens when you search the following terms:

1. Do a barrel roll
2. Askew
3. Anagram
4. Binary
5. Tilt
6. Recursion



Blackboard Learn Ariana Grande Radio - List Lexical Word Finder - Wor de2i control panel - Goog https://www.google.com/ 7 segment verilog - Goog https://www.google.com/#q=7+segment+verilog Apps song site shows python bia CLDC open stack Bacula hadoop java mysql cisco switch Micro v eng dhcp

Google 7 segment verilog

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About 86,600 results (0.38 seconds)

[Verilog: Seven Segment Display Decoder | Death by Logic](#)
www.deathbylogic.com/2008/12/verilog-seven-segment-display-decoder/ ▾
Dec 16, 2008 - Verilog: Seven Segment Display Decoder. Posted on December 16, ...
7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27.
You've visited this page 2 times. Last visit: 2/23/14

[PPT 7-Segment LED Display](#)
www.sonoma.edu.../ES210_Spring_2013_Lect... ▾ Sonoma State University
7-Segment LED Display. DD: Section 5.1-5.2 ... 7'b0000001 means 7 binary numbers. with a sequence ... Verilog actually defines four possible. Values for each ...
You've visited this page 2 times. Last visit: 2/23/14

[verilog - BCD and 7segment decoder show strange result - Stack ...](#)
stackoverflow.com/.../bcd-and-7segment-decoder-show-s... ▾ Stack Overflow
Dec 18, 2013 - I'm trying to create connection from BCD to 7-segment decoder. Well played, sir ... Greg , I'm already fix the design bug. But can't found the ...

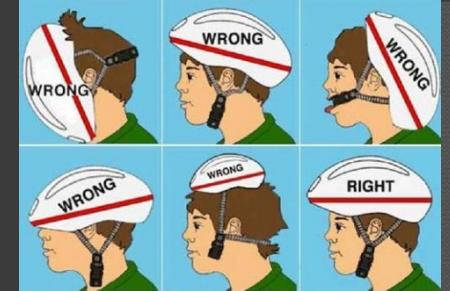
[seven segment display - Verilog: task using case not choosing the ...](#)
stackoverflow.com/.../verilog-task-using-case-not-choosi... ▾ Stack Overflow
Oct 31, 2013 - Verilog: task using case not choosing the correct case ... I'm using 7-segment for the 4 digit, hex[6:0], 1 is off. output reg [6:0] hex3, hex2, hex1, ...

[PDF Project: Binary to BCD to 7-Segment Conversion - ECEE](#)
ecee.colorado.edu/~ecen2350/pdf/binary2BCDproject.pdf ▾
Oct 29, 2013 - Project: Binary to BCD to 7-Segment Conversion. The goal of this project is to write parametrized (and scalable) Verilog code for the conversion.

[Verilog Programming Exercises - University of Minnesota](#)



Use it as a guide



This code will take a four bit number and decode it into the seven individual segments to drive a seven segment display. *nIn* is the four bit number to be decoded and *ssOut* is the array of segments for the display going from **a**, being the LSB, to **g** being the MSB.

```
1 module SevenSegmentDisplayDecoder(ssOut, nIn);
2   output reg [6:0] ssOut;
3   input [3:0] nIn;
4
5   // ssOut format {g, f, e, d, c, b, a}
6
7   always @(nIn)
8     case (nIn)
9       4'h0: ssOut = 7'b0111111;
10      4'h1: ssOut = 7'b0000110;
11      4'h2: ssOut = 7'b1011011;
12      4'h3: ssOut = 7'b1001111;
13      4'h4: ssOut = 7'b1100110;
14      4'h5: ssOut = 7'b1101101;
15      4'h6: ssOut = 7'b1111101;
16      4'h7: ssOut = 7'b0000111;
17      4'h8: ssOut = 7'b1111111;
18      4'h9: ssOut = 7'b1100111;
19      4'hA: ssOut = 7'b1110111;
20      4'hB: ssOut = 7'b1111100;
21      4'hC: ssOut = 7'b0111001;
22      4'hD: ssOut = 7'b1011110;
23      4'hE: ssOut = 7'b1111001;
24      4'hF: ssOut = 7'b1110001;
25      default: ssOut = 7'b1001001;
26    endcase
27 endmodule
```

Change Log:
11/1/2010: Added default case statement to prevent possible latching.

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This entry was posted in [Code](#), [Hardware](#) and tagged [Decoder](#), [FPGA](#), [Seven Segment](#), [Verilog](#) by Daniel. Bookmark the [permalink](#).



Compile and save

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 abd hello

..//hello.v Start Compilation Compilation Report - hello

```
1 module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2   output LED;
3   input clk;
4   reg LEDstatus;
5   reg [23:0] count;
6   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7   reg [3:0] nIn;
8   assign LED = LEDstatus;
9
10  always @ (posedge clk) begin
11    LEDstatus <= count[23];
12    count    <= count + 1;
13  end
14
15
16
17
18 endmodule
```

Tasks Flow: Compilation Customize...

Task
22% □ ► Compile Design
13% ✓ ► Analysis & Synthesis
0% □ ► Fitter (Place & Route)
0% □ ► Assembler (Generate programming files)
0% □ ► TimeQuest Timing Analysis
0% □ ► EDA Netlist Writer

Program Device (Open Programmer)

All <<Search>>

Type ID Message

- + 176444 Device migration not selected. If you intend to use device migration later, you may need to change the pin assignments as they may be incompatible with .
- + 169124 Fitter converted 5 user pins into dedicated programming pins
- 15714 Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details

Messages System Processing (29)

Starts a new compilation 22% 00:00:12

Almost there



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity ..hello.v* Compilation Report - hello

Cyclone IV GX: EP4CGX150DF31C8

Entity: hello

Tasks Flow: Compilation

Task: Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming files), TimeQuest Timing Analysis, EDA Netlist Writer

Code Editor:

```
2     output LED;
3     input clk;
4     reg LEDstatus;
5     reg [23:0] count;
6     output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7     reg [2:0] nIn;
8     assign LED = LEDstatus;
9
10    always @ (posedge clk) begin
11        LEDstatus <= count[23];
12        count   <= count + 1;
13    end
14    always @ (posedge LEDstatus) begin
15        nIn <= nIn + 1;
16        case (nIn)
17            4'h0: ssOut = 7'b0001001;
18            4'h1: ssOut = 7'b0000110;
19            4'h2: ssOut = 7'b1000111;
20            4'h3: ssOut = 7'b1000111;
21            4'h4: ssOut = 7'b1000000;
22            4'h5: ssOut = 7'b1111111;
23            4'h6: ssOut = 7'b1111111;
24            4'h7: ssOut = 7'b1111111;
25            4'h8: ssOut = 7'b1111111;
26        default: ssOut = 7'b00000000;
27    endmodule
```

Messages:

- 204019 Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
- Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
- 293000 Quartus II Full Compilation was successful. 0 errors, 43 warnings

System Processing (120)

Ln 26 Col 36 Verilog HDL File 100% 00:02:02

A screenshot of the Quartus II 32-bit software interface. The main window shows a Verilog code editor with the file ..\hello.v*. The code defines an entity named hello with an output LED, an input clk, and various internal registers and assignments. It includes two always blocks: one for the clock edge and another for the LED status. A case statement handles the nIn input to generate different ssOut values based on the binary representation of nIn. The interface also features a Project Navigator, a Tasks list showing successful compilation steps, and a Messages window displaying build logs for EDA simulation, netlist writer, and full compilation.



Errors

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity/hello.v* Compilation Report - hello

Entity: Cyclone IV GX: EP4CGX150DF31C8

Hierarchy Files Design Units Tasks Flow: Compilation

Task: Compile Design Analysis & Synthesis Fitter (Place & Route) Assembler (Generate programming files) TimeQuest Timing Analysis EDA Netlist Writer Program Device (Open Programmer)

Code Editor:

```
2   output LED;
3   input clk;
4   reg LEDstatus;
5   reg [23:0] count;
6   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7   reg [2:0] nIn;
8   assign LED = LEDstatus;
9
10  always @(posedge clk) begin
11    LEDstatus <= count[23];
12    count     <= count + 1;
13  end
14  always @(posedge LEDstatus) begin
15    nIn <= nIn + 1;
16    case (nIn)
17      4'h0: ssOut = 7'b00001001;
18      4'h1: ssOut = 7'b00000110;
19      4'h2: ssOut = 7'b10000111;
20      4'h3: ssOut = 7'b10000111;
21      4'h4: ssOut = 7'b10000000;
22      4'h5: ssOut = 7'b11111111;
23      4'h6: ssOut = 7'b11111111;
24      4'h7: ssOut = 7'b11111111;
25      4'h8: ssOut = 7'b11111111;
26    default: ssOut = 7'b00000000;
27  end
28 endmodule
```

Messages:

Type	ID	Message
✗	10170	Verilog HDL syntax error at hello.v(27) near text "endmodule"; expecting "endcase"
✗	293001	Quartus II 32-bit Analysis & Synthesis was unsuccessful. 1 error, 0 warnings
✗	293001	Quartus II Full Compilation was unsuccessful. 3 errors, 0 warnings

System Processing (3) 2% 00:00:04

COMPILED



Let's test it!!!!



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity

Cydone IV GX: EP4CGX abd hello

Assignment Editor Ctrl+Shift+A Pin Planner Ctrl+Shift+N

Remove Assignments... Back-Annotate Assignments... Import Assignments... Export Assignments... Assignment Groups...

LogiLock Regions Window Design Partitions Window

Hierarchy Files Design Units

Tasks Flow: Compilation Customize...

Task

Compile Design Analysis & Synthesis Fitter (Place & Route) Assembler (Generate programming files) TimeQuest Timing Analysis EDA Netlist Writer Program Device (Open Programmer)

204019 Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings 293000 Quartus II Full Compilation was successful. 0 errors, 37 warnings

System Processing (123)

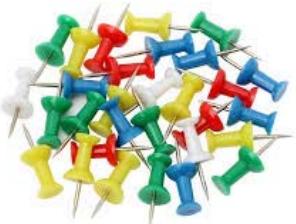
Edits pin assignments

100% 00:02:05

Code Snippet:

```
module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
    input LED;
    input clk;
    output reg [23:0] count;
    output reg [6:0] ssOut, ssOut2, ssOut3, ssOut4;
    input [2:0] nIn;
    assign LED = LEDstatus;

    always @(posedge clk) begin
        LEDstatus <= count[23];
        count <= count + 1;
    end
    always @(posedge LEDstatus) begin
        nIn <= nIn + 1;
        case (nIn)
            4'h0: ssOut = 7'b0001001;
            4'h1: ssOut = 7'b0000110;
            4'h2: ssOut = 7'b1000111;
            4'h3: ssOut = 7'b1000111;
            4'h4: ssOut = 7'b1000000;
            4'h5: ssOut = 7'b1111111;
            4'h6: ssOut = 7'b1111111;
            4'h7: ssOut = 7'b1111111;
            4'h8: ssOut = 7'b1111111;
            default: ssOut = 7'b00000000;
        endcase
    end
endmodule
```



Assign pins

Pin Planner - C:/altera/output_files/hello - hello

File Edit View Processing Tools Window Help

Groups Node Name

Named: *

Report Report not available

Tasks Run Ana Early Pin Early Run Export Change

Top View - Wire Bond
Cyclone IV GX - EP4CGX150DF31C8

PIN_D16

Node Name Direction Location I/O Bank VREF Group Filter L

Node Name	Direction	Location	I/O Bank	VREF Group	Filter L
out LED	Output			PIN_F16	
in clk	Input			PIN_W15	
out ssOut[6]	Output	PIN_F14	8	B8_N0	PIN_AH2
out ssOut[5]	Output	PIN_D16	8	B8_N0	PIN_AE1
out ssOut[4]	Output			PIN_AD1	
out ssOut[3]	Output			PIN_AH3	
out ssOut[2]	Output			PIN_A13	

0% 00:00:00

DE2i-150_FPGA_System_manual.pdf - Adobe Reader

File Edit View Window Help

Comment Share

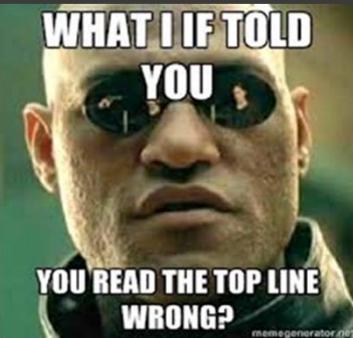
Convert file to PDF using Adobe CreatePDF online

Click on Comment and Share to create, mark-up and send PDF files.

Figure 3-11 Connections between the 7-segment display HEX0 and Cyclone IV GX FPGA

Table 3-5 Pin Assignments for 7-segment Displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX0[0]	PIN_E15	Seven Segment Digit 0[0]	2.5V
HEX0[1]	PIN_E12	Seven Segment Digit 0[1]	2.5V
HEX0[2]	PIN_G11	Seven Segment Digit 0[2]	2.5V
HEX0[3]	PIN_F11	Seven Segment Digit 0[3]	2.5V
HEX0[4]	PIN_F16	Seven Segment Digit 0[4]	2.5V
HEX0[5]	PIN_D16	Seven Segment Digit 0[5]	2.5V
HEX0[6]	PIN_F14	Seven Segment Digit 0[6]	2.5V
HEX1[0]	PIN_G14	Seven Segment Digit 1[0]	2.5V
HEX1[1]	PIN_B13	Seven Segment Digit 1[1]	2.5V
HEX1[2]	PIN_G13	Seven Segment Digit 1[2]	2.5V
HEX1[3]	PIN_F12	Seven Segment Digit 1[3]	2.5V
HEX1[4]	PIN_G12	Seven Segment Digit 1[4]	2.5V
HEX1[5]	PIN_J9	Seven Segment Digit 1[5]	2.5V
HEX1[6]	PIN_G10	Seven Segment Digit 1[6]	2.5V
HEX2[0]	PIN_G8	Seven Segment Digit 2[0]	2.5V
HEX2[1]	PIN_G7	Seven Segment Digit 2[1]	2.5V
HEX2[2]	PIN_F7	Seven Segment Digit 2[2]	2.5V
HEX2[3]	PIN_AG30	Seven Segment Digit 2[3]	2.5V
HEX2[4]	PIN_F6	Seven Segment Digit 2[4]	2.5V
HEX2[5]	PIN_F4	Seven Segment Digit 2[5]	2.5V
HEX2[6]	PIN_F10	Seven Segment Digit 2[6]	2.5V
HEX3[0]	PIN_D10	Seven Segment Digit 3[0]	2.5V
HEX3[1]	PIN_D7	Seven Segment Digit 3[1]	2.5V
HEX3[2]	PIN_E6	Seven Segment Digit 3[2]	2.5V
HEX3[3]	PIN_E4	Seven Segment Digit 3[3]	2.5V
HEX3[4]	PIN_E3	Seven Segment Digit 3[4]	2.5V
HEX3[5]	PIN_D5	Seven Segment Digit 3[5]	2.5V
HEX3[6]	PIN_D4	Seven Segment Digit 3[6]	2.5V
HEX4[0]	PIN_A14	Seven Segment Digit 4[0]	2.5V
HEX4[1]	PIN_A13	Seven Segment Digit 4[1]	2.5V



Don't forget to compile

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity

Cyclone IV GX: EP4CGX150DF31C8

abd hello

..//hello.v Start Compilation Compilation Report - hello

```
1 module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2 output LED;
3 input clk;
4 reg LEDstatus;
5 reg [23:0] count;
6 output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7 reg [2:0] nIn;
8 assign LED = LEDstatus;
9
10 always @ (posedge clk) begin
11     LEDstatus <= count[23];
12     count <= count + 1;
13 end
14 always @ (posedge LEDstatus) begin
15     nIn <= nIn + 1;
16     case (nIn)
17         4'h0: ssOut = 7'b0001001;
18         4'h1: ssOut = 7'b0000010;
19         4'h2: ssOut = 7'b1000111;
20         4'h3: ssOut = 7'b1000111;
21         4'h4: ssOut = 7'b1000000;
22         4'h5: ssOut = 7'b11111111;
23         4'h6: ssOut = 7'b11111111;
24         4'h7: ssOut = 7'b11111111;
25         4'h8: ssOut = 7'b11111111;
26         default: ssOut = 7'b00000000;
27     endcase

```

Hierarchy Files Design Units

Tasks Flow: Compilation

16% □ Compile Design

0% □ Analysis & Synthesis

0% □ Fitter (Place & Route)

0% □ Assembler (Generate programming files)

0% □ TimeQuest Timing Analysis

0% □ EDA Netlist Writer

Program Device (Open Programmer)

All <<Search>>

Type ID Message

+ 176214 Statistics of I/O pins that need to be placed that use the same VCCIO and VREF, before I/O pin placement

+ 176215 I/O bank details before I/O pin placement

- 171121 Fitter preparation operations ending: elapsed time is 00:00:09

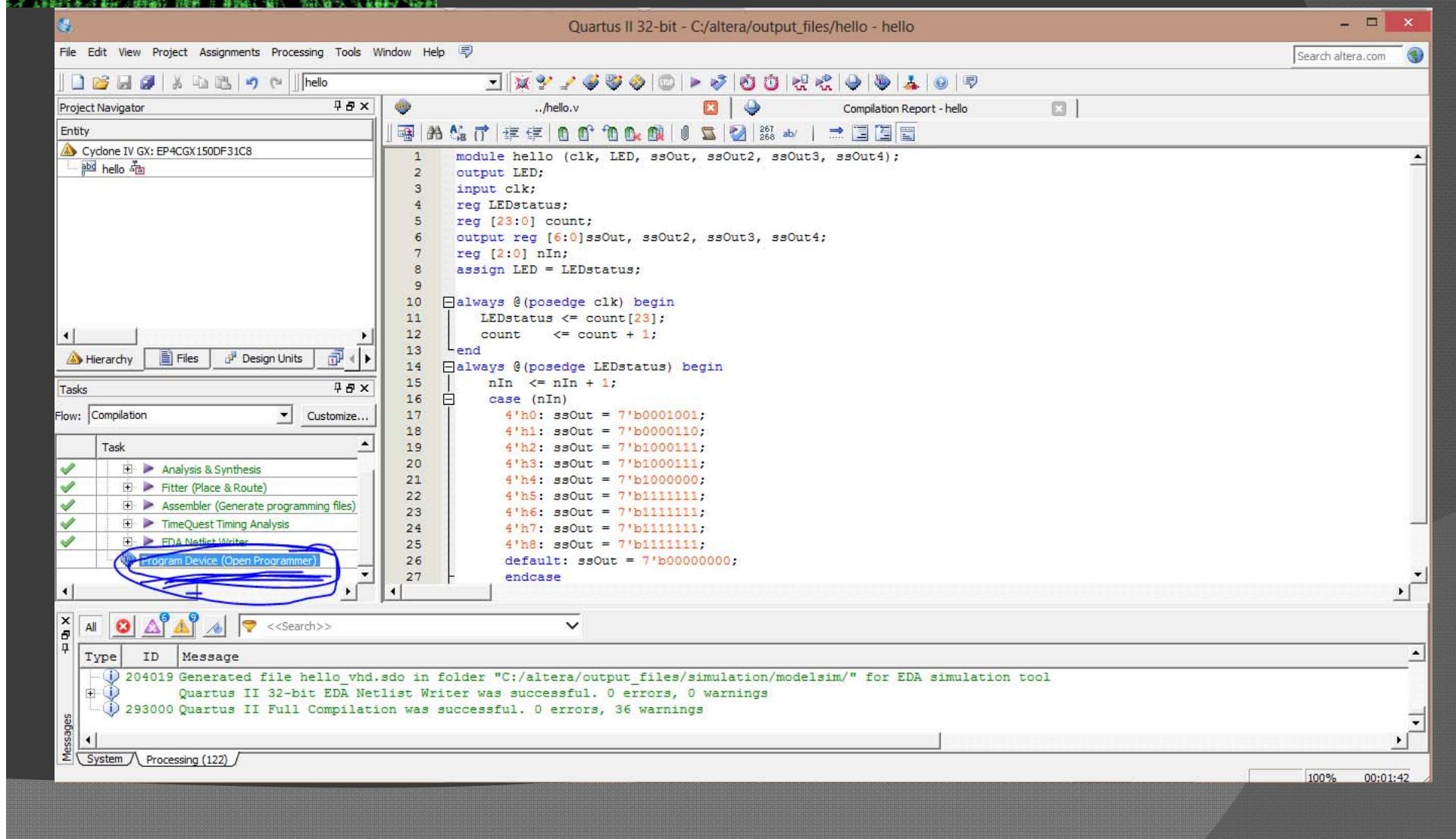
Messages

System Processing (44)

Starts a new compilation

26% 00:00:33

Program device





USB blaster and JTAG



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help Search altera.com

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 abd hello

Tasks Flow: Compilation Task Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming files), TimeQuest Timing Analysis, EDA Netlist Writer, Program Device (Open Programmer)

Programmer - C:/altera/output_files/hello - hello - [output_files/hel...]

File Edit View Processing Tools Window Help Search altera.com

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device Up Down

File	Device	Checksum	Usercode	Pn Co
output_files/hello.sof	EP4CGX150DF31	007269E9	FFFFFF	

TDI ALTRA

Messages Type ID Message

- 204019 Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
- Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
- 293000 Quartus II Full Compilation was successful. 0 errors, 36 warnings

System Processing (122) 100% 00:01:42



Almost there

Programmer - C:/altera/output_files/hello - hello - [output_files/hello.cdf]*

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 35%

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/hello.sof	EP4CGX150DF31	007269E9	FFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>					

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

The diagram shows a rectangular FPGA chip with the brand name "ALTERA" printed on it. Below the chip, the part number "EP4CGX150DF31" is written. Two pins on the left side are labeled "TDI" and "TDO". A small arrow points from the "TDI" pin towards the chip, and another arrow points away from the chip towards the "TDO" pin.



Repeat and reuse

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 abd hello

Hierarchy Files Design Units Tasks Flow: Compilation

Task Analysis & Synthesis Fitter (Place & Route) Assembler (Generate programming files) TimeQuest Timing Analysis EDA Netlist Writer Program Device (Open Programmer)

..//hello.v*

```
19 |     4'h2: ssOut = 7'b1000111;
20 |     4'h3: ssOut = 7'b1000111;
21 |     4'h4: ssOut = 7'b1000000;
22 |     4'h5: ssOut = 7'b1111111;
23 |     4'h6: ssOut = 7'b1111111;
24 |     4'h7: ssOut = 7'b1111111;
25 |     4'h8: ssOut = 7'b1111111;
26 |     default: ssOut = 7'b00000000;
27 |   endcase
28 |   always @(posedge LEDstatus) begin
29 |     nIn2 <= nIn2 + 1;
30 |     case (nIn2)
31 |       4'h0: ssOut = 7'b1111111;
32 |       4'h1: ssOut = 7'b0001001;
33 |       4'h2: ssOut = 7'b0000110;
34 |       4'h3: ssOut = 7'b1000111;
35 |       4'h4: ssOut = 7'b1000111;
36 |       4'h5: ssOut = 7'b1000000;
37 |       4'h6: ssOut = 7'b1111111;
38 |       4'h7: ssOut = 7'b1111111;
39 |       4'h8: ssOut = 7'b1111111;
40 |       default: ssOut = 7'b00000000;
41 |     endcase
42 |   always @(posedge LEDstatus) begin
43 |     nIn3 <= nIn3 + 1;
44 |     case (nIn3)
45 |       4'h0: ssOut = 7'b1111111;
```

All <> <<Search>>

Type	ID	Message
Info	204019	Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
Info		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Info	293000	Quartus II Full Compilation was successful. 0 errors, 36 warnings

Messages System (74) Processing (122)

100% 00:01:42

Remember to get the pins

The image consists of three main parts:

- Top Left:** A close-up photograph of a person's hand holding a black pin header with several pins visible.
- Middle Left:** A screenshot of the "Pin Planner - C:/altera/output_files/hello - hello" window. It shows a "Top View - Wire Bond" diagram for a Cyclone IV GX - EP4CGX150DF31C8 device. The diagram is a grid of pins labeled A through Z and AA through ZZ. A legend at the bottom identifies symbols for Power, Ground, Input, Output, and Tri-state. Below the diagram is a table of pin assignments:

Node Name	Direction	Location	I/O Bank	VREF Group	PIN
out LED	Output				PIN
in clk	Input	PIN_A16	4	B4_N2	PIN
out ssOut[6]	Output	PIN_F14	8	B8_N0	PIN
out ssOut[5]	Output	PIN_D16	8	B8_N0	PIN
out ssOut[4]	Output	PIN_F16	8	B8_N0	PIN
out ssOut[3]	Output	PIN_F11	8	B8_N1	PIN
out ssOut[2]	Output	PIN_G11	R	RR_N1	PIN

- Right:** A screenshot of the "DE2i-150_FPGA_System_manual.pdf - Adobe Reader" window. It displays Figure 3-11: "Connections between the 7-segment display HEX0 and HEX1". A callout box points to a lightbulb icon with the text: "Click on Comment and Share to create, mark-up and send PDF files." Below the figure is Table 3-5: "Pin Assignments for 7-segment Displays".

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX0[0]	PIN_E15	Seven Segment Digit 0[0]	2.5V
HEX0[1]	PIN_E12	Seven Segment Digit 0[1]	2.5V
HEX0[2]	PIN_G11	Seven Segment Digit 0[2]	2.5V
HEX0[3]	PIN_F11	Seven Segment Digit 0[3]	2.5V
HEX0[4]	PIN_F16	Seven Segment Digit 0[4]	2.5V
HEX0[5]	PIN_D16	Seven Segment Digit 0[5]	2.5V
HEX0[6]	PIN_F14	Seven Segment Digit 0[6]	2.5V
HEX1[0]	PIN_G14	Seven Segment Digit 1[0]	2.5V
HEX1[1]	PIN_B13	Seven Segment Digit 1[1]	2.5V
HEX1[2]	PIN_G13	Seven Segment Digit 1[2]	2.5V
HEX1[3]	PIN_F12	Seven Segment Digit 1[3]	2.5V
HEX1[4]	PIN_G12	Seven Segment Digit 1[4]	2.5V
HEX1[5]	PIN_J9	Seven Segment Digit 1[5]	2.5V
HEX1[6]	PIN_G10	Seven Segment Digit 1[6]	2.5V
HEX2[0]	PIN_G8	Seven Segment Digit 2[0]	2.5V
HEX2[1]	PIN_G7	Seven Segment Digit 2[1]	2.5V
HEX2[2]	PIN_F7	Seven Segment Digit 2[2]	2.5V
HEX2[3]	PIN_AG30	Seven Segment Digit 2[3]	2.5V
HEX2[4]	PIN_F6	Seven Segment Digit 2[4]	2.5V
HEX2[5]	PIN_F4	Seven Segment Digit 2[5]	2.5V
HEX2[6]	PIN_F10	Seven Segment Digit 2[6]	2.5V
HEX3[0]	PIN_D10	Seven Segment Digit 3[0]	2.5V
HEX3[1]	PIN_D7	Seven Segment Digit 3[1]	2.5V
HEX3[2]	PIN_E6	Seven Segment Digit 3[2]	2.5V
HEX3[3]	PIN_E4	Seven Segment Digit 3[3]	2.5V
HEX3[4]	PIN_E3	Seven Segment Digit 3[4]	2.5V
HEX3[5]	PIN_D5	Seven Segment Digit 3[5]	2.5V
HEX3[6]	PIN_D4	Seven Segment Digit 3[6]	2.5V
HEX4[0]	PIN_A14	Seven Segment Digit 4[0]	2.5V
HEX4[1]	PIN_A13	Seven Segment Digit 4[1]	2.5V

One does not simply

Compile

"ERRORS"

Oh no!



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help Search altera.com

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 hello

Tasks Flow: Compilation Customize...

Task Analysis & Synthesis Fitter (Place & Route) Assembler (Generate programming files) TimeQuest Timing Analysis EDA Netlist Writer Program Device (Open Programmer)

..//hello.v Compilation Report - hello

```
46      4'h1: ssOut = 7'b1111111;
47      4'h2: ssOut = 7'b0001001;
48      4'h3: ssOut = 7'b0000110;
49      4'h4: ssOut = 7'b1000111;
50      4'h5: ssOut = 7'b1000111;
51      4'h6: ssOut = 7'b1000000;
52      4'h7: ssOut = 7'b1111111;
53      4'h8: ssOut = 7'b1111111;
54      default: ssOut = 7'b00000000;
55      endcase
56  always @ (posedge LEDstatus) begin
57    nIn4 <= nIn4 + 1;
58    case (nIn4)
59      4'h0: ssOut = 7'b1111111;
60      4'h1: ssOut = 7'b1111111;
61      4'h2: ssOut = 7'b1111111;
62      4'h3: ssOut = 7'b0001001;
63      4'h4: ssOut = 7'b0000110;
64      4'h5: ssOut = 7'b1000111;
65      4'h6: ssOut = 7'b1000111;
66      4'h7: ssOut = 7'b1000000;
67      4'h8: ssOut = 7'b1111111;
68      default: ssOut = 7'b00000000;
69      endcase
70    end
71  endmodule
```

All <<Search>>

Type	ID	Message
10170 Verilog HDL syntax error at hello.v(28)		near text "always"; expecting "end"
10170 Verilog HDL syntax error at hello.v(42)		near text "always"; expecting "end"
10170 Verilog HDL syntax error at hello.v(56)		near text "always"; expecting "end"
10170 Verilog HDL syntax error at hello.v(71)		near text "endmodule"; expecting "end"

Messages System (34) Processing (6)

2% 00:00:02



Remember to change SsOuts

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 abd hello

Hierarchy Files Design Units Tasks Flow: Compilation

Task Analysis & Synthesis Filter (Place & Route) Assembler (Generate programming files) TimeQuest Timing Analysis EDA Netlist Writer Program Device (Open Programmer)

..../hello.v* Compilation Report - hello

```
16    case (nIn)
17        4'h0: ssOut = 7'b0001001;
18        4'h1: ssOut = 7'b0000110;
19        4'h2: ssOut = 7'b1000111;
20        4'h3: ssOut = 7'b1000111;
21        4'h4: ssOut = 7'b1000000;
22        4'h5: ssOut = 7'b1111111;
23        4'h6: ssOut = 7'b1111111;
24        4'h7: ssOut = 7'b1111111;
25        4'h8: ssOut = 7'b1111111;
26    default: ssOut = 7'b00000000;
27 endcase
28
29 always @(posedge LEDstatus) begin
30     nIn2 <= nIn2 + 1;
31     case (nIn2)
32         4'h0: ssOut2 = 7'b1111111;
33         4'h1: ssOut2 = 7'b0001001;
34         4'h2: ssOut2 = 7'b0000110;
35         4'h3: ssOut2 = 7'b1000111;
36         4'h4: ssOut2 = 7'b1000111;
37         4'h5: ssOut2 = 7'b1000000;
38         4'h6: ssOut2 = 7'b1111111;
39         4'h7: ssOut2 = 7'b1111111;
40         4'h8: ssOut2 = 7'b1111111;
41     default: ssOut2 = 7'b00000000;
42 endcase
```

All <> <<Search>>

Type ID Message

- 10028 Can't resolve multiple constant drivers for net "ssOut[6]" at hello.v(29)
- 10029 Constant driver at hello.v(14)
- 10028 Can't resolve multiple constant drivers for net "ssOut[5]" at hello.v(29)
- 10028 Can't resolve multiple constant drivers for net "ssOut[4]" at hello.v(29)

Messages System (34) Processing (11) 9% 00:00:02

A screenshot of the Quartus II software interface. The main window shows a VHDL code editor with the file 'hello.v' open. The code contains two cases: one for 'nIn' and one for 'nIn2', both defining 'ssOut' and 'ssOut2' respectively. The code uses binary constants for the assignments. Below the code editor is a 'Tasks' panel showing a list of compilation steps: Analysis & Synthesis, Filter (Place & Route), Assembler (Generate programming files), TimeQuest Timing Analysis, EDA Netlist Writer, and Program Device (Open Programmer). The 'Analysis & Synthesis' task is currently selected. At the bottom of the interface is a 'Messages' window displaying several error messages related to multiple constant drivers for specific net names like 'ssOut[6]' and 'ssOut[5]'. The status bar at the bottom right indicates the system is at 9% completion and took 00:00:02.

One more thing!!!



Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Processing Tools Window Help Search altera.com

Project Navigator Entity Cyclone IV GX: EP4CGX150DF31C8 abd hello

Hierarchy Files Design Units Tasks Flow: Compilation Customize... Task Analysis & Synthesis Fitter (Place & Route) Assembler (Generate programming files) TimeQuest Timing Analysis EDA Netlist Writer Program Device (Open Programmer)

..../hello.v

```
16    case (nIn)
17        4'h0: ssOut = 7'b0001001;
18        4'h1: ssOut = 7'b0000110;
19        4'h2: ssOut = 7'b1000111;
20        4'h3: ssOut = 7'b1000111;
21        4'h4: ssOut = 7'b1000000;
22        4'h5: ssOut = 7'b1111111;
23        4'h6: ssOut = 7'b1111111;
24        4'h7: ssOut = 7'b1111111;
25        4'h8: ssOut = 7'b1111111;
26        default: ssOut = 7'b00000000;
27    endcase
28
29    always @(posedge LEDstatus) begin
30        nIn2 <= nIn2 + 1;
31        case (nIn2)
32            4'h0: ssOut2 = 7'b1111111;
33            4'h1: ssOut2 = 7'b0001001;
34            4'h2: ssOut2 = 7'b0000110;
35            4'h3: ssOut2 = 7'b1000111;
36            4'h4: ssOut2 = 7'b1000111;
37            4'h5: ssOut2 = 7'b1000000;
38            4'h6: ssOut2 = 7'b1111111;
39            4'h7: ssOut2 = 7'b1111111;
40            4'h8: ssOut2 = 7'b1111111;
41            default: ssOut2 = 7'b00000000;
42        endcase

```

Programmer - C:/altera/output_files/hello - hello [output_files/hel...]

File Edit View Processing Tools Window Help Search altera.com

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

File Device Checksum Usercode Pro Co

output_files/hello.sof EP4CGX150DF31 0072A9D6 FFFFFFFF

TDI

All <> <<Search>>

Type ID Message

204019 Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool

Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 17 warnings

Messages

System (74) Processing (124)

100% 00:00:57

Congratulations!!!



WHO'S AWESOME?
YOU'RE AWESOME



Warning for the Next Subject (Schematics)



If you are comfortable with creating circuits
then this method will be easy and probably
more favorable for you. If not, don't torture
yourself.....

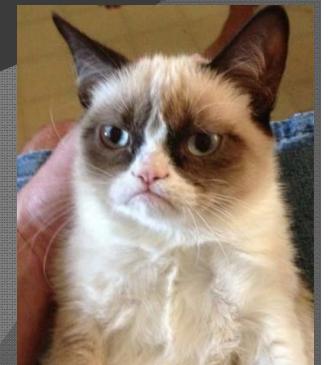
.....

.....

.....

.....

Seriously.....don't



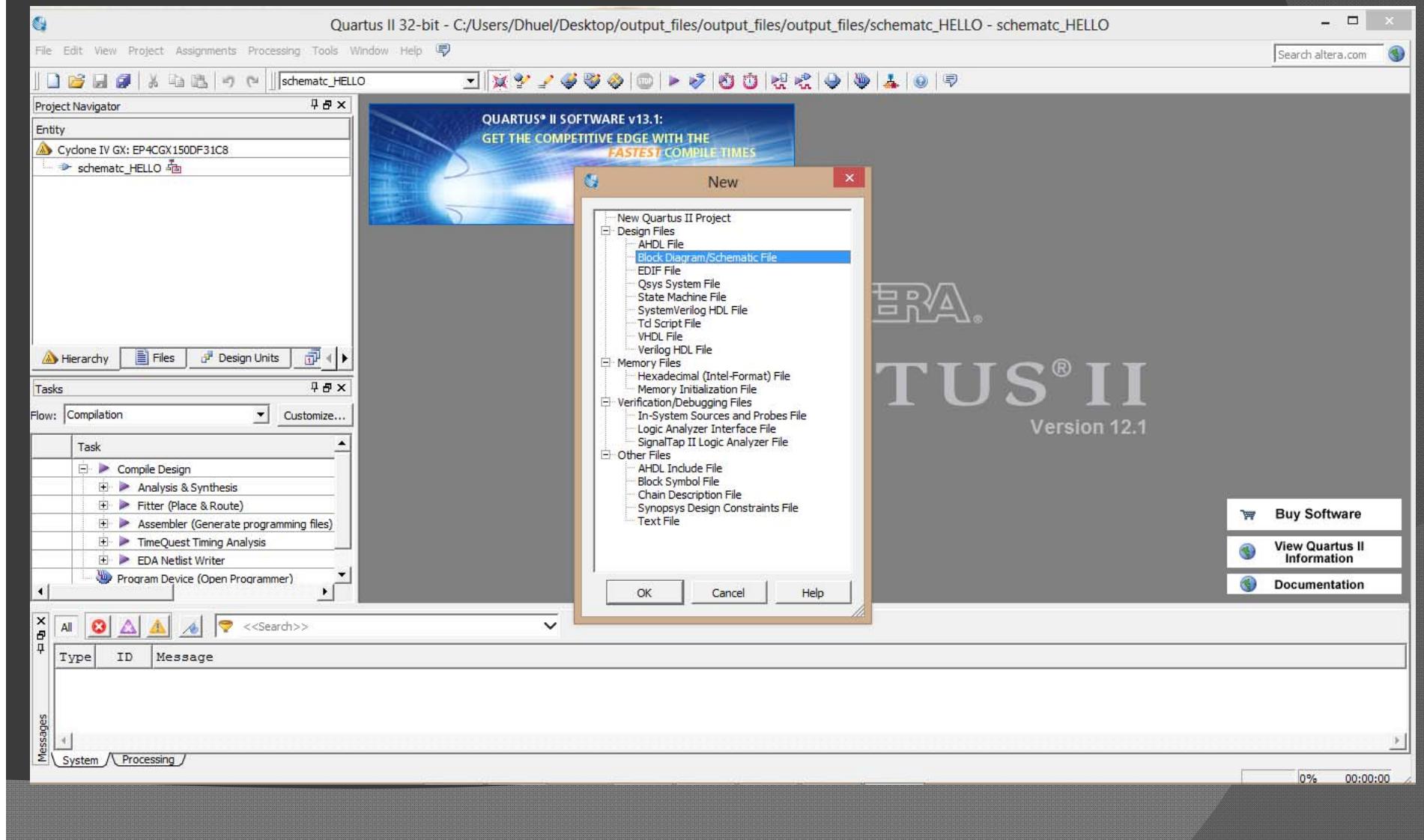


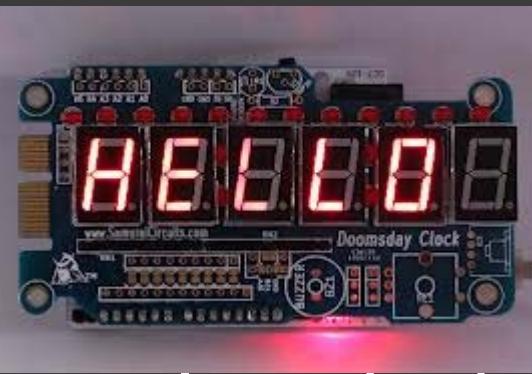
Follow previous setup instructions

The screenshot shows the Quartus II 32-bit software interface. A red box highlights the "New Project Wizard" dialog box, which is titled "Directory, Name, Top-Level Entity [page 1 of 5]". The dialog contains three input fields: "What is the working directory for this project?" (C:\Users\dhuel\Desktop), "What is the name of this project?" (schematic_HELLO), and "What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file." (schematic_HELLO). Below these fields is a "Use Existing Project Settings..." button. At the bottom of the dialog are buttons for "< Back", "Next >", "Finish", "Cancel", and "Help". The main workspace of the software shows the "Project Navigator" with a "Compilation Hierarchy" tree. The "Tasks" pane on the left is expanded to show the "Task" tree, with "Compile Design" selected. The "Messages" pane at the bottom shows a table with columns "Type", "ID", and "Message". The status bar at the bottom right indicates "0%" and "00:00:00".



Choose block diagram/Schematic file



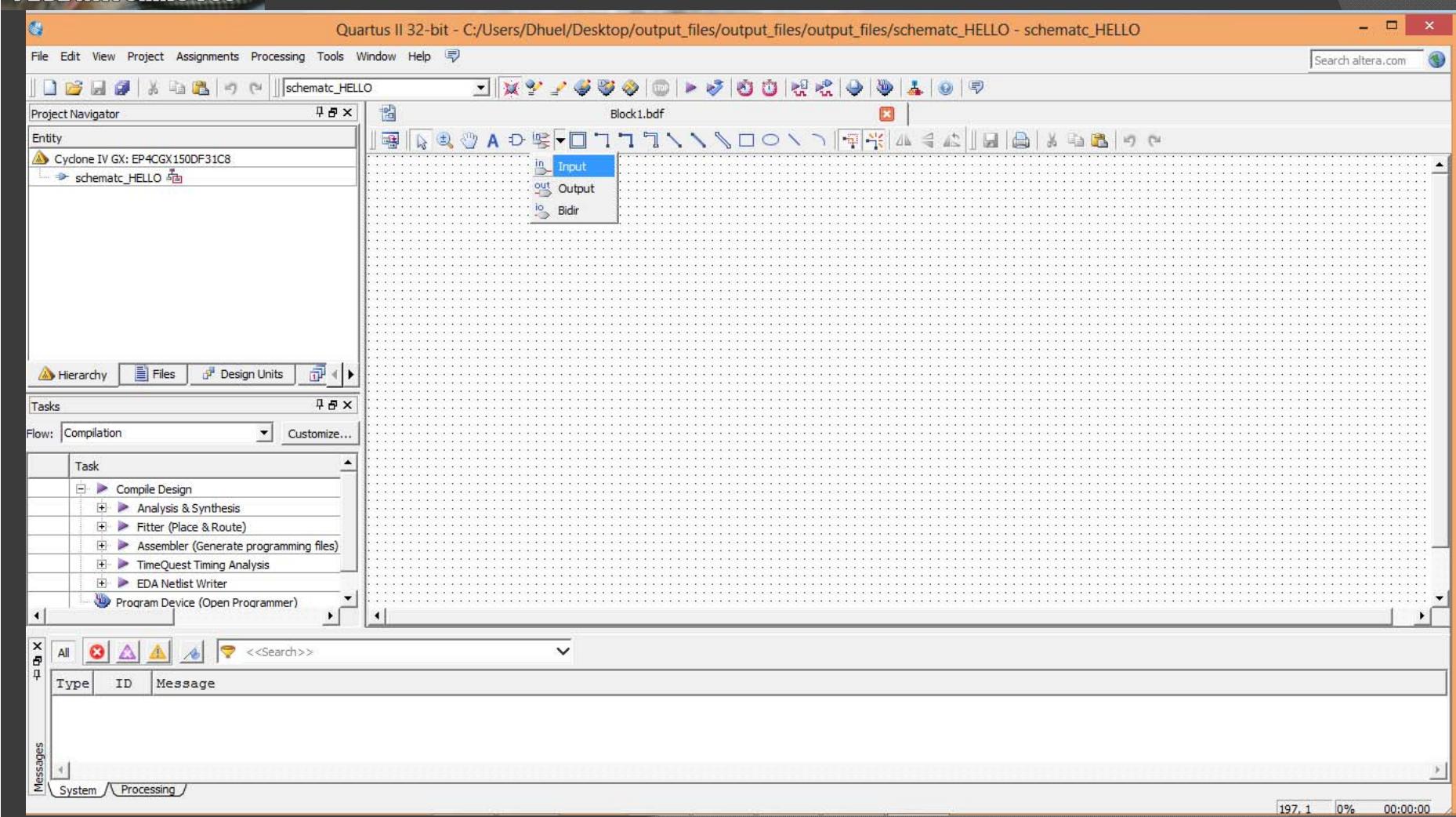


Note

- In order to continue, it would be best if you have already sketched or thought about the circuit that you will need to create.
- For demonstration purposes, I will show how to display a simple HELLO on the 7 segment display.

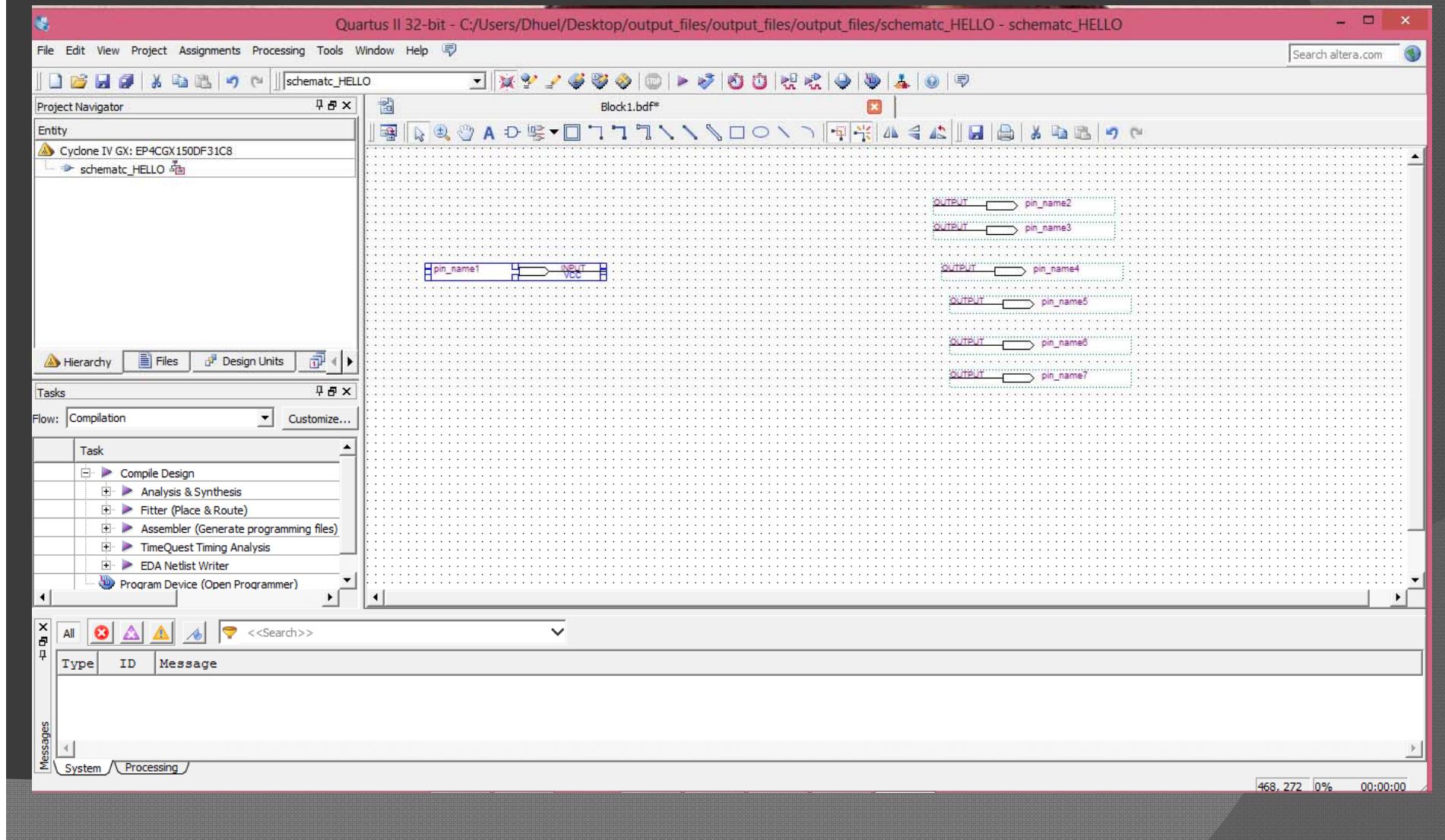


Choose inputs and outputs





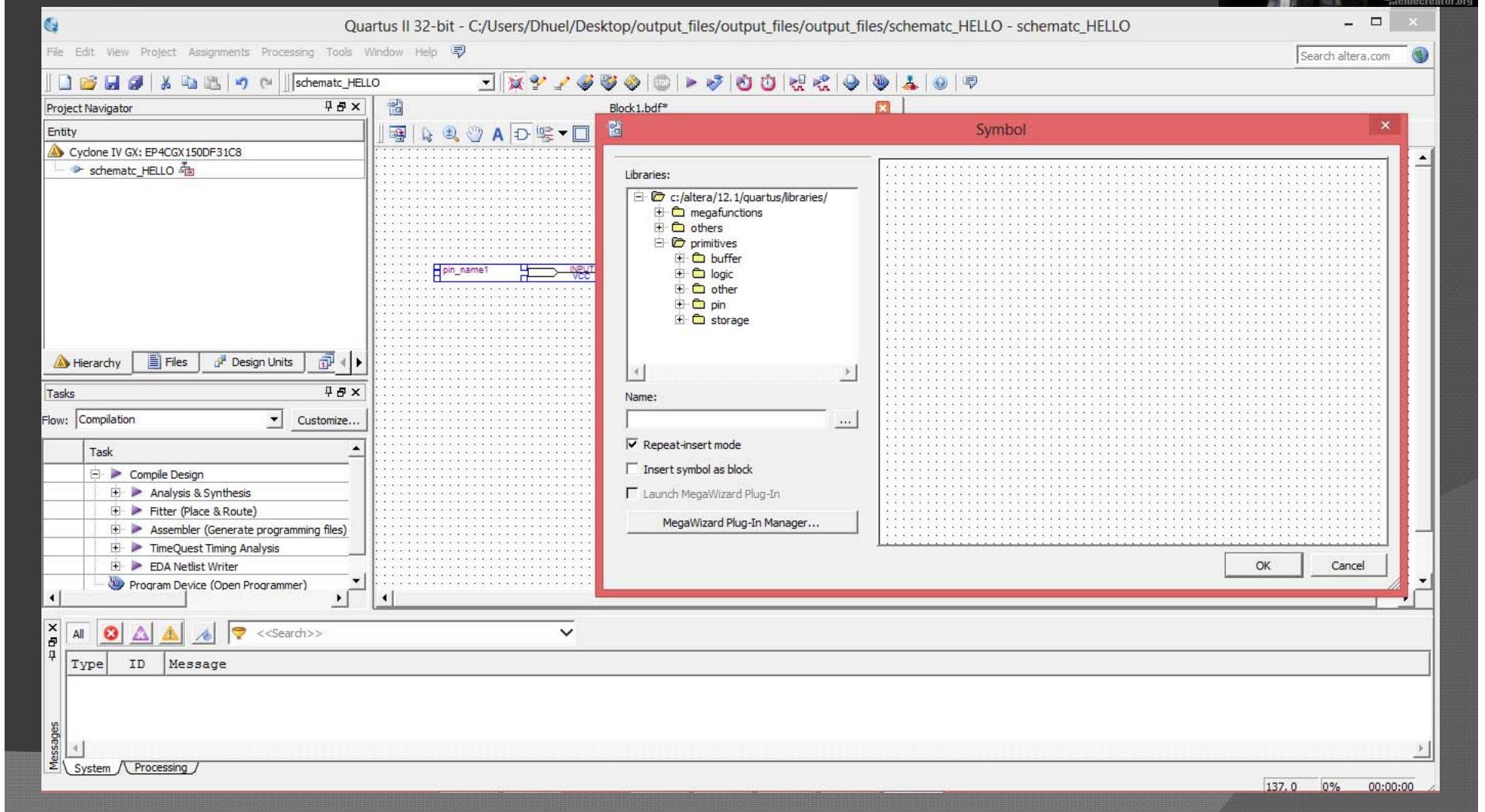
Place all the pins you will



Brace Yourselves



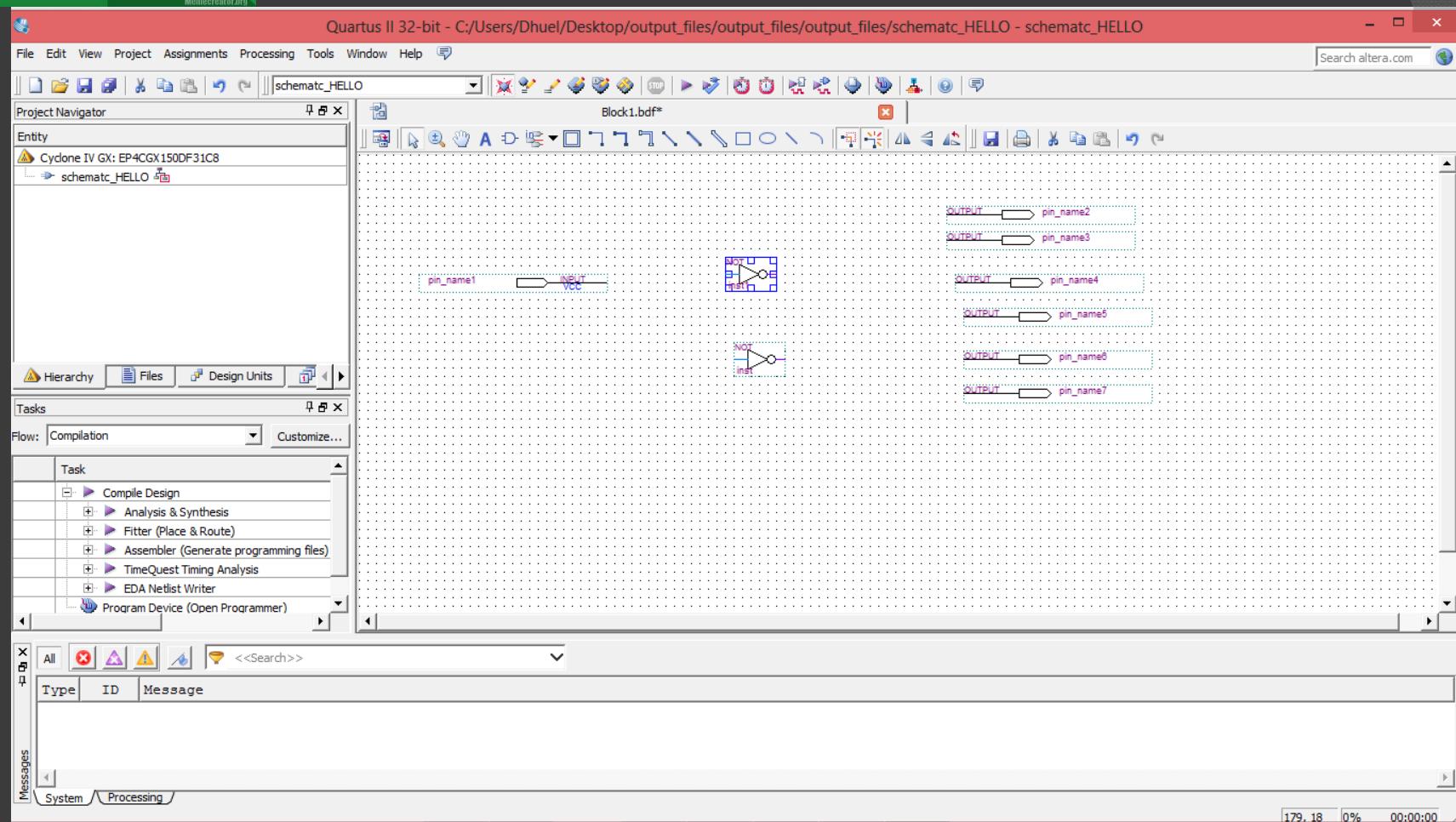
If you require other gates/switches/latches/ etc.

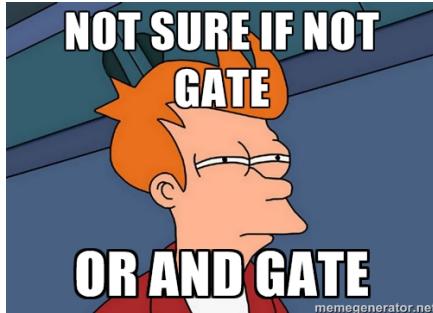


You NOT get A?



Place two NOT gates





Connect wires using wire diagrams

The screenshot shows the Quartus II 32-bit software interface. The title bar reads "Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/output_files/schematic_HELLO - schematic_HELLO". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, Help, and a search bar for "altera.com".

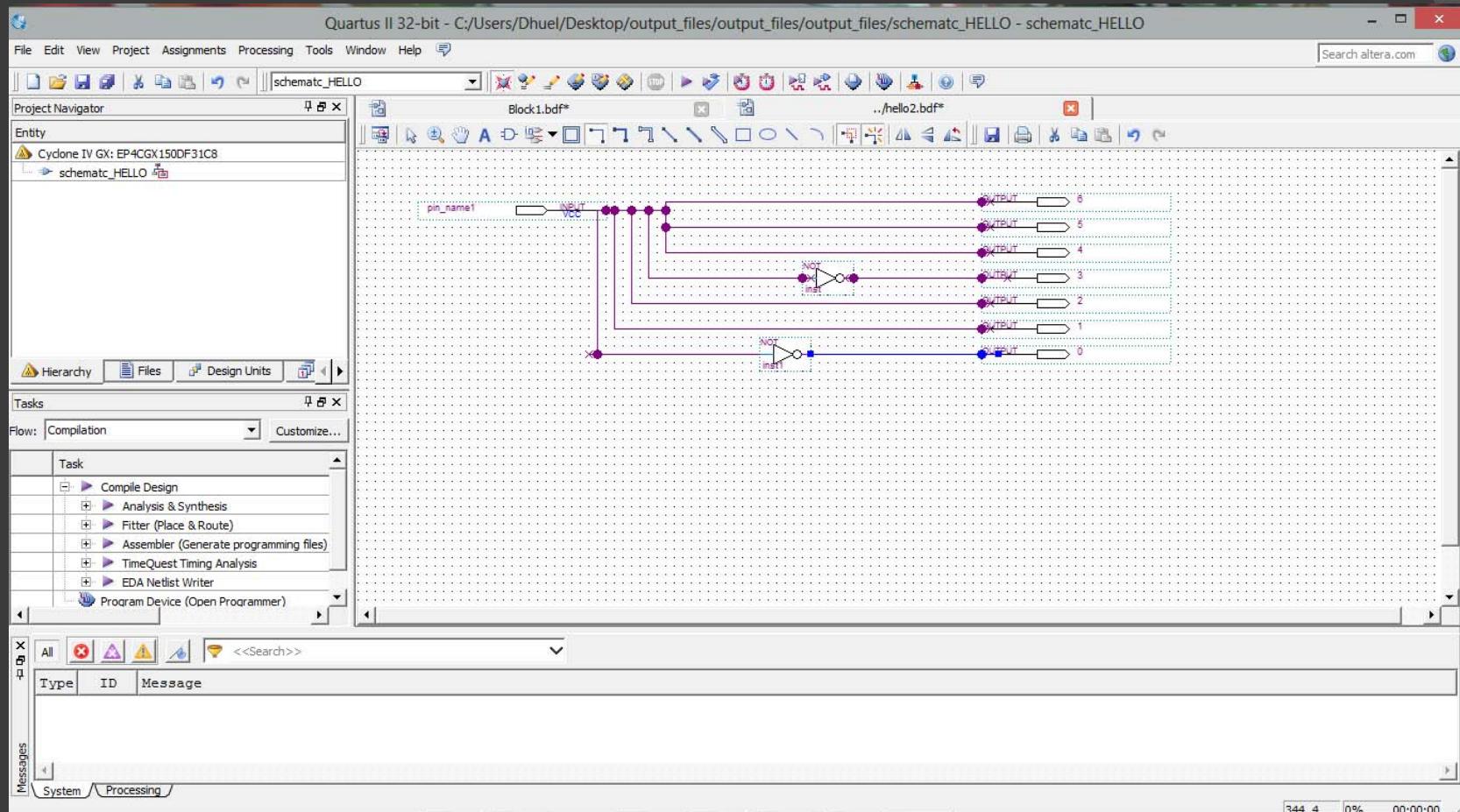
The main workspace displays a wire diagram titled "Block1.bdf*". The diagram shows a complex network of wires connecting various logic gates and pins. A specific node, labeled "pin_name1", is highlighted with a red box and connected to a "VCC" power rail. Other nodes include "pin_name2", "pin_name3", "pin_name4", "pin_name5", "pin_name6", and "pin_name7". Logic gates labeled "NOT inst1" and "NOT inst2" are present in the circuit.

The left side of the interface features the "Project Navigator" and "Hierarchy" panes. The "Project Navigator" pane shows the project structure with "Entity" and "schematic_HELLO" listed. The "Hierarchy" pane shows the design units. The bottom left contains the "Tasks" pane with a "Compilation" flow and a list of tasks: Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming files), TimeQuest Timing Analysis, EDA Netlist Writer, and Program Device (Open Programmer).

The bottom right corner of the interface shows status information: 223, 0, 0%, and 00:00:00.

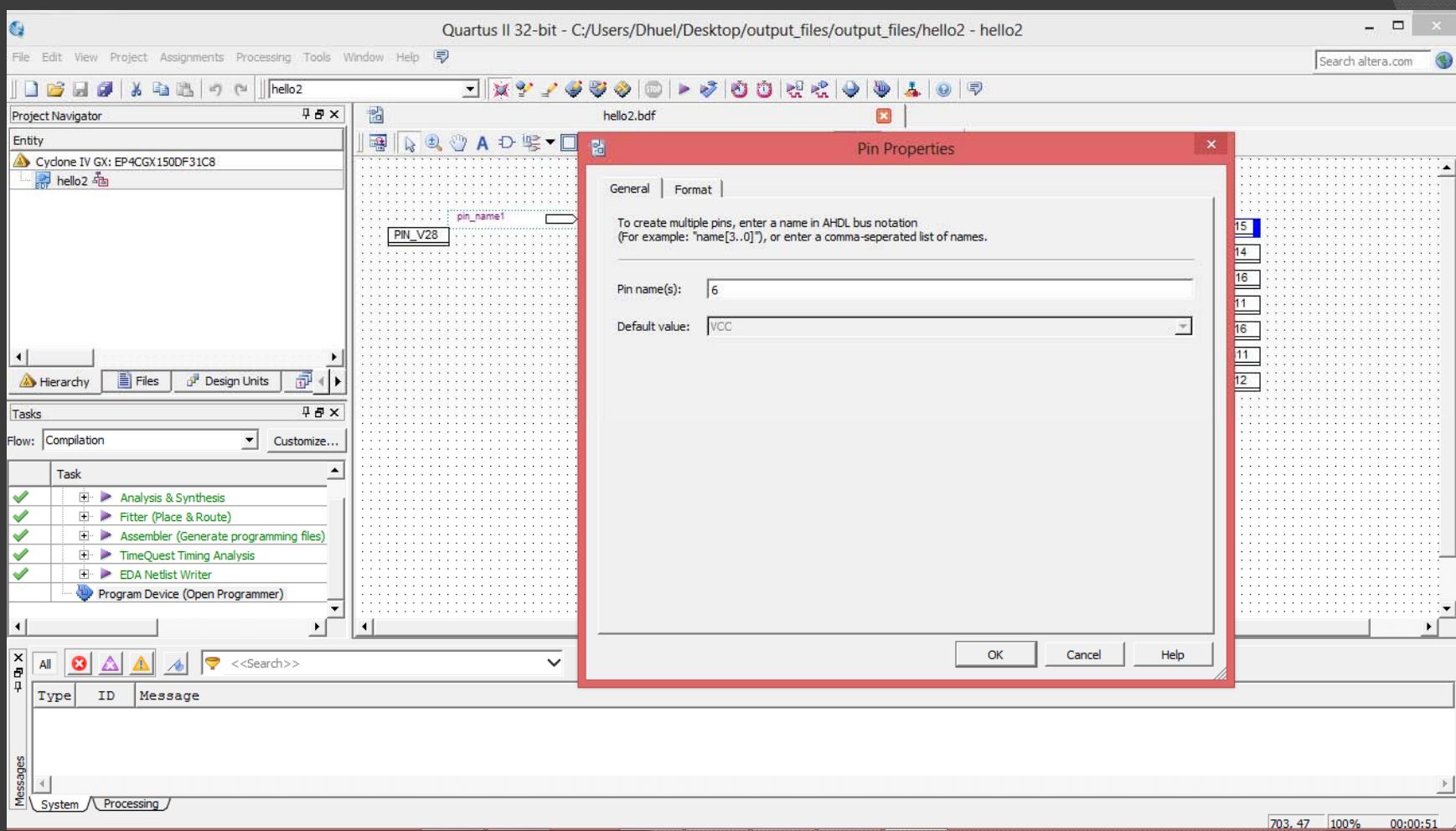
A NEAT DESK IS
THE SIGN OF A
SICK MIND

Neat work also helps with understanding





Double click items to rename



I REMEMBERED

TO COMPILE



Don't forget to compile!

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/output_files/schematic_HELLO - schematic_HELLO

File Edit View Project Assignments Processing Tools Window Help

Project Navigator .. ./schematic_HELLO.bdf .. ./hello2.bdf Compilation Report - schematic_HELLO

Entity Cydone IV GX: EP4CGX150DF31C8 schematic_HELLO

Hierarchy Files Design Units

Tasks Flow: Compilation

Task 64% Analysis & Synthesis 71% Fitter (Place & Route) 0% Assembler (Generate programming files) 0% TimeQuest Timing Analysis 0% EDA Netlist Writer

Program Device (Open Programmer)

All <<Search>>

Type ID Message

170137 Fitter placement was successful
170192 Fitter placement operations ending: elapsed time is 00:00:01
170193 Fitter routing operations beginning

System Processing (48)

377, 17 34% 00:00:18

The screenshot shows the Quartus II 32-bit software interface. The main window displays a schematic diagram for a device named 'schematic_HELLO' on a 'Cydone IV GX: EP4CGX150DF31C8' device. The schematic includes various logic gates like NOT and AND, and connections to pins labeled 'pin_name'. On the left, the 'Project Navigator' shows the project structure with files like 'schematic_HELLO.bdf' and 'hello2.bdf'. The 'Tasks' panel shows the compilation progress with steps like 'Analysis & Synthesis' (71% complete), 'Fitter (Place & Route)' (64% complete), and 'Assembler (Generate programming files)' (0% complete). The 'Messages' panel at the bottom shows log entries related to the fitter placement and routing process. The status bar at the bottom right indicates the system has 377, 17 components, 34% completion, and a total time of 00:00:18.



Assign Pins

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/hello2 - hello2

File Edit View Project Assignments Processing Tools Window Help

Device... Ctrl+Shift+E
Settings... Ctrl+Shift+N
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D

Project Navigator Entity Cydone IV GX: EP4CGX hello2

Tasks Flow: Compilation Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

Message Type ID Message

System Processing

Edits pin assignments

100% 00:00:51

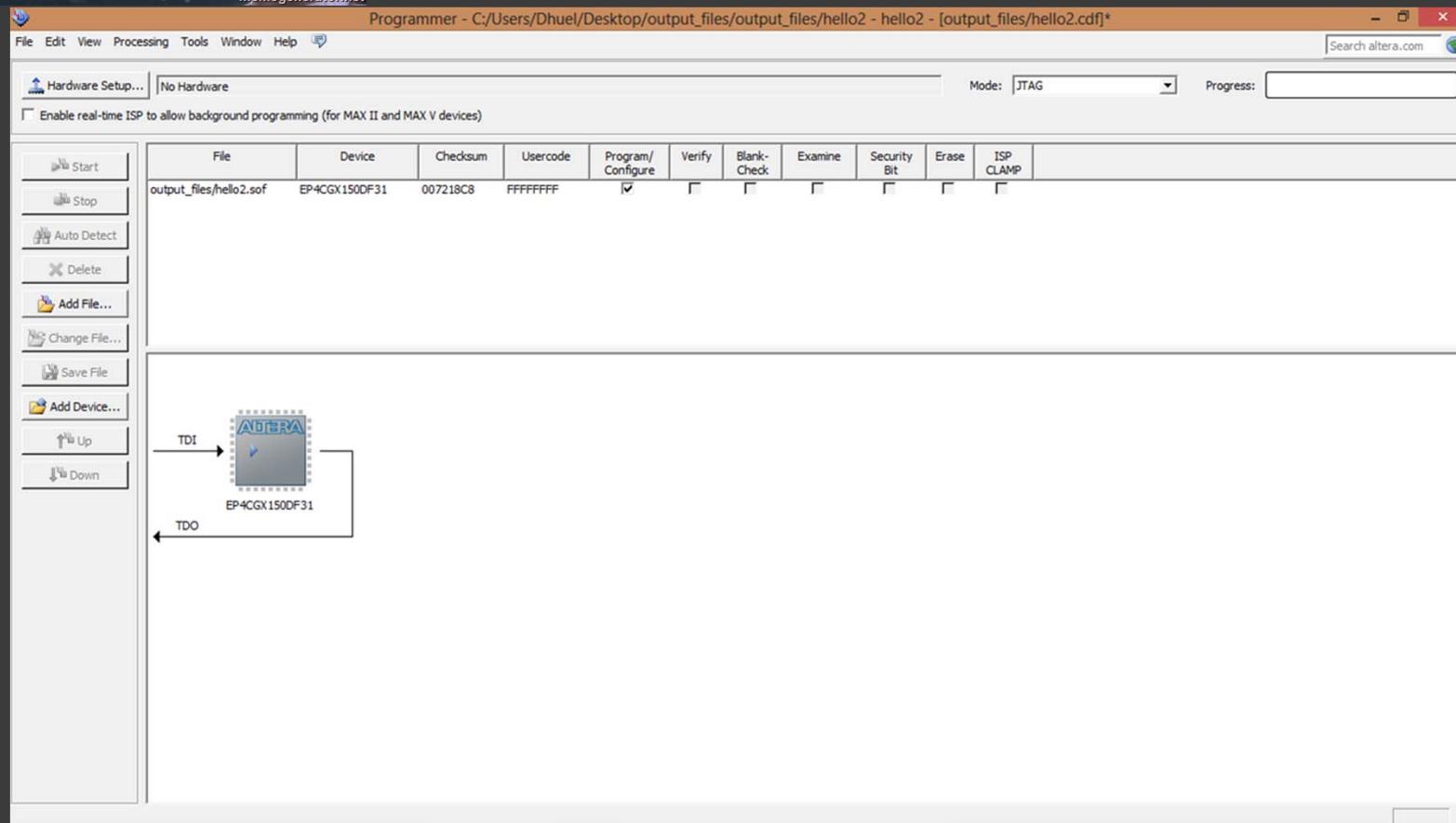
The screenshot shows the Quartus II software interface for a project named "hello2". The main window displays a logic diagram with several NOT gates and their connections to pins. The "Pin Planner" menu option is highlighted. The "Messages" panel at the bottom shows the status "Edits pin assignments". The status bar at the bottom right indicates "100% 00:00:51".

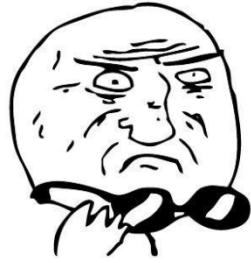
SENT IT TO MY
BOARD...

ONCE.....

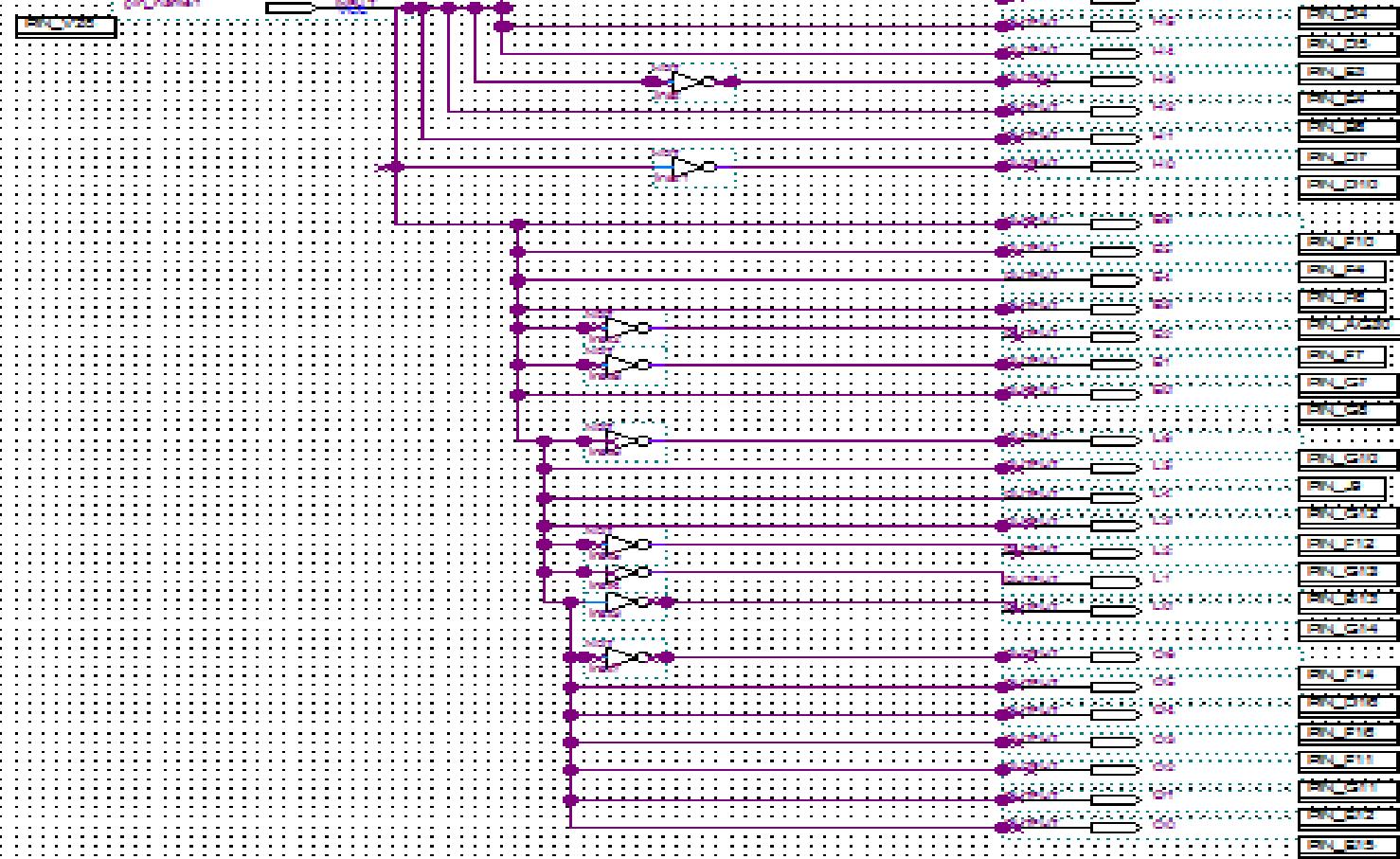
memegenerator.net

Send to board to see if it all works well



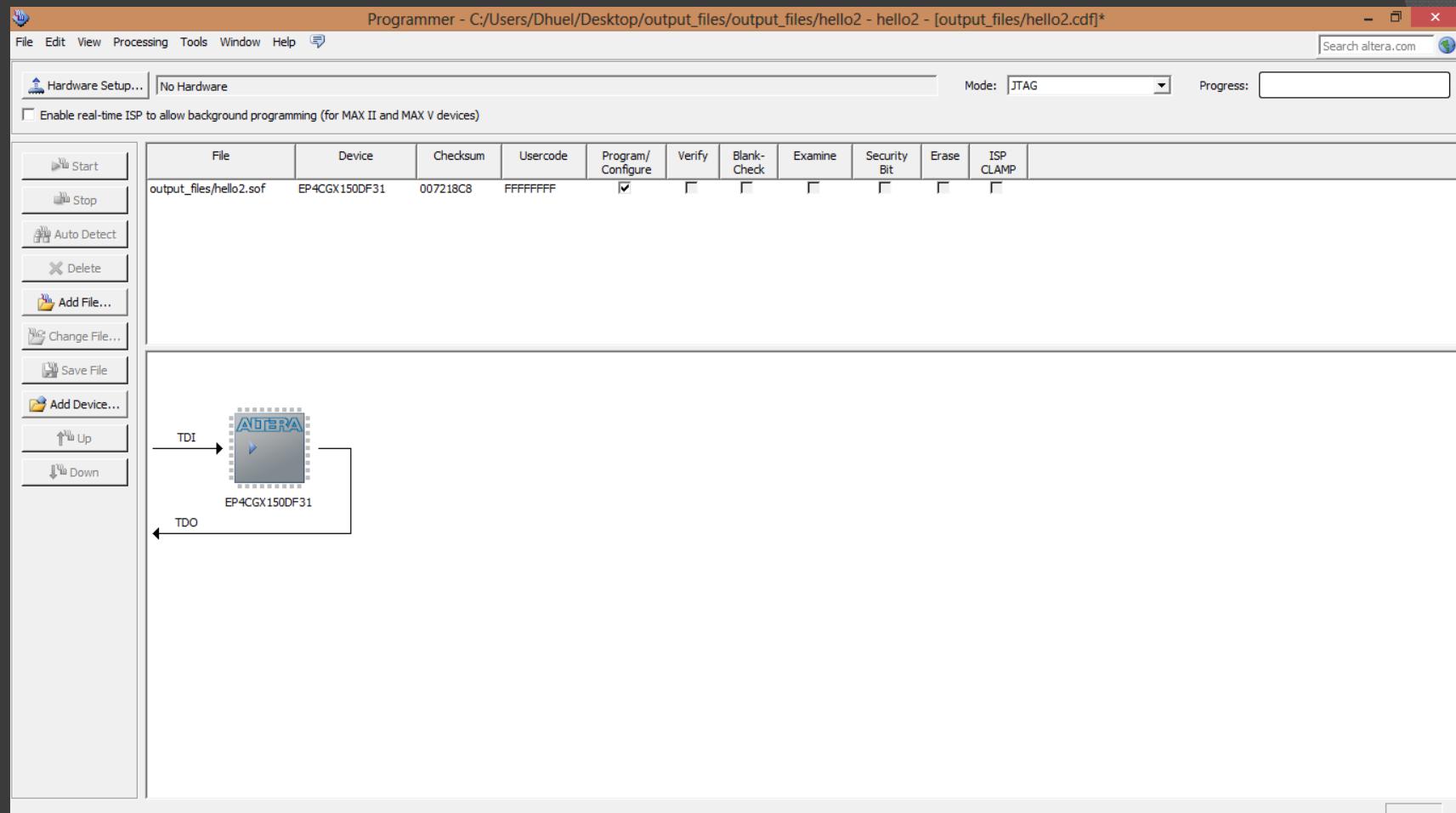


If it works, repeat and reuse





Then we send it all to the board to see the final form



Congratulations, you wrote
HELLO using Verilog and
schematic diagrams.



In case you missed it

```
○ module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
○   output LED;
○   input clk;
○   reg LEDstatus;
○   reg [23:0] count;
○   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
○   reg [2:0] nIn, nIn2, nIn3, nIn4;
○   assign LED = LEDstatus;

○   always @(posedge clk) begin
○     LEDstatus <= count[23];
○     count  <= count + 1;
○   end
○   always @(posedge LEDstatus) begin
○     nIn <= nIn + 1;
○     case (nIn)
○       4'h0: ssOut = 7'b0001001;
○       4'h1: ssOut = 7'b0000110;
○       4'h2: ssOut = 7'b1000111;
○       4'h3: ssOut = 7'b1000111;
○       4'h4: ssOut = 7'b1000000;
○       4'h5: ssOut = 7'b1111111;
○       4'h6: ssOut = 7'b1111111;
○       4'h7: ssOut = 7'b1111111;
○       4'h8: ssOut = 7'b1111111;
○       default: ssOut = 7'b00000000;
○     endcase
○   end
```

```
○ always @(posedge LEDstatus) begin
○     nIn2 <= nIn2 + 1;
○     case (nIn2)
○         4'h0: ssOut2 = 7'b1111111;
○         4'h1: ssOut2 = 7'b00001001;
○         4'h2: ssOut2 = 7'b00000110;
○             4'h3: ssOut2 = 7'b1000111;
○             4'h4: ssOut2 = 7'b1000111;
○             4'h5: ssOut2 = 7'b1000000;
○             4'h6: ssOut2 = 7'b1111111;
○             4'h7: ssOut2 = 7'b1111111;
○             4'h8: ssOut2 = 7'b1111111;
○             default: ssOut = 7'b00000000;
○             endcase
○     end
```

```
○ always @(posedge LEDstatus) begin
○     nIn3 <= nIn3 + 1;
○     case (nIn3)
○         4'h0: ssOut3 = 7'b1111111;
○         4'h1: ssOut3 = 7'b1111111;
○         4'h2: ssOut3 = 7'b00001001;
○         4'h3: ssOut3 = 7'b00000110;
○         4'h4: ssOut3 = 7'b1000111;
○         4'h5: ssOut3 = 7'b1000111;
○         4'h6: ssOut3 = 7'b1000000;
○         4'h7: ssOut3 = 7'b1111111;
○         4'h8: ssOut3 = 7'b1111111;
○         default: ssOut3 = 7'b00000000;
○     endcase
○ end
```

```
○ always @(posedge LEDstatus) begin
○     nIn4 <= nIn4 + 1;
○     case (nIn4)
○         4'h0: ssOut4 = 7'b1111111;
○             4'h1: ssOut4 = 7'b1111111;
○             4'h2: ssOut4 = 7'b1111111;
○             4'h3: ssOut4 = 7'b00001001;
○             4'h4: ssOut4 = 7'b00000110;
○                 4'h5: ssOut4 = 7'b1000111;
○                 4'h6: ssOut4 = 7'b1000111;
○                 4'h7: ssOut4 = 7'b1000000;
○                 4'h8: ssOut4 = 7'b1111111;
○             default: ssOut4 = 7'b00000000;
○         endcase
○     end
○ endmodule
```

