Dhuel Fisher

EECE494 Computer Bus and SoC Interfacing
Electrical and Computer Engineering
Howard University

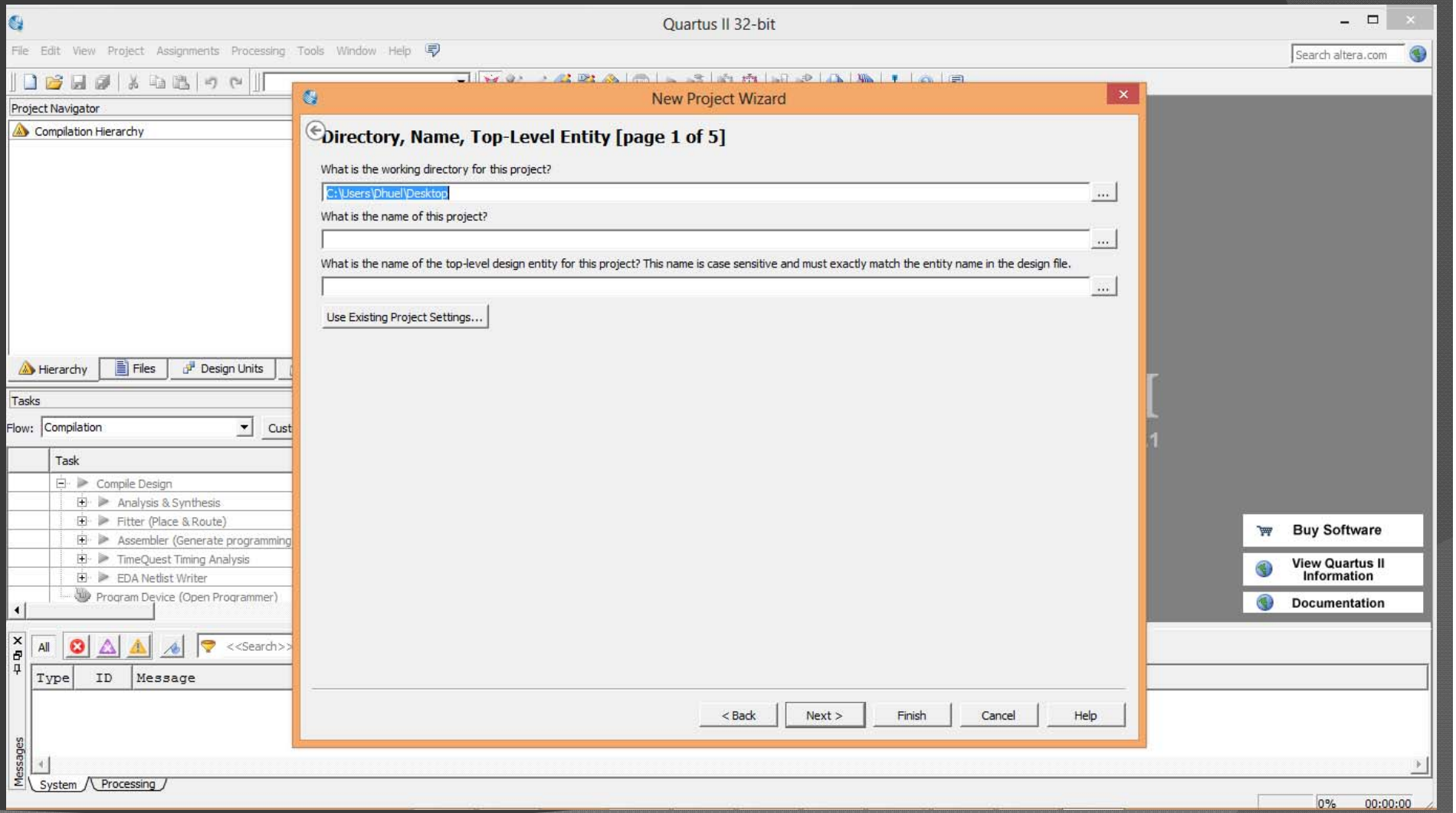
Instructor: Dr. Charles Kim

Steps

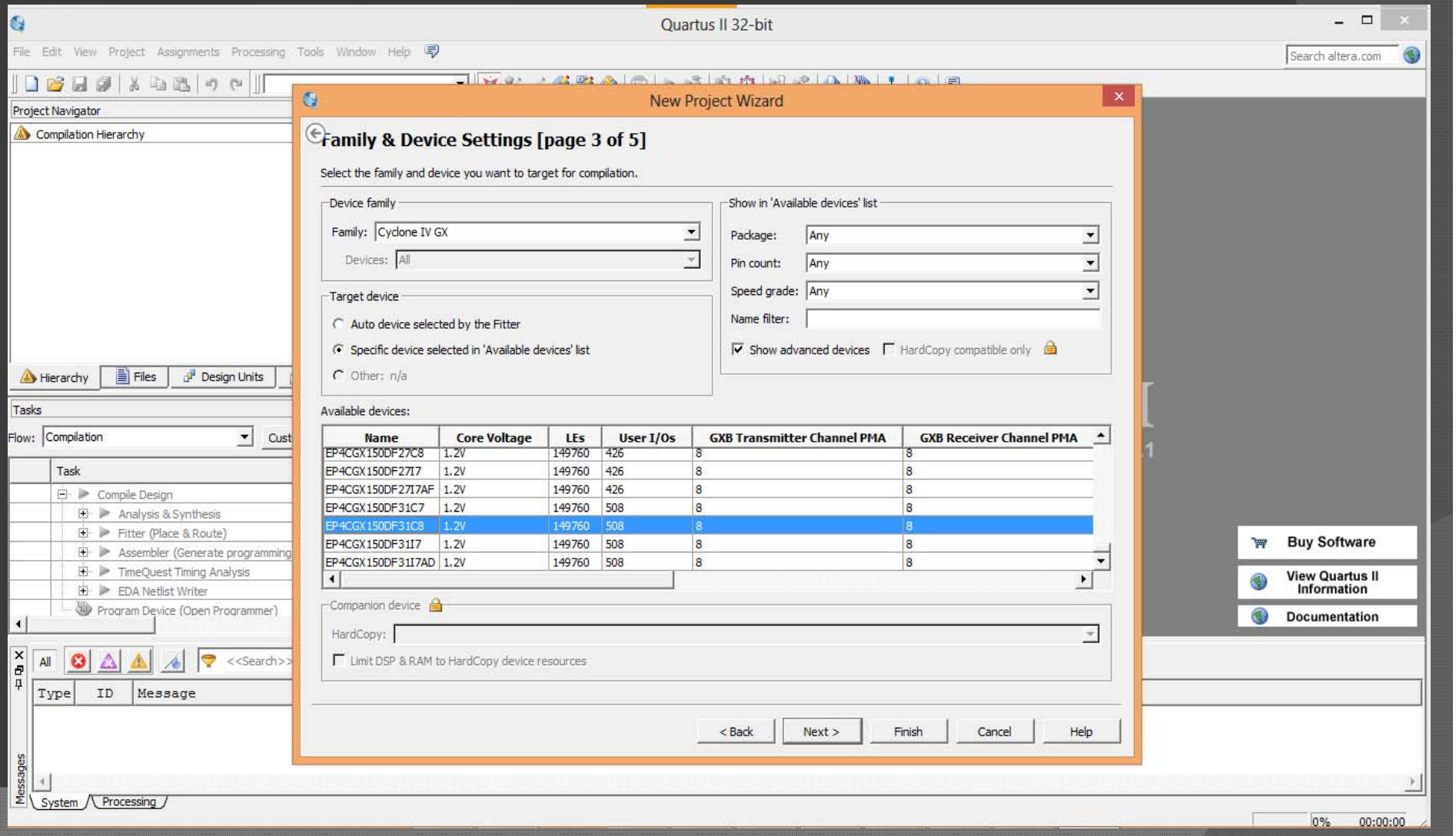
1. Aim: To create display on 7 segment display
2. Tools : What will I need
3. Research
4. Code

Starting Quartus

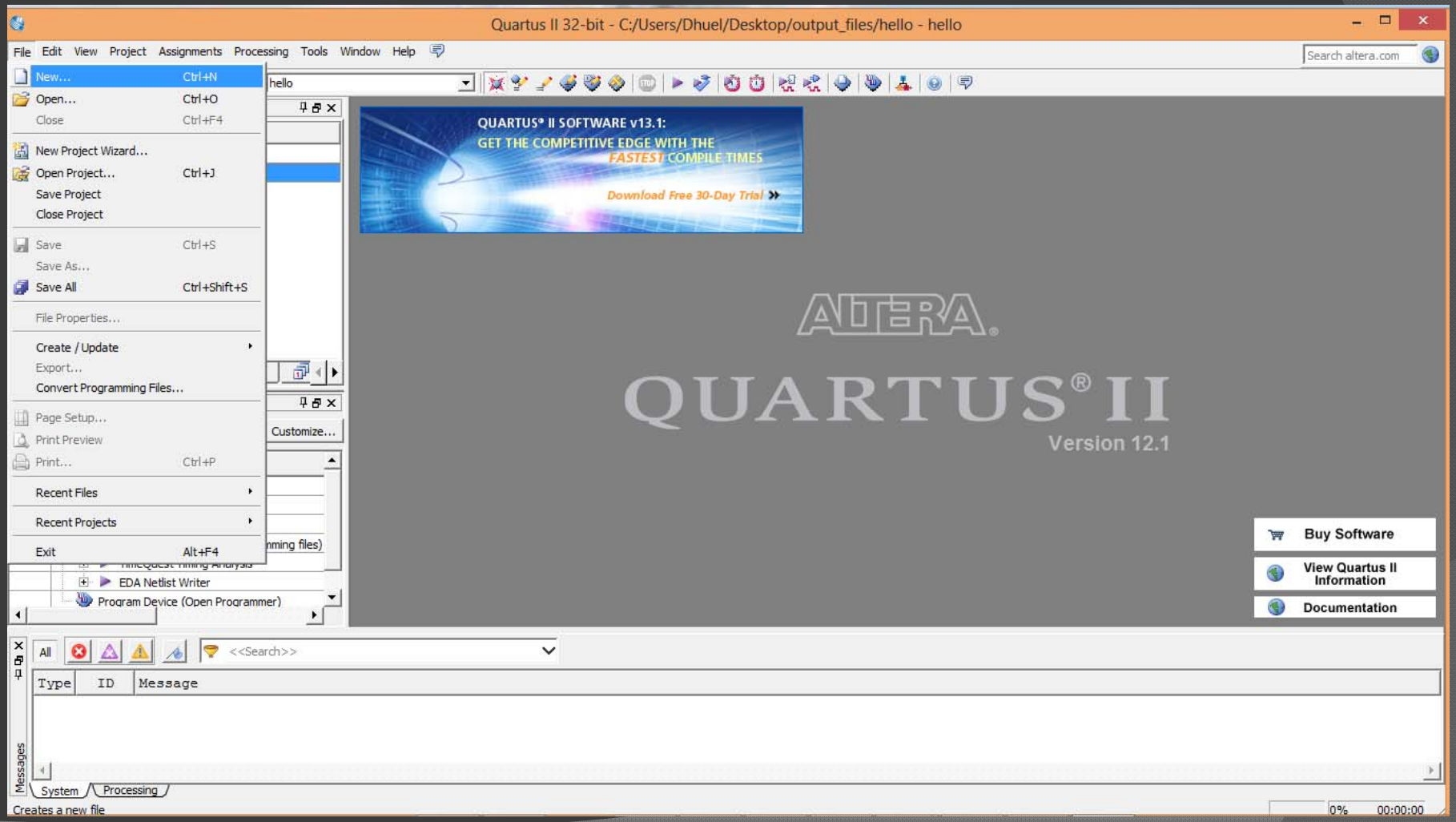

Create
New
Project


Quartus II 32-bit
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator
Compilation Hierarchy
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Buy Software
View Quartus II Information
Documentation
All
<<Search>>
Type
ID
Message
Messages
System
Processing
0%
00:00:00
New Project Wizard
Directory, Name, Top-Level Entity [page 1 of 5]
What is the working directory for this project?
C:\Users\Dhuel\Desktop
What is the name of this project?
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
Use Existing Project Settings...
< Back
Next >
Finish
Cancel
Help

Choose Correct Device



Now, We Begin.


Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/hello - hello
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
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ALTERA
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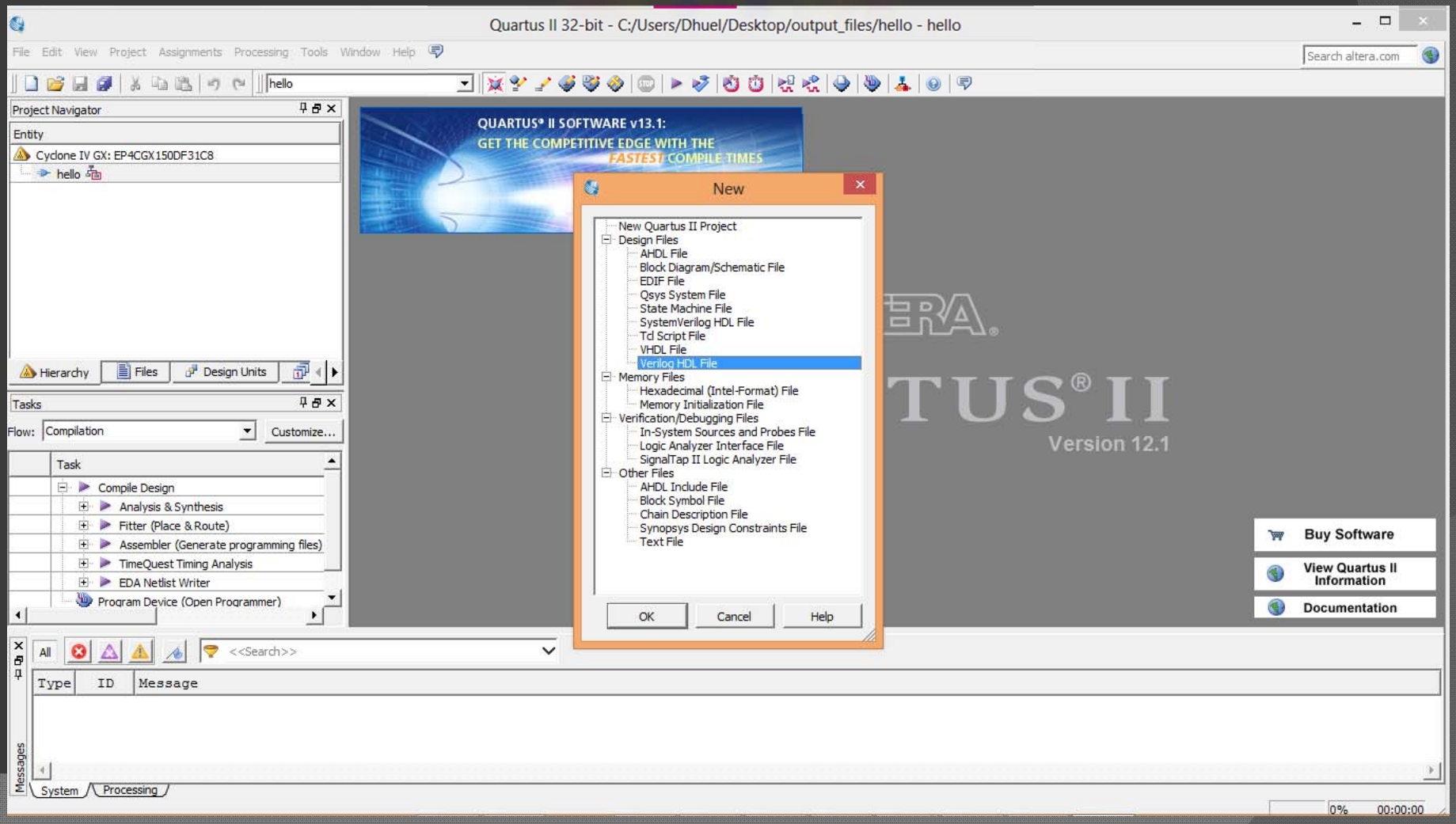
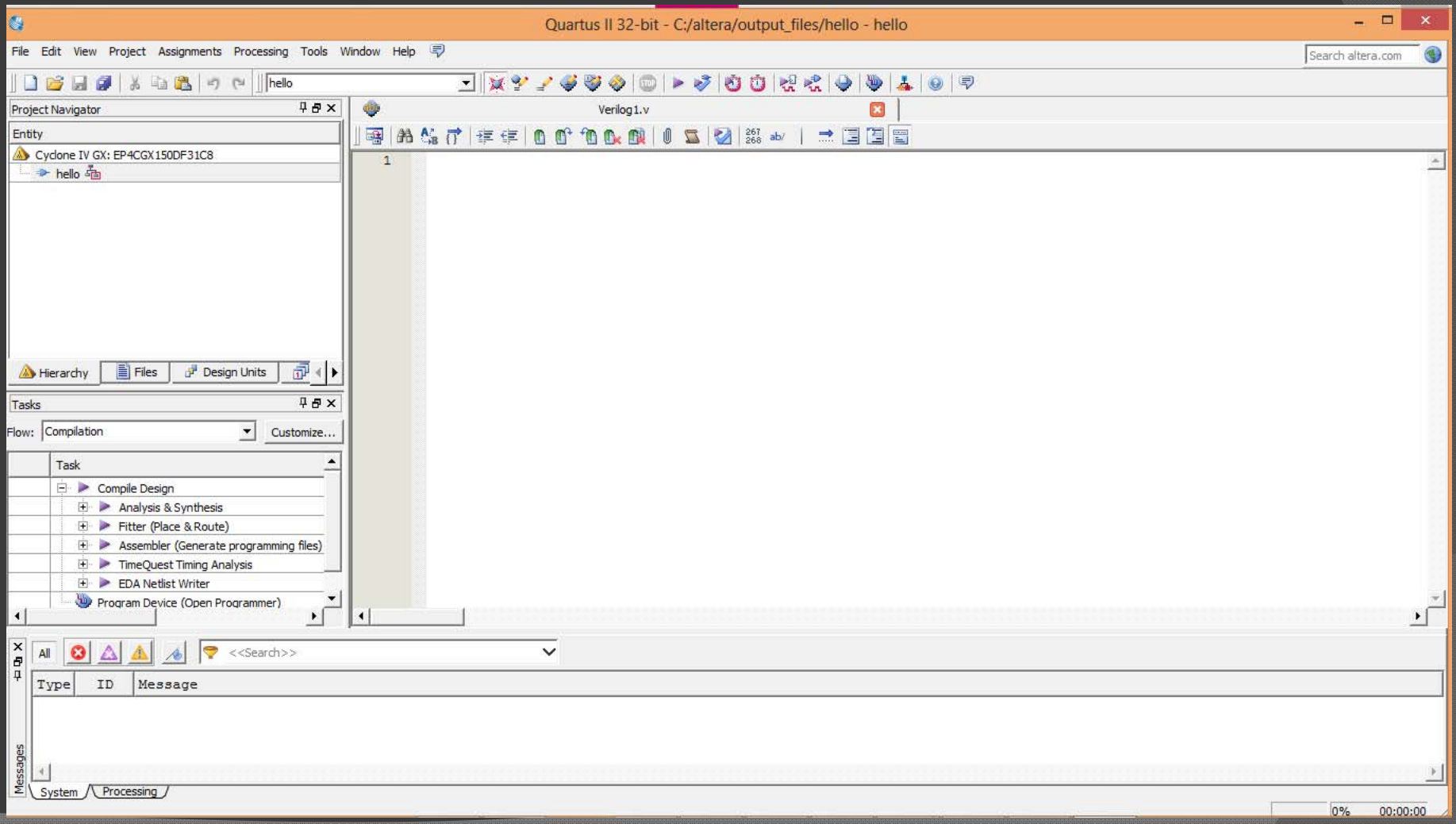
Version 12.1
Buy Software
View Quartus II Information
Documentation
Customize...
EDA Netlist Writer
Program Device (Open Programmer)
All
<<Search>>
Type ID Message
Messages
System Processing
Creates a new file
0% 00:00:00

Verilog is FUN



Time to c-c-c-c-code



List inputs and outputs

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

	Task
20%	Compile Design
✓	Analysis & Synthesis
0%	Fitter (Place & Route)
0%	Assembler (Generate programming files)
0%	TimeQuest Timing Analysis
0%	EDA Netlist Writer
	Program Device (Open Programmer)

../hello.v Start Compilation Compilation Report - hello

```
1  module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2  output LED;
3  input clk;
4  reg [23:0] count;
5  output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
6  endmodule
```

All <<Search>>

Type	ID	Message
	21077	Core supply voltage is 1.2V
	21077	Low junction temperature is 0 degrees C
	21077	High junction temperature is 85 degrees C

Messages

System Processing (24)

Starts a new compilation

20% 00:00:10

Save and Compile

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

../hello.v

Start Compilation

Compilation Report - hello

```
1  module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2  output LED;
3  input clk;
4  reg [23:0] count;
5  output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
6  endmodule
```

Tasks

Flow: Compilation Customize...

	Task
20%	Compile Design
✓	Analysis & Synthesis
0%	Fitter (Place & Route)
0%	Assembler (Generate programming files)
0%	TimeQuest Timing Analysis
0%	EDA Netlist Writer
	Program Device (Open Programmer)

All <<Search>>

Type	ID	Message
	21077	Core supply voltage is 1.2V
	21077	Low junction temperature is 0 degrees C
	21077	High junction temperature is 85 degrees C

Messages

System Processing (24)

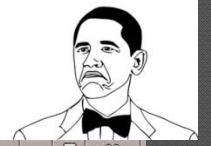
Starts a new compilation

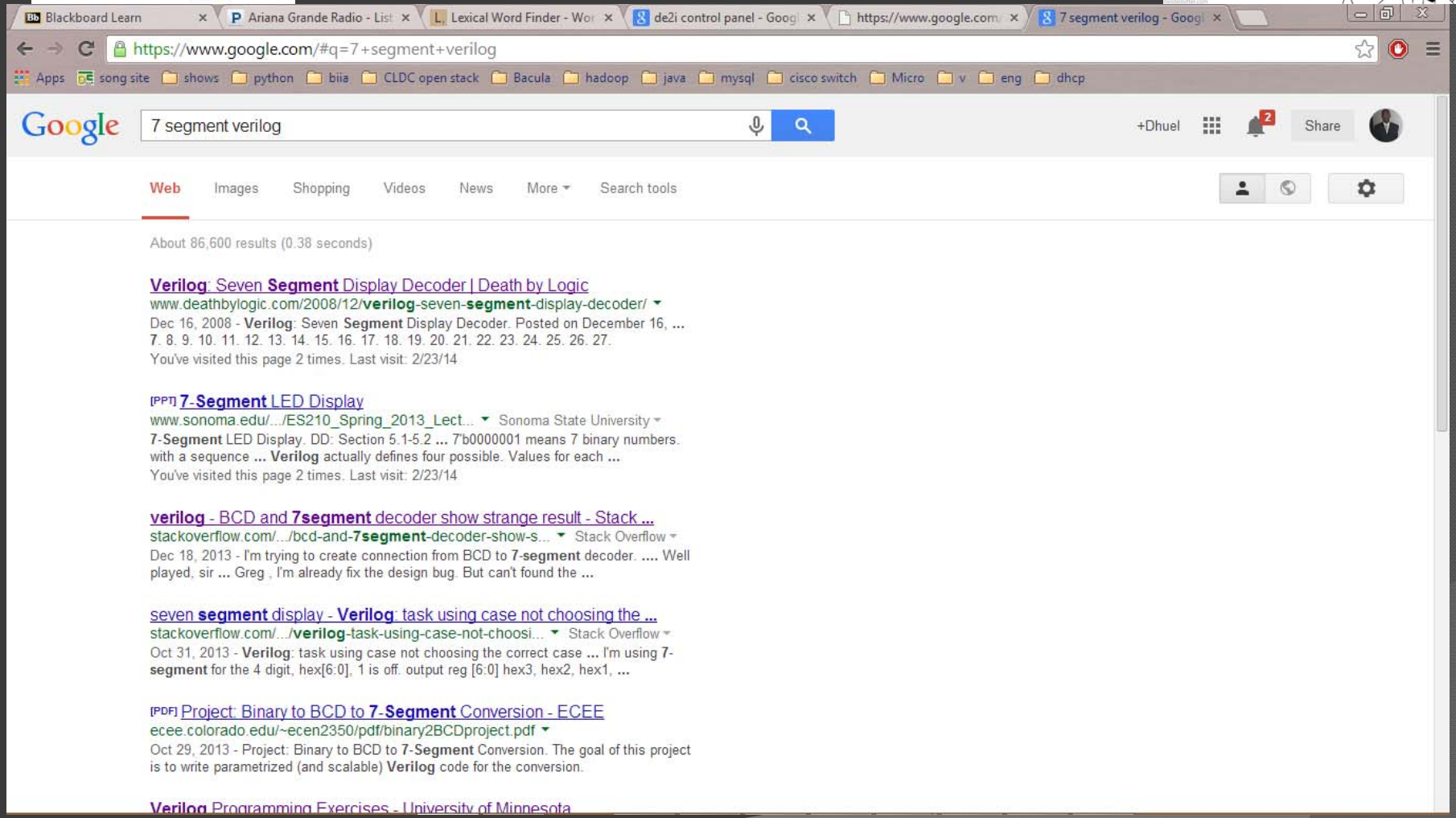
20% 00:00:10

All hail google

Go to Google and see what happens when you search the following terms:

1. Do a barrel roll
2. Askew
3. Anagram
4. Binary
5. Tilt
6. Recursion





Use it as a guide

Blackboard Learn | Ariana Grande Radio - List | Lexical Word Finder - Wor | de2i control panel - Goog | https://www.google.com | Verilog: Seven Segment D

www.deathbylogic.com/2008/12/verilog-seven-segment-display-decoder/

Apps | song site | shows | python | biia | CLDC open stack | Bacula | hadoop | java | mysql | cisco switch | Micro | v | eng | dhcp

This code will take a four bit number and decode it into the seven individual segments to drive a seven segment display. *nIn* is the four bit number to be decoded and *ssOut* is the array of segments for the display going from **a**, being the LSB, to **g** being the MSB.

```
1  module SevenSegmentDisplayDecoder(ssOut, nIn);
2    output reg [6:0] ssOut;
3    input [3:0] nIn;
4
5    // ssOut format {g, f, e, d, c, b, a}
6
7    always @(nIn)
8      case (nIn)
9        4'h0: ssOut = 7'b0111111;
10       4'h1: ssOut = 7'b0000110;
11       4'h2: ssOut = 7'b1011011;
12       4'h3: ssOut = 7'b1001111;
13       4'h4: ssOut = 7'b1100110;
14       4'h5: ssOut = 7'b1101101;
15       4'h6: ssOut = 7'b1111101;
16       4'h7: ssOut = 7'b0000111;
17       4'h8: ssOut = 7'b1111111;
18       4'h9: ssOut = 7'b1100111;
19       4'hA: ssOut = 7'b1110111;
20       4'hB: ssOut = 7'b1111100;
21       4'hC: ssOut = 7'b0111001;
22       4'hD: ssOut = 7'b1011110;
23       4'hE: ssOut = 7'b1111001;
24       4'hF: ssOut = 7'b1110001;
25       default: ssOut = 7'b1001001;
26     endcase
27 endmodule
```

Change Log:

11/1/2010: Added default case statement to prevent possible latching.

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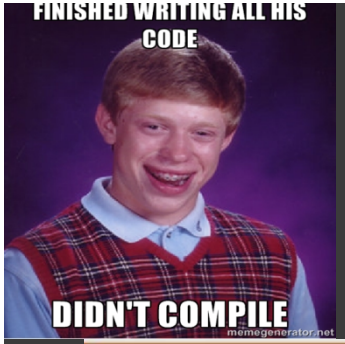
This entry was posted in **Code**, **Hardware** and tagged **Decoder**, **FPGA**, **Seven Segment**, **Verilog** by **Daniel**. Bookmark the **permalink**.



Compile and save

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

../hello.v

Start Compilation

Compilation Report - hello

```
1   module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2   output LED;
3   input clk;
4   reg LEDstatus;
5   reg [23:0] count;
6   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7   reg [3:0] nIn;
8   assign LED = LEDstatus;
9
10  always @(posedge clk) begin
11     LEDstatus <= count[23];
12     count     <= count + 1;
13  end
14
15
16
17
18  endmodule
```

Tasks

Flow: Compilation Customize...

	Task
22%	Compile Design
✓	Analysis & Synthesis
13%	Fitter (Place & Route)
0%	Assembler (Generate programming files)
0%	TimeQuest Timing Analysis
0%	EDA Netlist Writer
	Program Device (Open Programmer)

All <<Search>>

Type	ID	Message
	176444	Device migration not selected. If you intend to use device migration later, you may need to change the pin assignments as they may be incompatible with
	169124	Fitter converted 5 user pins into dedicated programming pins
⚠	15714	Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details

Messages

System Processing (29)

Starts a new compilation

22% 00:00:12

Almost there

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

../hello.v*

Compilation Report - hello

```
2   output LED;
3   input clk;
4   reg LEDstatus;
5   reg [23:0] count;
6   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7   reg [2:0] nIn;
8   assign LED = LEDstatus;
9
10  always @(posedge clk) begin
11     LEDstatus <= count[23];
12     count    <= count + 1;
13  end
14  always @(posedge LEDstatus) begin
15      nIn  <= nIn + 1;
16      case (nIn)
17        4'h0: ssOut = 7'b0001001;
18        4'h1: ssOut = 7'b0000110;
19        4'h2: ssOut = 7'b1000111;
20        4'h3: ssOut = 7'b1000111;
21        4'h4: ssOut = 7'b1000000;
22        4'h5: ssOut = 7'b1111111;
23        4'h6: ssOut = 7'b1111111;
24        4'h7: ssOut = 7'b1111111;
25        4'h8: ssOut = 7'b1111111;
26        default: ssOut = 7'b00000000;
27  endmodule
```

All <<Search>>

Type	ID	Message
	204019	Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
	293000	Quartus II Full Compilation was successful. 0 errors, 43 warnings

Messages

System Processing (120)

Ln 26 Col 36 Verilog HDL File 100% 00:02:02

Errors

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

	Task
✗	Compile Design
✗	Analysis & Synthesis
	Fitter (Place & Route)
	Assembler (Generate programming files)
	TimeQuest Timing Analysis
	EDA Netlist Writer
	Program Device (Open Programmer)

../hello.v*

Compilation Report - hello

```
2   output LED;
3   input clk;
4   reg LEDstatus;
5   reg [23:0] count;
6   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7   reg [2:0] nIn;
8   assign LED = LEDstatus;
9
10  always @(posedge clk) begin
11      LEDstatus <= count[23];
12      count     <= count + 1;
13  end
14  always @(posedge LEDstatus) begin
15      nIn  <= nIn + 1;
16      case (nIn)
17        4'h0: ssOut = 7'b0001001;
18        4'h1: ssOut = 7'b0000110;
19        4'h2: ssOut = 7'b1000111;
20        4'h3: ssOut = 7'b1000111;
21        4'h4: ssOut = 7'b1000000;
22        4'h5: ssOut = 7'b1111111;
23        4'h6: ssOut = 7'b1111111;
24        4'h7: ssOut = 7'b1111111;
25        4'h8: ssOut = 7'b1111111;
26        default: ssOut = 7'b00000000;
27        end
28  endmodule
```

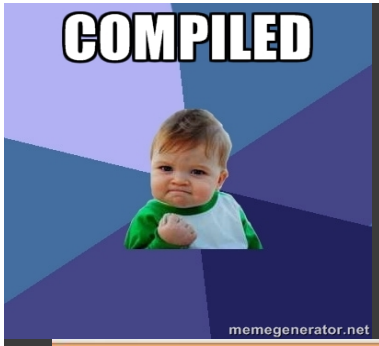
All <<Search>>

Type	ID	Message
✗	10170	Verilog HDL syntax error at hello.v(27) near text "endmodule"; expecting "endcase"
✗		Quartus II 32-bit Analysis & Synthesis was unsuccessful. 1 error, 0 warnings
✗	293001	Quartus II Full Compilation was unsuccessful. 3 errors, 0 warnings

Messages

System Processing (3)

2% 00:00:04



Let’s test it!!!!

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Device...
Settings... Ctrl+Shift+E
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D

Project Navigator
Entity
Cyclone IV GX: EP4CGX
hello

../hello.v
Compilation Report - hello

```
ule hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
put LED;
ut clk;
 LEDstatus;
 [23:0] count;
put reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
 [2:0] nIn;
ign LED = LEDstatus;

ays @(posedge clk) begin
LEDstatus <= count[23];
count    <= count + 1;
end
always @(posedge LEDstatus) begin
    nIn  <= nIn + 1;
    case (nIn)
      4'h0: ssOut = 7'b0001001;
      4'h1: ssOut = 7'b0000110;
      4'h2: ssOut = 7'b1000111;
      4'h3: ssOut = 7'b1000111;
      4'h4: ssOut = 7'b1000000;
      4'h5: ssOut = 7'b1111111;
      4'h6: ssOut = 7'b1111111;
      4'h7: ssOut = 7'b1111111;
      4'h8: ssOut = 7'b1111111;
      default: ssOut = 7'b00000000;
      endcase
```

Hierarchy Files Design Units

Tasks
Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

All <<Search>>

Type	ID	Message
	204019	Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
	293000	Quartus II Full Compilation was successful. 0 errors, 37 warnings

Messages
System Processing (123)
Edits pin assignments
100% 00:02:05

Assign pins

Pin Planner - C:/altera/output_files/hello - hello

File Edit View Processing Tools Window Help

Top View - Wire Bond
Cyclone IV GX - EP4CGX150DF31C8

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter L
LED	Output				PIN_F16
clk	Input				PIN_W15
ssOut[6]	Output	PIN_F14	8	B8_N0	PIN_AH2
ssOut[5]	Output	PIN_D16	8	B8_N0	PIN_AE11
ssOut[4]	Output	PIN_A3			PIN_AD10
ssOut[3]	Output				PIN_AH3

DE2i-150_FPGA_System_manual.pdf - Adobe Reader

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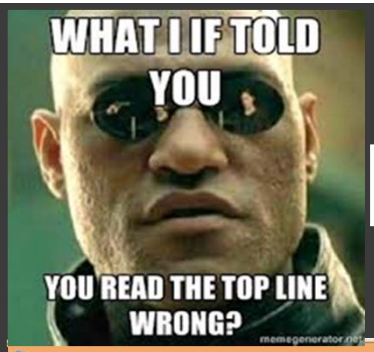
Figure 3-11 Connections between the 7-segment display HEX0 and Cyclone IV GX FPGA

Table 3-5 Pin Assignments for 7-segment Displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX0[0]	PIN_E15	Seven Segment Digit 0[0]	2.5V
HEX0[1]	PIN_E12	Seven Segment Digit 0[1]	2.5V
HEX0[2]	PIN_G11	Seven Segment Digit 0[2]	2.5V
HEX0[3]	PIN_F11	Seven Segment Digit 0[3]	2.5V
HEX0[4]	PIN_F16	Seven Segment Digit 0[4]	2.5V
HEX0[5]	PIN_D16	Seven Segment Digit 0[5]	2.5V
HEX0[6]	PIN_F14	Seven Segment Digit 0[6]	2.5V
HEX1[0]	PIN_G14	Seven Segment Digit 1[0]	2.5V
HEX1[1]	PIN_B13	Seven Segment Digit 1[1]	2.5V
HEX1[2]	PIN_G13	Seven Segment Digit 1[2]	2.5V
HEX1[3]	PIN_F12	Seven Segment Digit 1[3]	2.5V
HEX1[4]	PIN_G12	Seven Segment Digit 1[4]	2.5V
HEX1[5]	PIN_J9	Seven Segment Digit 1[5]	2.5V
HEX1[6]	PIN_G10	Seven Segment Digit 1[6]	2.5V
HEX2[0]	PIN_G8	Seven Segment Digit 2[0]	2.5V
HEX2[1]	PIN_G7	Seven Segment Digit 2[1]	2.5V
HEX2[2]	PIN_F7	Seven Segment Digit 2[2]	2.5V
HEX2[3]	PIN_AG30	Seven Segment Digit 2[3]	2.5V
HEX2[4]	PIN_F6	Seven Segment Digit 2[4]	2.5V
HEX2[5]	PIN_F4	Seven Segment Digit 2[5]	2.5V
HEX2[6]	PIN_F10	Seven Segment Digit 2[6]	2.5V
HEX3[0]	PIN_D10	Seven Segment Digit 3[0]	2.5V
HEX3[1]	PIN_D7	Seven Segment Digit 3[1]	2.5V
HEX3[2]	PIN_E6	Seven Segment Digit 3[2]	2.5V
HEX3[3]	PIN_E4	Seven Segment Digit 3[3]	2.5V
HEX3[4]	PIN_E3	Seven Segment Digit 3[4]	2.5V
HEX3[5]	PIN_D5	Seven Segment Digit 3[5]	2.5V
HEX3[6]	PIN_D4	Seven Segment Digit 3[6]	2.5V
HEX4[0]	PIN_A14	Seven Segment Digit 4[0]	2.5V
HEX4[1]	PIN_A13	Seven Segment Digit 4[1]	2.5V



Don’t forget to compile

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

	Task
26%	Compile Design
✓	Analysis & Synthesis
30%	Fitter (Place & Route)
0%	Assembler (Generate programming files)
0%	TimeQuest Timing Analysis
0%	EDA Netlist Writer
	Program Device (Open Programmer)

../hello.v

Start Compilation

Compilation Report - hello

```
1   module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
2   output LED;
3   input clk;
4   reg LEDstatus;
5   reg [23:0] count;
6   output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
7   reg [2:0] nIn;
8   assign LED = LEDstatus;
9
10  always @(posedge clk) begin
11     LEDstatus <= count[23];
12     count     <= count + 1;
13  end
14  always @(posedge LEDstatus) begin
15      nIn  <= nIn + 1;
16      case (nIn)
17        4'h0: ssOut = 7'b0001001;
18        4'h1: ssOut = 7'b0000110;
19        4'h2: ssOut = 7'b1000111;
20        4'h3: ssOut = 7'b1000111;
21        4'h4: ssOut = 7'b1000000;
22        4'h5: ssOut = 7'b1111111;
23        4'h6: ssOut = 7'b1111111;
24        4'h7: ssOut = 7'b1111111;
25        4'h8: ssOut = 7'b1111111;
26        default: ssOut = 7'b00000000;
27        endcase
```

All <<Search>>

Type	ID	Message
	176214	Statistics of I/O pins that need to be placed that use the same VCCIO and VREF, before I/O pin placement
	176215	I/O bank details before I/O pin placement
	171121	Fitter preparation operations ending: elapsed time is 00:00:09

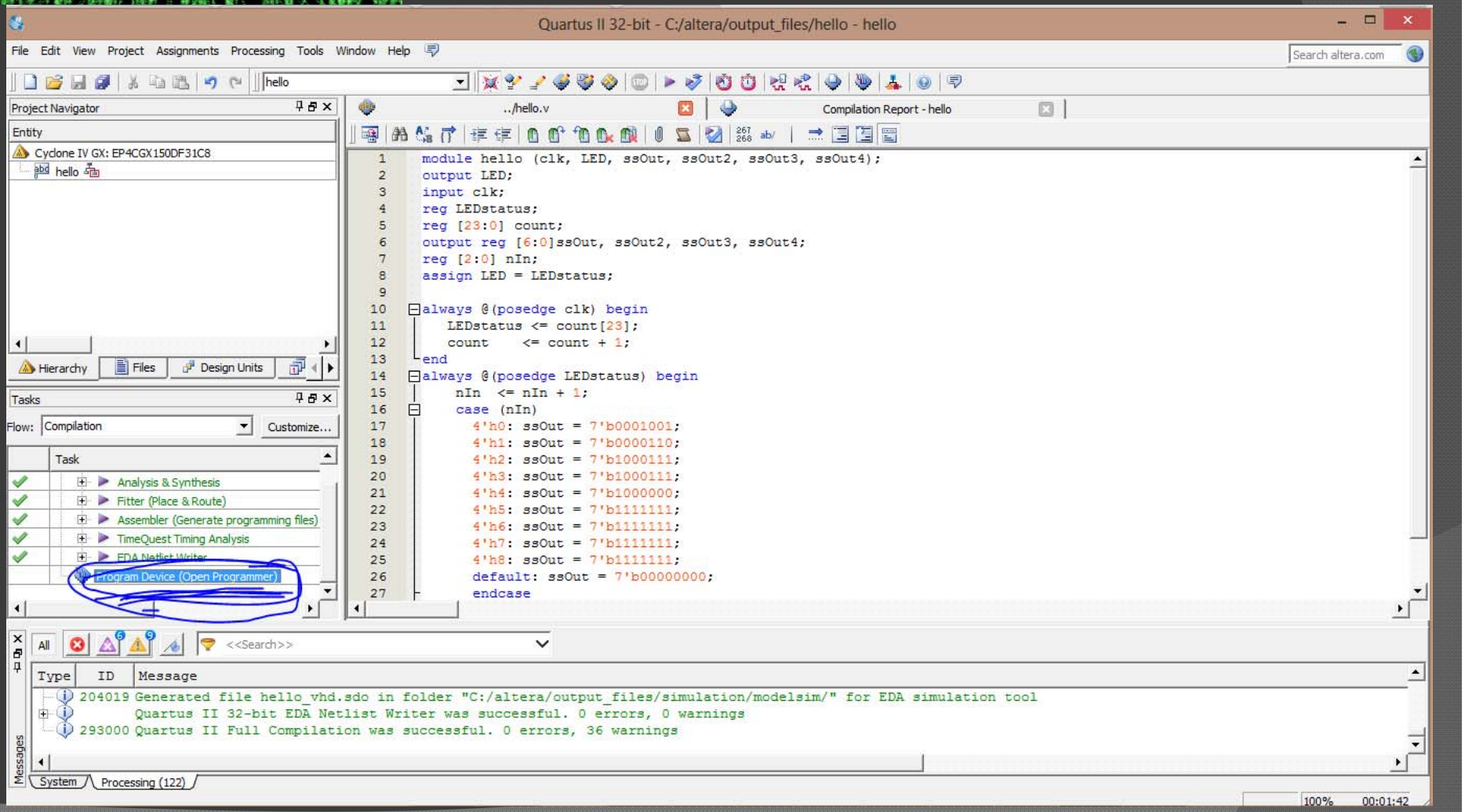
Messages

System Processing (44)

Starts a new compilation

26% 00:00:33

Program device



USB blaster and JTAG

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	
Analysis & Synthesis	✓
Fitter (Place & Route)	✓
Assembler (Generate programming files)	✓
TimeQuest Timing Analysis	✓
EDA Netlist Writer	✓
Program Device (Open Programmer)	

../hello.v

Compilation Report - hello

Programmer - C:/altera/output_files/hello - hello - [output_files/hel...

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down

File	Device	Checksum	Usercode	Pr Co
output_files/hello.sof	EP4CGX150DF31	007269E9	FFFFFFFF	

TDI

ALTERA

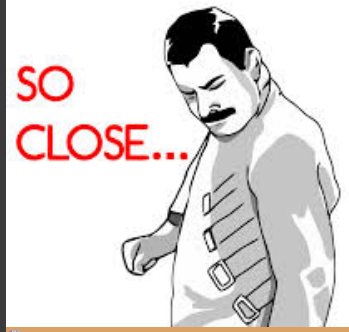
All <<Search>>

Type	ID	Message
	204019	Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
	293000	Quartus II Full Compilation was successful. 0 errors, 36 warnings

Messages

System Processing (122)

100% 00:01:42



Almost there

Programmer - C:/altera/output_files/hello - hello - [output_files/hello.cdf]*

File Edit View Processing Tools Window Help

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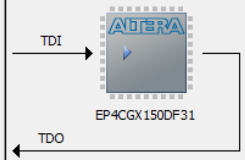
Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 35%

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/hello.sof	EP4CGX150DF31	007269E9	FFFFFFFF	☑	☐	☐	☐	☐	☐	☐



Repeat and reuse

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

../hello.v*

Compilation Report - hello

```
19          4'h2: ssOut = 7'b1000111;
20          4'h3: ssOut = 7'b1000111;
21          4'h4: ssOut = 7'b1000000;
22          4'h5: ssOut = 7'b1111111;
23          4'h6: ssOut = 7'b1111111;
24          4'h7: ssOut = 7'b1111111;
25          4'h8: ssOut = 7'b1111111;
26          default: ssOut = 7'b00000000;
27          endcase
28  always @(posedge LEDstatus) begin
29      nIn2  <= nIn2 + 1;
30      case (nIn2)
31          4'h0: ssOut = 7'b1111111;
32          4'h1: ssOut = 7'b0001001;
33          4'h2: ssOut = 7'b0000110;
34          4'h3: ssOut = 7'b1000111;
35          4'h4: ssOut = 7'b1000111;
36          4'h5: ssOut = 7'b1000000;
37          4'h6: ssOut = 7'b1111111;
38          4'h7: ssOut = 7'b1111111;
39          4'h8: ssOut = 7'b1111111;
40          default: ssOut = 7'b00000000;
41          endcase
42  always @(posedge LEDstatus) begin
43      nIn3  <= nIn3 + 1;
44      case (nIn3)
45          4'h0: ssOut = 7'b1111111;
```

All <<Search>>

Type	ID	Message
	204019	Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
	293000	Quartus II Full Compilation was successful. 0 errors, 36 warnings

Messages

System (74) Processing (122)

100% 00:01:42

Remember to get the pins

Pin Planner - C:/altera/output_files/hello - hello

Top View - Wire Bond
Cyclone IV GX - EP4CGX150DF31C8

Node Name	Direction	Location	I/O Bank	VREF Group
LED	Output			
clk	Input	PIN_AJ16	4	B4_N2
ssOut[6]	Output	PIN_F14	8	B8_N0
ssOut[5]	Output	PIN_D16	8	B8_N0
ssOut[4]	Output	PIN_F16	8	B8_N0
ssOut[3]	Output	PIN_F11	8	B8_N1

DE2i-150_FPGA_System_manual.pdf - Adobe Reader

Figure 3-11 Connections between the 7-segment display HEX0 and

Table 3-5 Pin Assignments for 7-segment Displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX0[0]	PIN_E15	Seven Segment Digit 0[0]	2.5V
HEX0[1]	PIN_E12	Seven Segment Digit 0[1]	2.5V
HEX0[2]	PIN_G11	Seven Segment Digit 0[2]	2.5V
HEX0[3]	PIN_F11	Seven Segment Digit 0[3]	2.5V
HEX0[4]	PIN_F16	Seven Segment Digit 0[4]	2.5V
HEX0[5]	PIN_D16	Seven Segment Digit 0[5]	2.5V
HEX0[6]	PIN_F14	Seven Segment Digit 0[6]	2.5V
HEX1[0]	PIN_G14	Seven Segment Digit 1[0]	2.5V
HEX1[1]	PIN_B13	Seven Segment Digit 1[1]	2.5V
HEX1[2]	PIN_G13	Seven Segment Digit 1[2]	2.5V
HEX1[3]	PIN_F12	Seven Segment Digit 1[3]	2.5V
HEX1[4]	PIN_G12	Seven Segment Digit 1[4]	2.5V
HEX1[5]	PIN_J9	Seven Segment Digit 1[5]	2.5V
HEX1[6]	PIN_G10	Seven Segment Digit 1[6]	2.5V
HEX2[0]	PIN_G8	Seven Segment Digit 2[0]	2.5V
HEX2[1]	PIN_G7	Seven Segment Digit 2[1]	2.5V
HEX2[2]	PIN_F7	Seven Segment Digit 2[2]	2.5V
HEX2[3]	PIN_AG30	Seven Segment Digit 2[3]	2.5V
HEX2[4]	PIN_F6	Seven Segment Digit 2[4]	2.5V
HEX2[5]	PIN_F4	Seven Segment Digit 2[5]	2.5V
HEX2[6]	PIN_F10	Seven Segment Digit 2[6]	2.5V
HEX3[0]	PIN_D10	Seven Segment Digit 3[0]	2.5V
HEX3[1]	PIN_D7	Seven Segment Digit 3[1]	2.5V
HEX3[2]	PIN_E6	Seven Segment Digit 3[2]	2.5V
HEX3[3]	PIN_E4	Seven Segment Digit 3[3]	2.5V
HEX3[4]	PIN_E3	Seven Segment Digit 3[4]	2.5V
HEX3[5]	PIN_D5	Seven Segment Digit 3[5]	2.5V
HEX3[6]	PIN_D4	Seven Segment Digit 3[6]	2.5V
HEX4[0]	PIN_A14	Seven Segment Digit 4[0]	2.5V
HEX4[1]	PIN_A13	Seven Segment Digit 4[1]	2.5V

Terasic DE2i-150 User Manual 34 www.terasic.com

Oh no!

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	
	Analysis & Synthesis
	Fitter (Place & Route)
	Assembler (Generate programming files)
	TimeQuest Timing Analysis
	EDA Netlist Writer
	Program Device (Open Programmer)

../hello.v

Compilation Report - hello

```
46          4'h1: ssOut = 7'b1111111;
47          4'h2: ssOut = 7'b0001001;
48          4'h3: ssOut = 7'b0000110;
49          4'h4: ssOut = 7'b1000111;
50          4'h5: ssOut = 7'b1000111;
51          4'h6: ssOut = 7'b1000000;
52          4'h7: ssOut = 7'b1111111;
53          4'h8: ssOut = 7'b1111111;
54          default: ssOut = 7'b00000000;
55          endcase
56  always @(posedge LEDstatus) begin
57      nIn4  <= nIn4 + 1;
58      case (nIn4)
59          4'h0: ssOut = 7'b1111111;
60          4'h1: ssOut = 7'b1111111;
61          4'h2: ssOut = 7'b1111111;
62          4'h3: ssOut = 7'b0001001;
63          4'h4: ssOut = 7'b0000110;
64          4'h5: ssOut = 7'b1000111;
65          4'h6: ssOut = 7'b1000111;
66          4'h7: ssOut = 7'b1000000;
67          4'h8: ssOut = 7'b1111111;
68          default: ssOut = 7'b00000000;
69          endcase
70  end
71  endmodule
```

All <<Search>>

Type	ID	Message
	10170	Verilog HDL syntax error at hello.v(28) near text "always"; expecting "end"
	10170	Verilog HDL syntax error at hello.v(42) near text "always"; expecting "end"
	10170	Verilog HDL syntax error at hello.v(56) near text "always"; expecting "end"
	10170	Verilog HDL syntax error at hello.v(71) near text "endmodule"; expecting "end"

Messages

System (34) Processing (6)

2% 00:00:02

Remember to change SsOuts

Quartus II 32-bit - C:/altera/output_files/hello - hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

hello

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

hello

Hierarchy Files Design Units

../hello.v*

Compilation Report - hello

```
16      case (nIn)
17        4'h0: ssOut = 7'b0001001;
18        4'h1: ssOut = 7'b0000110;
19        4'h2: ssOut = 7'b1000111;
20        4'h3: ssOut = 7'b1000111;
21        4'h4: ssOut = 7'b1000000;
22        4'h5: ssOut = 7'b1111111;
23        4'h6: ssOut = 7'b1111111;
24        4'h7: ssOut = 7'b1111111;
25        4'h8: ssOut = 7'b1111111;
26        default: ssOut = 7'b00000000;
27        endcase
28    end
29  always @(posedge LEDstatus) begin
30      nIn2  <= nIn2 + 1;
31      case (nIn2)
32        4'h0: ssOut2 = 7'b1111111;
33        4'h1: ssOut2 = 7'b0001001;
34        4'h2: ssOut2 = 7'b0000110;
35        4'h3: ssOut2 = 7'b1000111;
36        4'h4: ssOut2 = 7'b1000111;
37        4'h5: ssOut2 = 7'b1000000;
38        4'h6: ssOut2 = 7'b1111111;
39        4'h7: ssOut2 = 7'b1111111;
40        4'h8: ssOut2 = 7'b1111111;
41        default: ssOut = 7'b00000000;
42        endcase
```

Tasks

Flow: Compilation Customize...

Task
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

All <<Search>>

Type	ID	Message
Error	10028	Can't resolve multiple constant drivers for net "ssOut[6]" at hello.v(29)
Error	10029	Constant driver at hello.v(14)
Error	10028	Can't resolve multiple constant drivers for net "ssOut[5]" at hello.v(29)
Error	10028	Can't resolve multiple constant drivers for net "ssOut[4]" at hello.v(29)

Messages

System (34) Processing (11)

9% 00:00:02

One more thing!!!

Quartus II 32-bit - C:/altera/output_files/hello - hello

```
16      case (nIn)
17        4'h0: ssOut = 7'b0001001;
18        4'h1: ssOut = 7'b0000110;
19        4'h2: ssOut = 7'b1000111;
20        4'h3: ssOut = 7'b1000111;
21        4'h4: ssOut = 7'b1000000;
22        4'h5: ssOut = 7'b1111111;
23        4'h6: ssOut = 7'b1111111;
24        4'h7: ssOut = 7'b1111111;
25        4'h8: ssOut = 7'b1111111;
26        default: ssOut = 7'b00000000;
27        endcase
28    end
29    always @(posedge LEDstatus) begin
30        nIn2  <= nIn2 + 1;
31        case (nIn2)
32          4'h0: ssOut2 = 7'b1111111;
33          4'h1: ssOut2 = 7'b0001001;
34          4'h2: ssOut2 = 7'b0000110;
35          4'h3: ssOut2 = 7'b1000111;
36          4'h4: ssOut2 = 7'b1000111;
37          4'h5: ssOut2 = 7'b1000000;
38          4'h6: ssOut2 = 7'b1111111;
39          4'h7: ssOut2 = 7'b1111111;
40          4'h8: ssOut2 = 7'b1111111;
41          default: ssOut = 7'b00000000;
42          endcase
```

```
204019 Generated file hello_vhd.sdo in folder "C:/altera/output_files/simulation/modelsim/" for EDA simulation tool
       Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 17 warnings
```

Congratulations!!!

Warning for the Next Subject (Schematics)

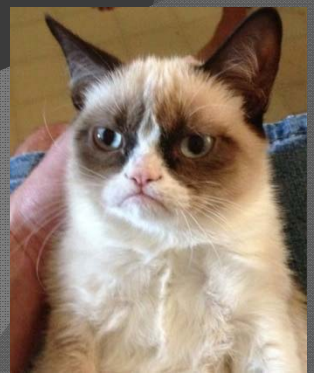
If you are comfortable with creating circuits then this method will be easy and probably more favorable for you. If not, don't torture yourself……

……

……

……

Seriously……don't



Follow previous setup instructions

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

All <<Search>>

Type ID Message

Messages

System Processing

0% 00:00:00

Buy Software

View Quartus II Information

Documentation

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

C:\Users\Dhuel\Desktop

What is the name of this project?

schematc_HELLO

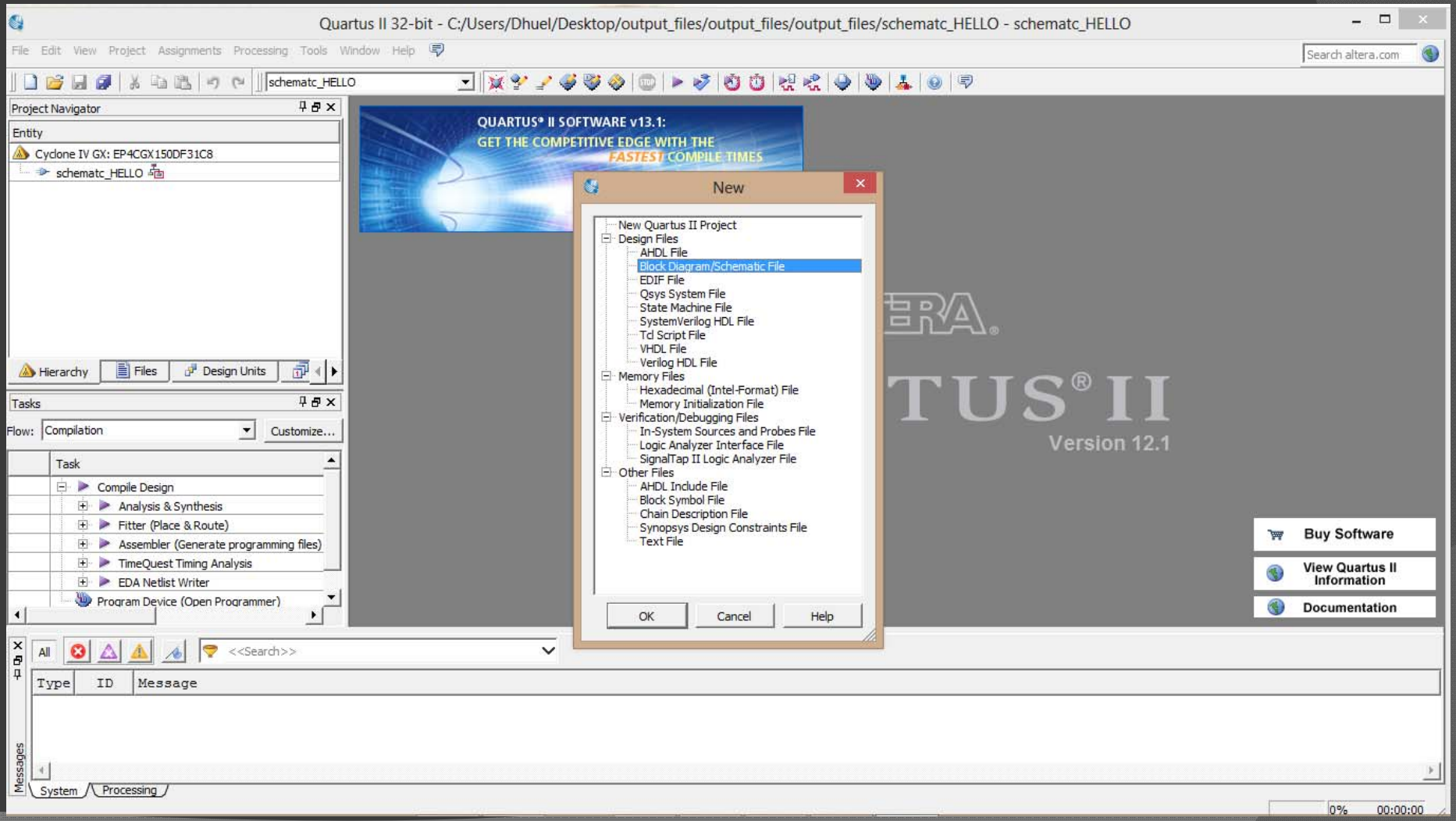
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

schematc_HELLO

Use Existing Project Settings...

< Back Next > Finish Cancel Help

Choose block diagram/Schematic file



Note

- In order to continue, it would be best if you have already sketched or thought about the circuit that you will need to create.
- For demonstration purposes, I will show how to display a simple HELLO on the 7 segment display.

Choose inputs and outputs

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/output_files/schematc_HELLO - schematc_HELLO

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

schematc_HELLO

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

schematc_HELLO

Hierarchy Files Design Units

Block1.bdf

Input

Output

Bidir

Tasks

Flow: Compilation Customize...

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming files)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

All

<<Search>>

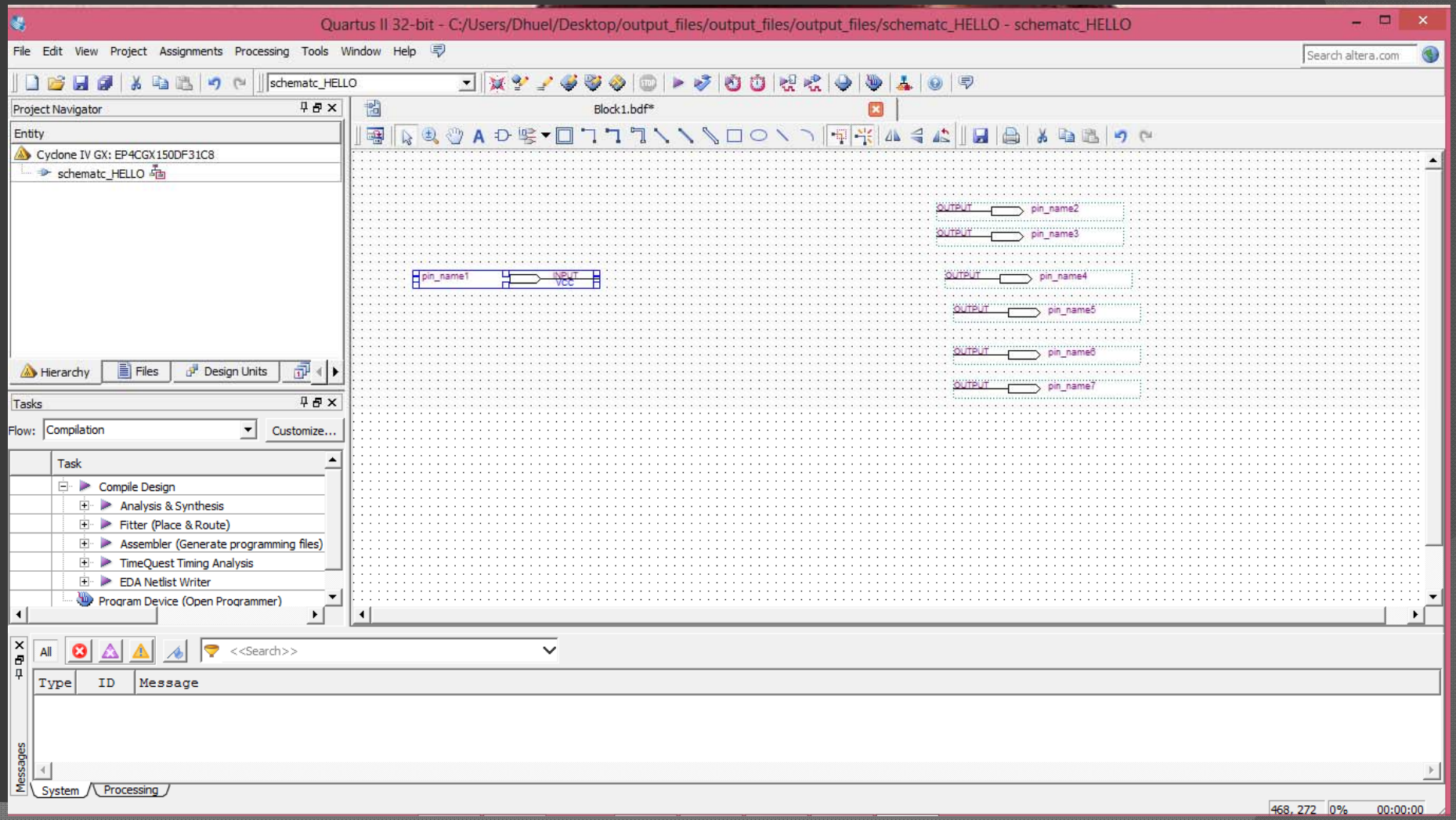
Type ID Message

Messages

System Processing

197, 1 0% 00:00:00

Place all the pins you will



If you require other gates/switches/latches/ etc.

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/output_files/schematc_HELLO - schematc_HELLO

Symbol

Libraries:

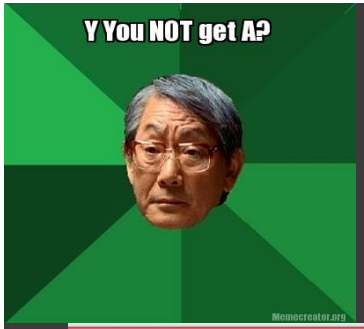
c:/altera/12.1/quartus/libraries/
megafunctions
others
primitives
buffer
logic
other
pin
storage

Name:

Repeat-insert mode
Insert symbol as block
Launch MegaWizard Plug-In

MegaWizard Plug-In Manager...

OK Cancel



Place two NOT gates

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/output_files/schematc_HELLO - schematc_HELLO

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

schematc_HELLO

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

schematc_HELLO

Hierarchy Files Design Units

Block1.bdf*

pin_name1 VCC

NOT inst

NOT inst1

OUTPUT pin_name2

OUTPUT pin_name3

OUTPUT pin_name4

OUTPUT pin_name5

OUTPUT pin_name6

OUTPUT pin_name7

Tasks

Flow: Compilation Customize...

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming files)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

All <<Search>>

Type ID Message

Messages

System Processing

179, 18 0% 00:00:00

Connect wires using wire diagrams

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/output_files/schematc_HELLO - schematc_HELLO

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

schematc_HELLO

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

schematc_HELLO

Hierarchy Files Design Units

Block1.bdf*

Orthogonal Node Tool

pin_name1 pin_name2 pin_name3 pin_name4 pin_name5 pin_name6 pin_name7

Tasks

Flow: Compilation Customize...

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming files)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

All <<Search>>

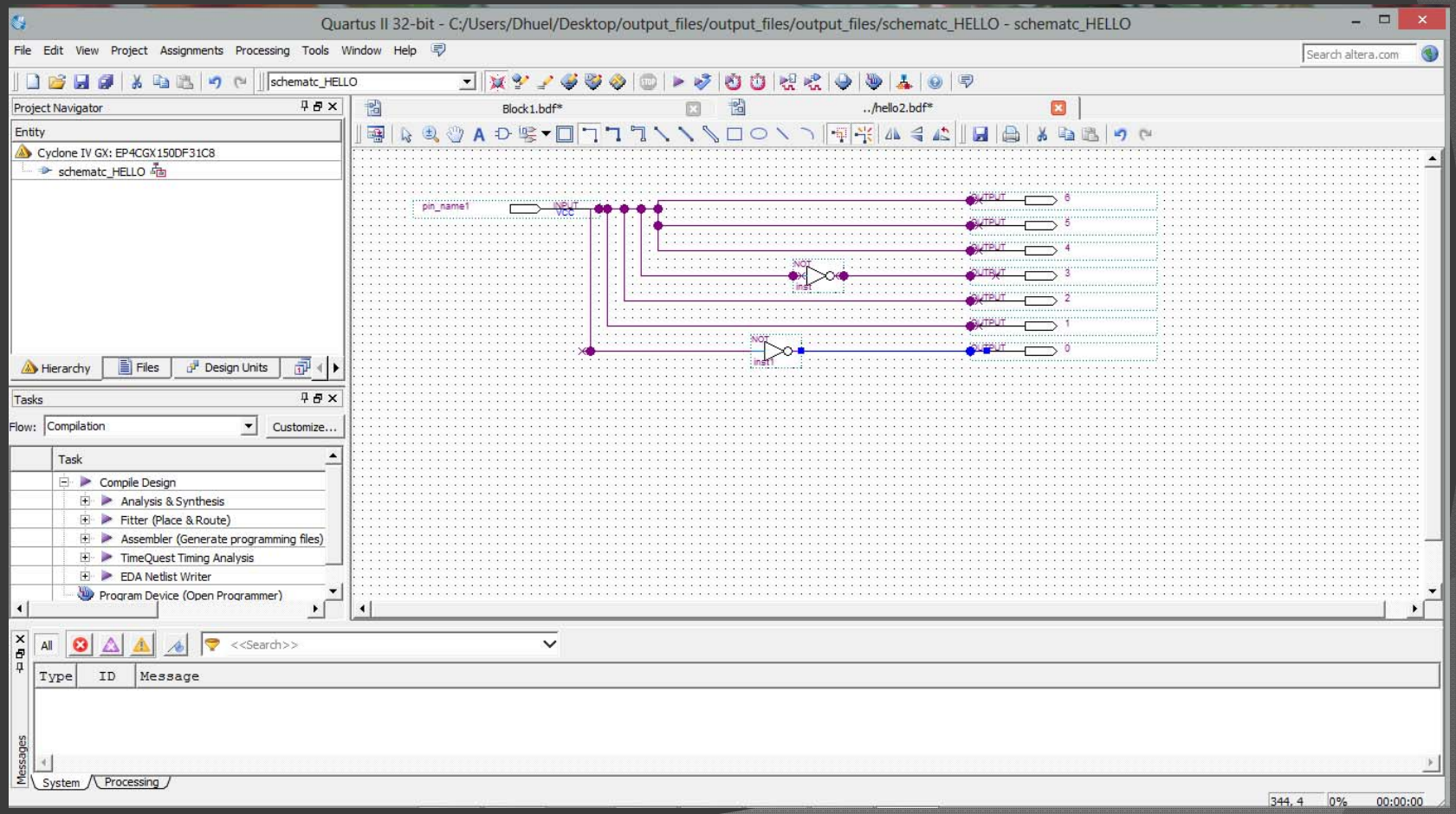
Type ID Message

Messages

System Processing

223, 0 0% 00:00:00

Neat work also helps with understanding



Double click items to rename

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/hello2 - hello2

Pin Properties

General | Format

To create multiple pins, enter a name in AHDL bus notation
(For example: "name[3..0]"), or enter a comma-seperated list of names.

Pin name(s): 6

Default value: VCC

OK | Cancel | Help

Don’t forget to compile!

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/output_files/schematc_HELLO - schematc_HELLO

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

schematc_HELLO

Project Navigator

Entity

Cyclone IV GX: EP4CGX150DF31C8

schematc_HELLO

Hierarchy Files Design Units

../schematc_HELLO.bdf ../hello2.bdf Compilation Report - schematc_HELLO

pin_name1 VCC NOT inst OUTPUT 6 5 4 3 2 1 0 inst1

Tasks

Flow: Compilation Customize...

	Task
34%	
✓	Analysis & Synthesis
71%	Fitter (Place & Route)
0%	Assembler (Generate programming files)
0%	TimeQuest Timing Analysis
0%	EDA Netlist Writer
	Program Device (Open Programmer)

All <<Search>>

Type	ID	Message
	170137	Fitter placement was successful
	170192	Fitter placement operations ending: elapsed time is 00:00:01
	170193	Fitter routing operations beginning

Messages System Processing (48)

377, 17 34% 00:00:18

Assign Pins

Quartus II 32-bit - C:/Users/Dhuel/Desktop/output_files/output_files/hello2 - hello2

File Edit View Project Assignments Processing Tools Window Help

Device...
Settings... Ctrl+Shift+E
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D

Project Navigator
Entity
Cyclone IV GX: EP4CGX
hello2

Hierarchy Files Design Units

Tasks
Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

hello2.bdf

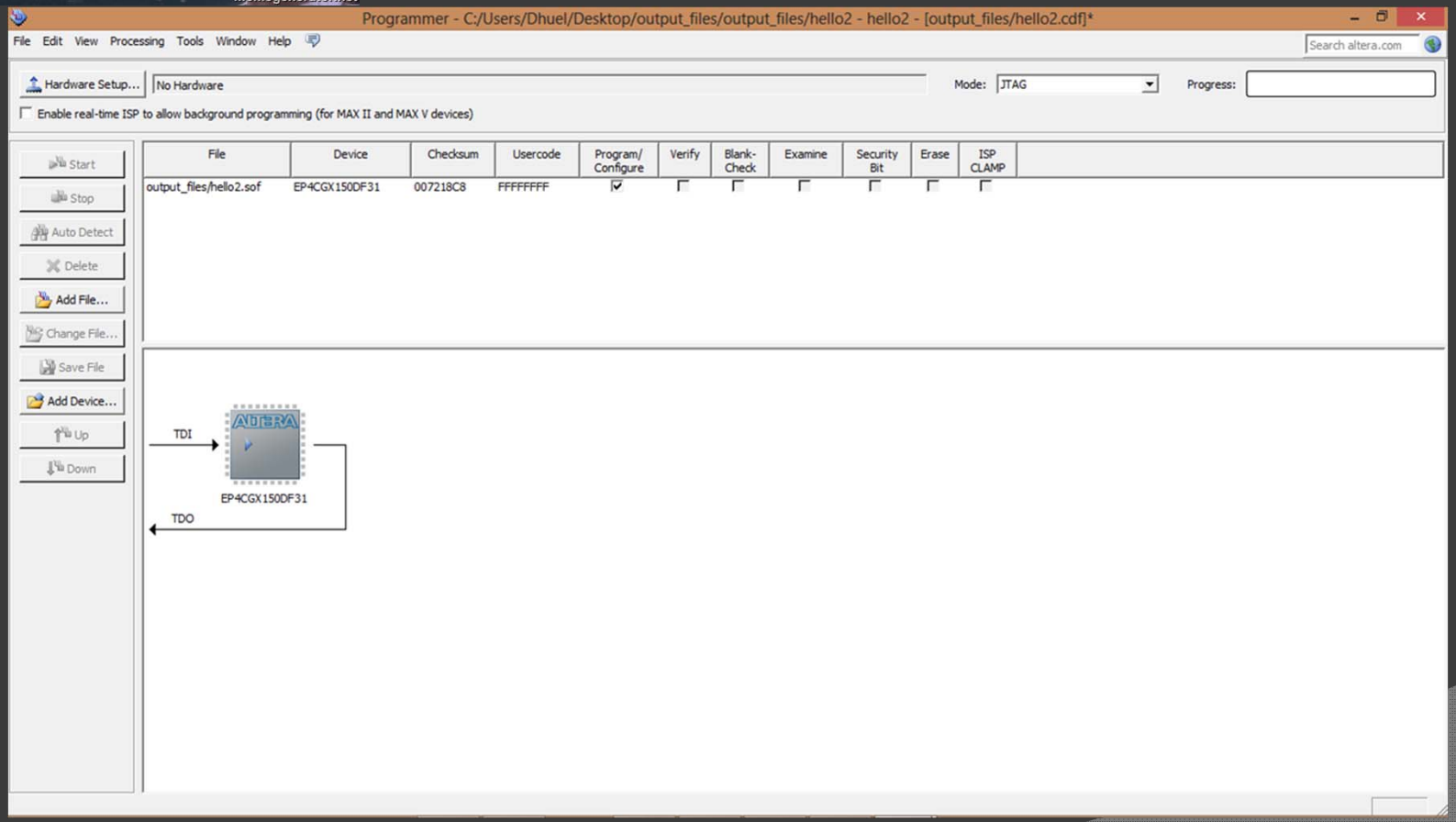
pin_name1 VCC NOT inst

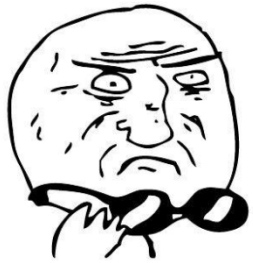
PIN_E15 PIN_F14 PIN_D16 PIN_F11 PIN_F16 PIN_G11 PIN_E12

All <<Search>>
Type ID Message
System Processing
Messages

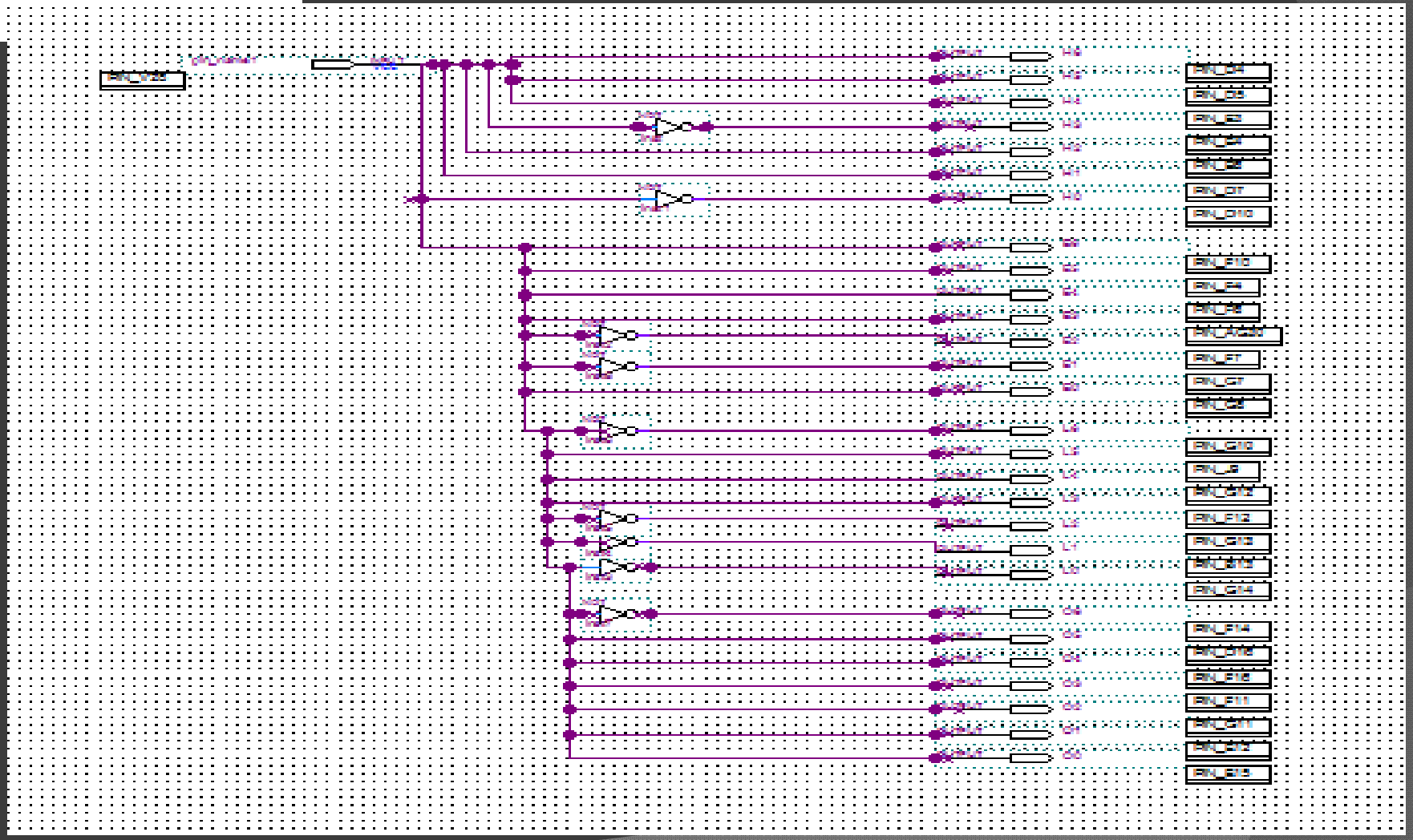
Edits pin assignments 100% 00:00:51

Send to board to see if it all works well

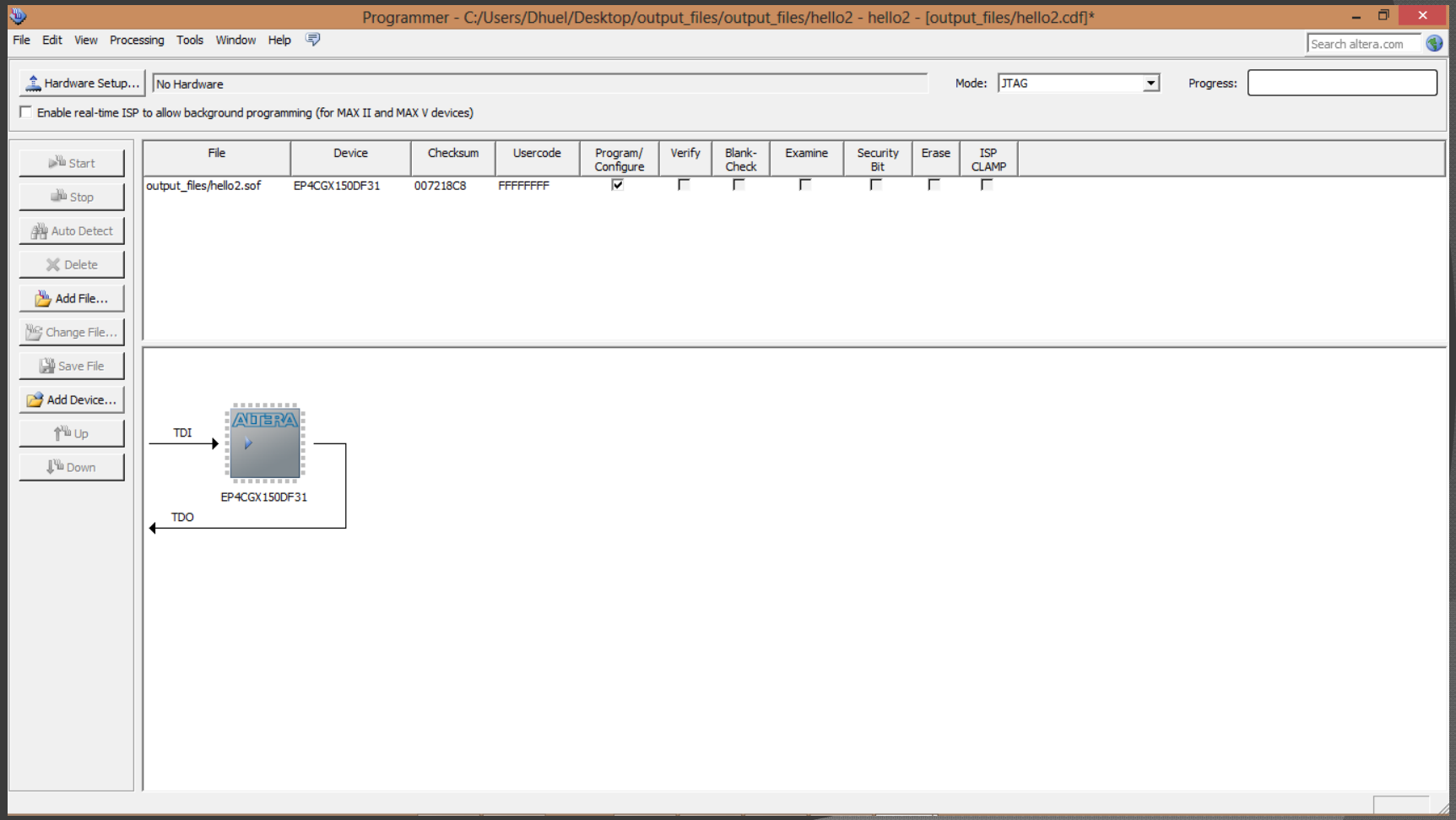




If it works, repeat and reuse



Then we send it all to the board to see the final form



Congratulations, you wrote HELLO using Verilog and schematic diagrams.

In case you missed it

```
module hello (clk, LED, ssOut, ssOut2, ssOut3, ssOut4);
output LED;
input clk;
reg LEDstatus;
reg [23:0] count;
output reg [6:0]ssOut, ssOut2, ssOut3, ssOut4;
reg [2:0] nIn, nIn2, nIn3, nIn4;
assign LED = LEDstatus;

always @(posedge clk) begin
            LEDstatus <= count[23];
            count    <= count + 1;
end
always @(posedge LEDstatus) begin
             nIn  <= nIn + 1;
   case (nIn)
     4'h0: ssOut = 7'b0001001;
     4'h1: ssOut = 7'b0000110;
     4'h2: ssOut = 7'b1000111;
     4'h3: ssOut = 7'b1000111;
    4'h4: ssOut = 7'b1000000;
    4'h5: ssOut = 7'b1111111;
    4'h6: ssOut = 7'b1111111;
    4'h7: ssOut = 7'b1111111;
    4'h8: ssOut = 7'b1111111;
    default: ssOut = 7'b00000000;
    endcase
end
```

```
always @(posedge LEDstatus) begin
        nIn2  <= nIn2 + 1;
    case (nIn2)
          4'h0: ssOut2 = 7'b1111111;
      4'h1: ssOut2 = 7'b0001001;
      4'h2: ssOut2 = 7'b0000110;
                  4'h3: ssOut2 = 7'b1000111;
                  4'h4: ssOut2 = 7'b1000111;
                  4'h5: ssOut2 = 7'b1000000;
                  4'h6: ssOut2 = 7'b1111111;
                  4'h7: ssOut2 = 7'b1111111;
                  4'h8: ssOut2 = 7'b1111111;
                  default: ssOut = 7'b00000000;
                  endcase
end
```

```
always @(posedge LEDstatus) begin
        nIn3  <= nIn3 + 1;
    case (nIn3)
                4'h0: ssOut3 = 7'b1111111;
          4'h1: ssOut3 = 7'b1111111;
      4'h2: ssOut3 = 7'b0001001;
      4'h3: ssOut3 = 7'b0000110;
                4'h4: ssOut3 = 7'b1000111;
                4'h5: ssOut3 = 7'b1000111;
                4'h6: ssOut3 = 7'b1000000;
                4'h7: ssOut3 = 7'b1111111;
                4'h8: ssOut3 = 7'b1111111;
                default: ssOut3 = 7'b00000000;
                endcase
end
```

```
always @(posedge LEDstatus) begin
        nIn4  <= nIn4 + 1;
    case (nIn4)
          4'h0: ssOut4 = 7'b1111111;
                4'h1: ssOut4 = 7'b1111111;
          4'h2: ssOut4 = 7'b1111111;
      4'h3: ssOut4 = 7'b0001001;
      4'h4: ssOut4 = 7'b0000110;
                4'h5: ssOut4 = 7'b1000111;
                4'h6: ssOut4 = 7'b1000111;
                4'h7: ssOut4 = 7'b1000000;
                4'h8: ssOut4 = 7'b1111111;
                default: ssOut4 = 7'b00000000;
                endcase
end
endmodule
```