CONTROL OF ON-BOARD COMPONENTS BY ATOM PROCESSOR THROUGH PCI BUS COMMUNICATION

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Department of Electrical and Computer Engineering
Howard University
Instructor: Dr. Charles Kim

AGENDA

- Introduction
- Setup
- Implementation
- Questions

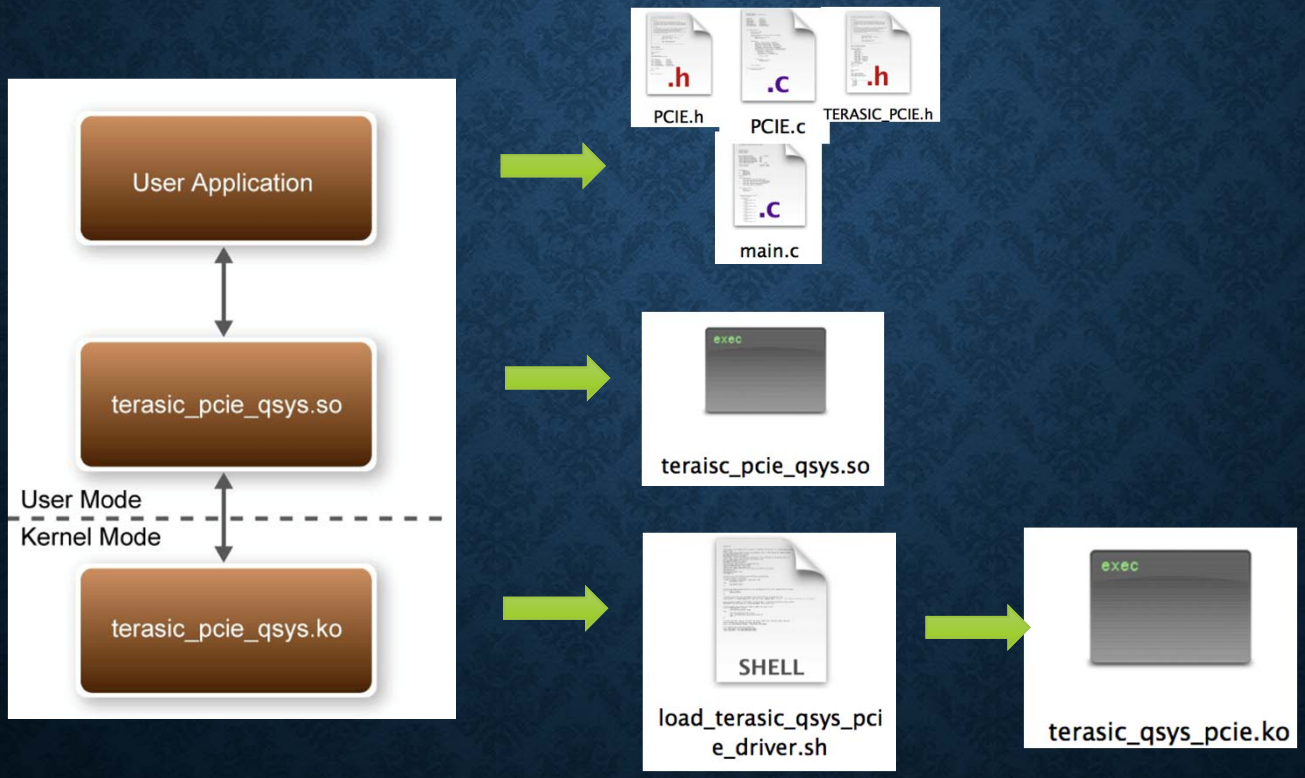
INTRODUCTION

- In the past…
  - Write the program
  - Assign pins
  - Compile
  - Program
  - Use on-board switches or push buttons to control LEDs
- PCIe Bus Communication
  - Write the program
  - Compile
  - Program
  - Use Atom Processor to control LEDs

BACKGROUND ON INTEL ATOM PCI EXPRESS

- PCI Express (PCIe)
- Terasic DE2-i250 has two 1x PCIe links

PCIE FURTHER EXPLAINED

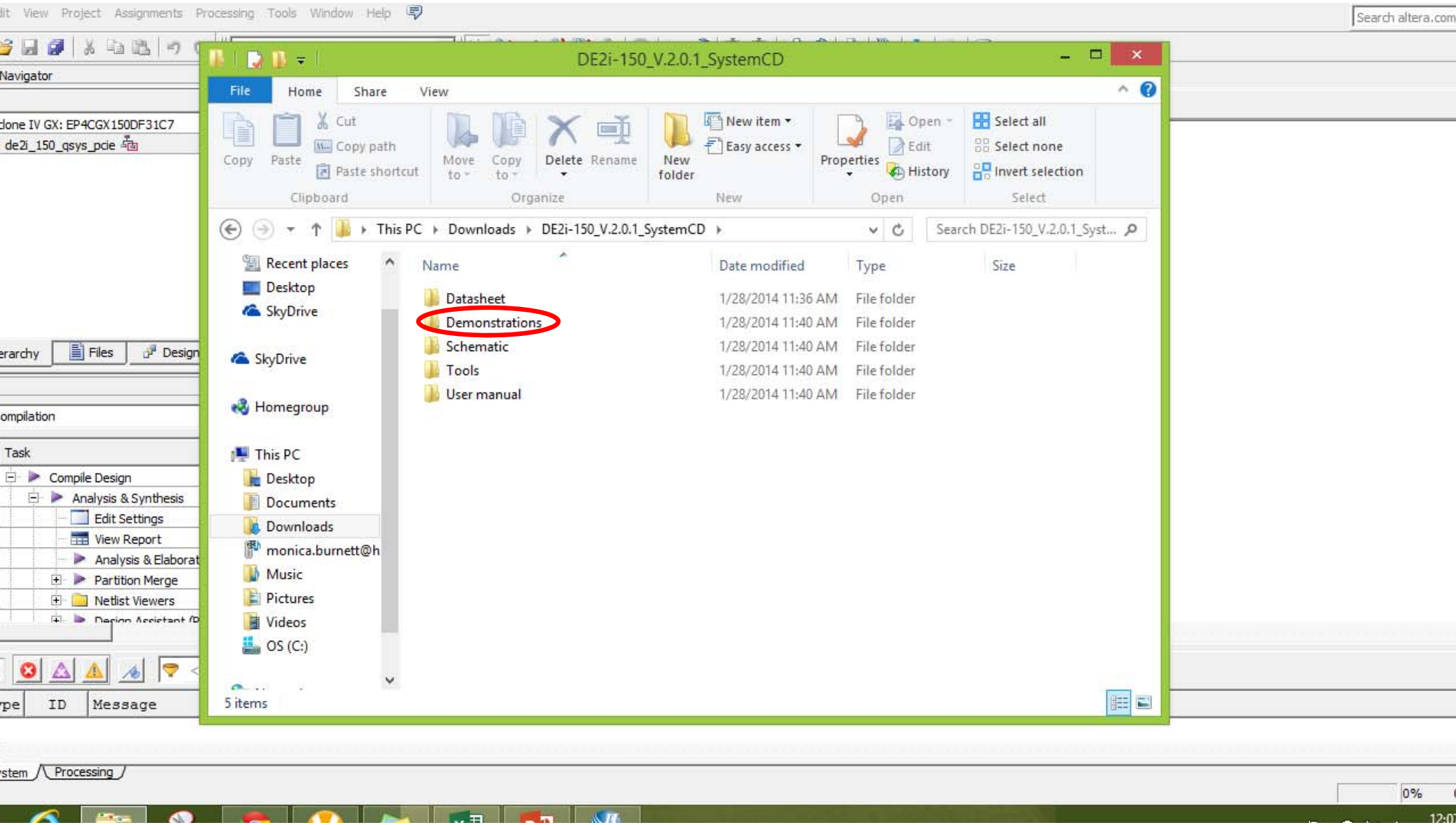


SETUP

- Open DE2i-150 System CD

SETUP

- Open DE2i-150 System CD
- Click Demonstrations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Schematic 1/28/2014 11:40 AM File folder
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User manual 1/28/2014 11:40 AM File folder
5 items
Navigator
Files
Design
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Partition Merge
Netlist Viewers
ID
Message
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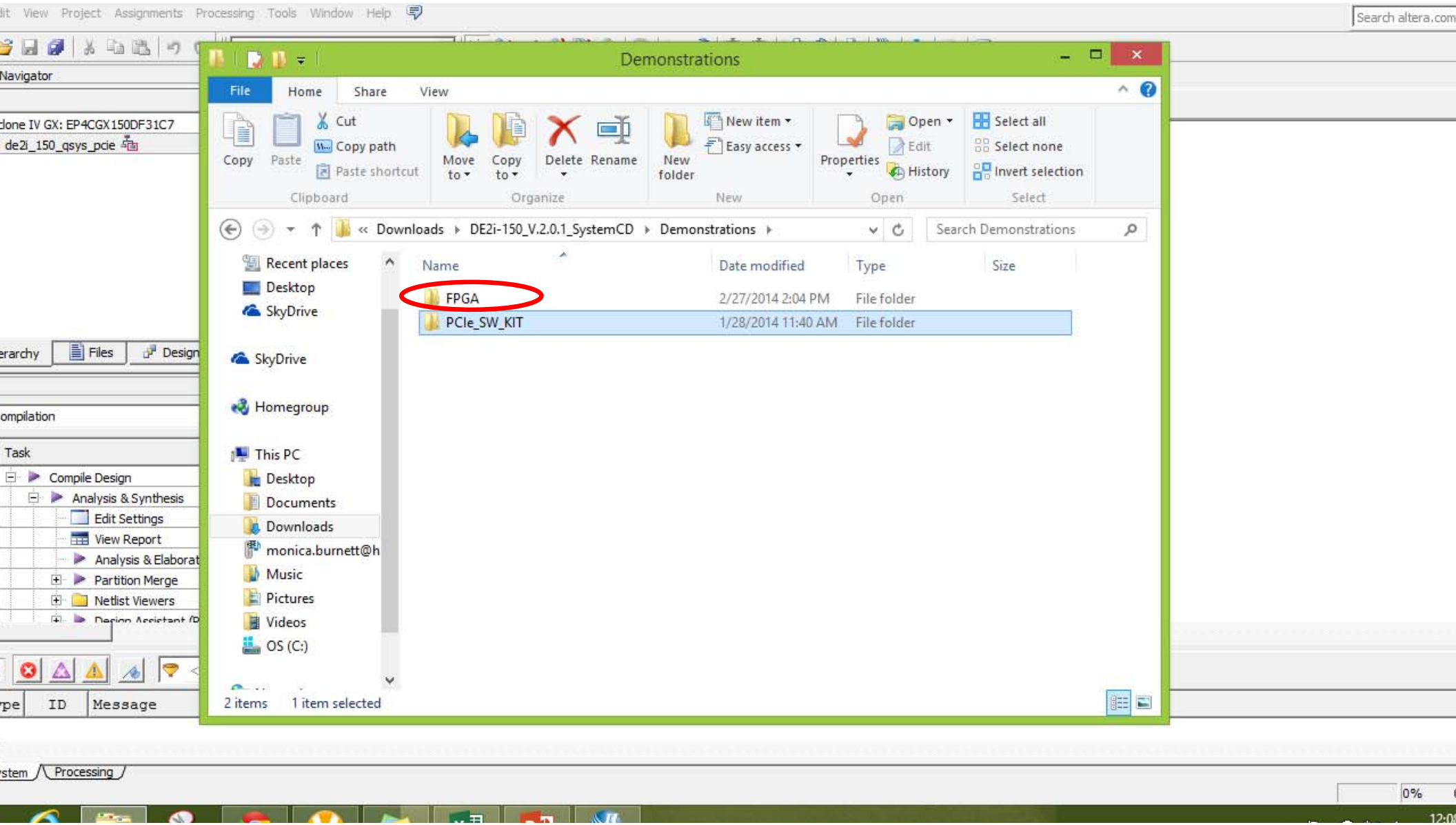
SETUP

- Open DE2i-150 System CD
- Click Demonstrations
- Click FPGA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Music
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FPGA
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PCIe_SW_KIT
1/28/2014 11:40 AM
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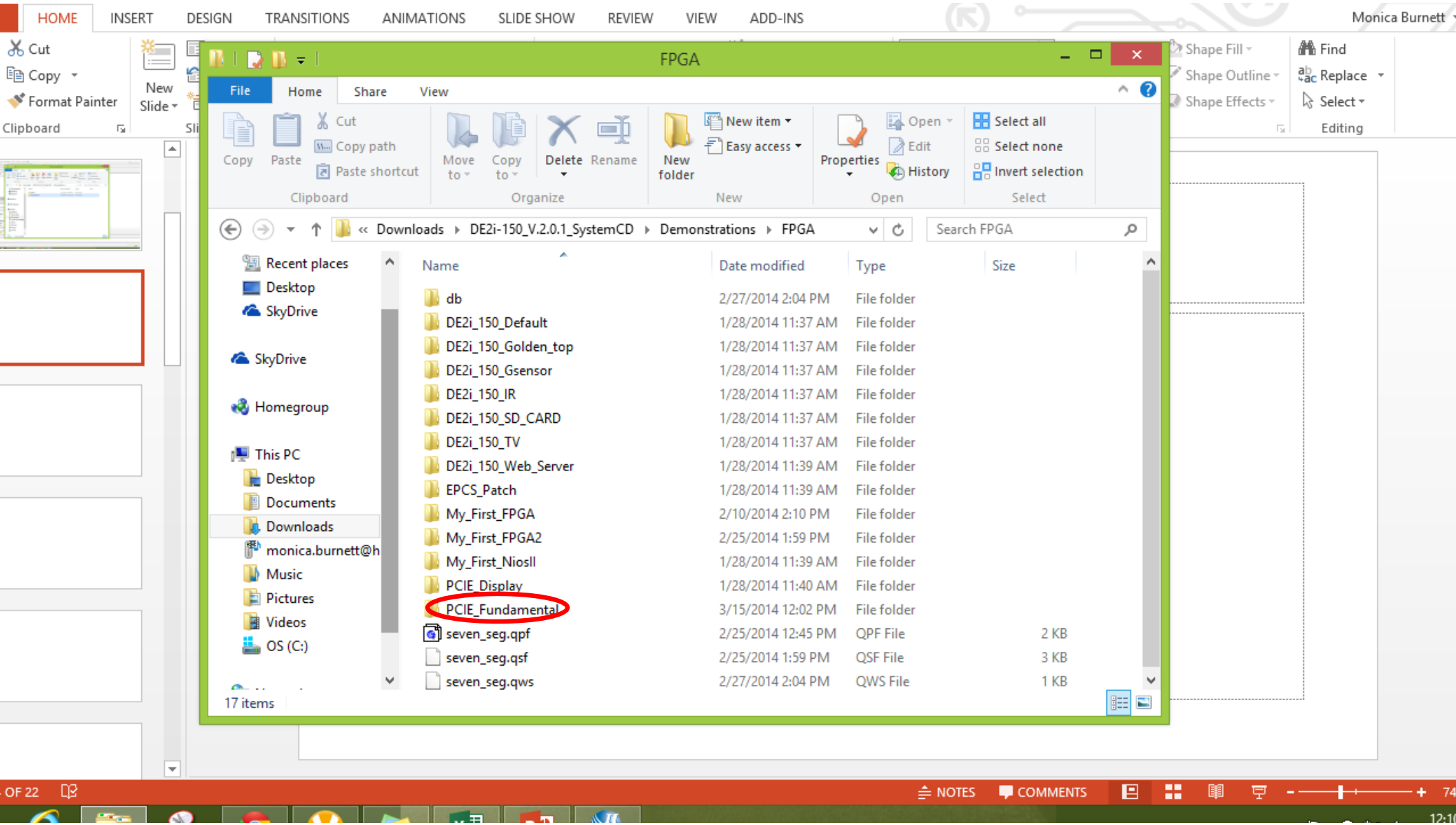
2 items
1 item selected

SETUP

- Open DE2i-150 System CD
- Click Demonstrations
- Click FPGA
- Click PCIe_Fundamental


HOME
INSERT
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ANIMATIONS
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Monica Burnett
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Shape Fill
Shape Outline
Shape Effects
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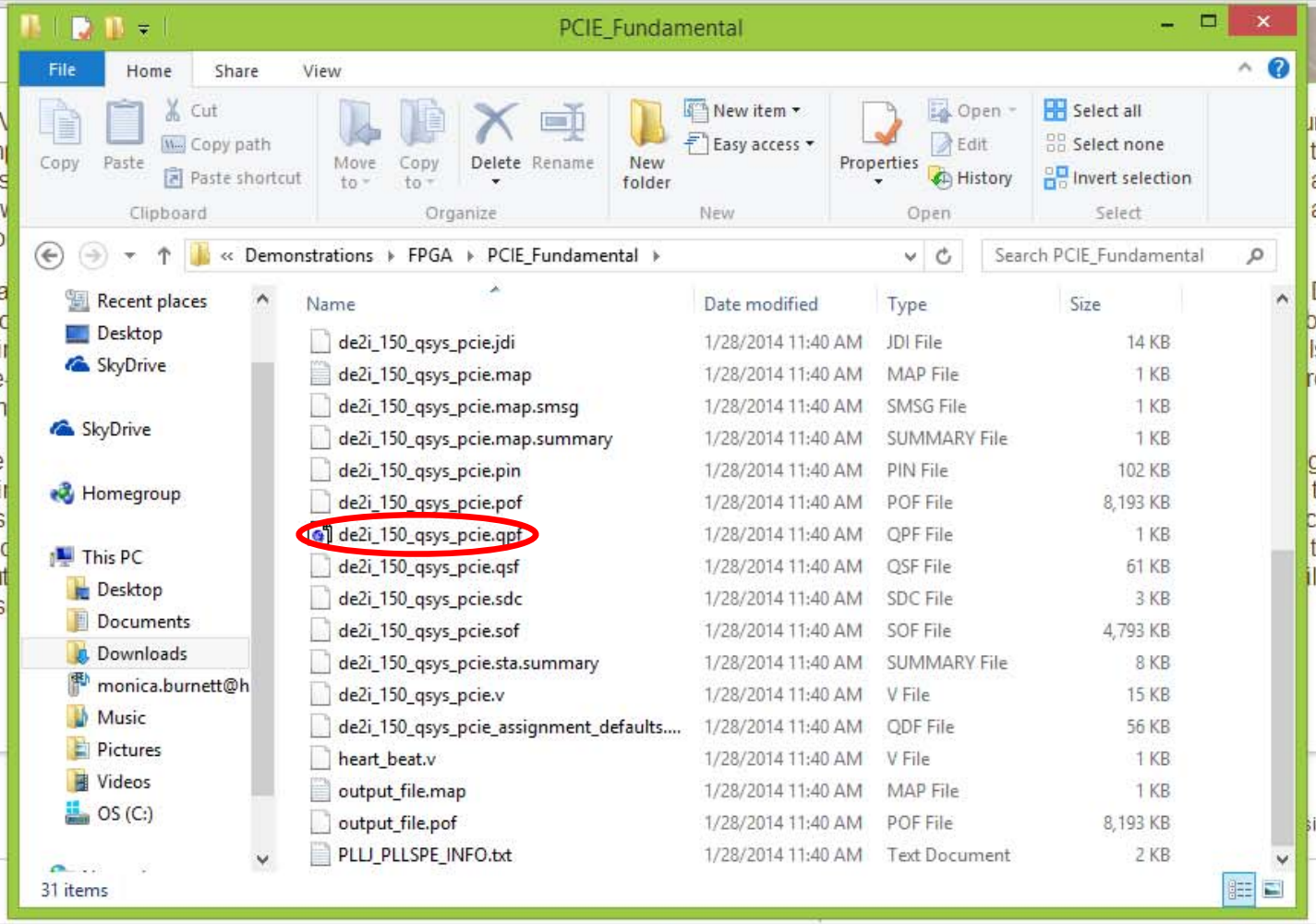
db 2/27/2014 2:04 PM File folder
DE2i_150_Default 1/28/2014 11:37 AM File folder
DE2i_150_Golden_top 1/28/2014 11:37 AM File folder
DE2i_150_Gsensor 1/28/2014 11:37 AM File folder
DE2i_150_IR 1/28/2014 11:37 AM File folder
DE2i_150_SD_CARD 1/28/2014 11:37 AM File folder
DE2i_150_TV 1/28/2014 11:37 AM File folder
DE2i_150_Web_Server 1/28/2014 11:39 AM File folder
EPCS_Patch 1/28/2014 11:39 AM File folder
My_First_FPGA 2/10/2014 2:10 PM File folder
My_First_FPGA2 2/25/2014 1:59 PM File folder
My_First_NiosII 1/28/2014 11:39 AM File folder
PCIE_Display 1/28/2014 11:40 AM File folder
PCIE_Fundamental 3/15/2014 12:02 PM File folder
seven_seg.qpf 2/25/2014 12:45 PM QPF File 2 KB
seven_seg.qsf 2/25/2014 1:59 PM QSF File 3 KB
seven_seg.qws 2/27/2014 2:04 PM QWS File 1 KB
17 items
OF 22
NOTES
COMMENTS

SETUP

- Open DE2i-150 System CD
- Click Demonstrations
- Click FPGA
- Click PCIe_Fundamental
- Click de2i_150_qsys_pcie.qpf


PCIE_Fundamental
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Music
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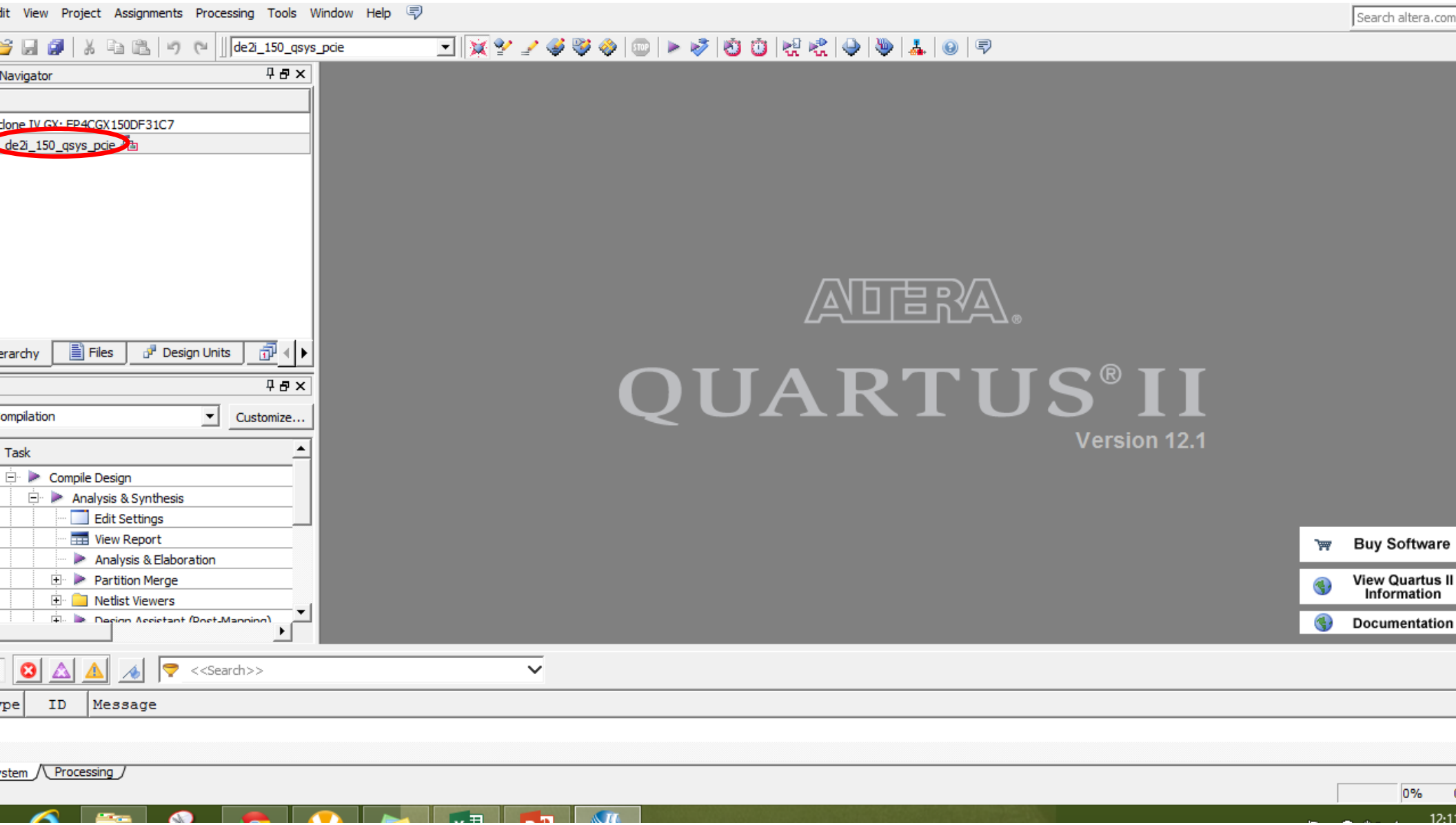
de2i_150_qsys_pcie.jdi 1/28/2014 11:40 AM JDI File 14 KB
de2i_150_qsys_pcie.map 1/28/2014 11:40 AM MAP File 1 KB
de2i_150_qsys_pcie.map.smsg 1/28/2014 11:40 AM SMSG File 1 KB
de2i_150_qsys_pcie.map.summary 1/28/2014 11:40 AM SUMMARY File 1 KB
de2i_150_qsys_pcie.pin 1/28/2014 11:40 AM PIN File 102 KB
de2i_150_qsys_pcie.pof 1/28/2014 11:40 AM POF File 8,193 KB
de2i_150_qsys_pcie.qpf 1/28/2014 11:40 AM QPF File 1 KB
de2i_150_qsys_pcie.qsf 1/28/2014 11:40 AM QSF File 61 KB
de2i_150_qsys_pcie.sdc 1/28/2014 11:40 AM SDC File 3 KB
de2i_150_qsys_pcie.sof 1/28/2014 11:40 AM SOF File 4,793 KB
de2i_150_qsys_pcie.sta.summary 1/28/2014 11:40 AM SUMMARY File 8 KB
de2i_150_qsys_pcie.v 1/28/2014 11:40 AM V File 15 KB
de2i_150_qsys_pcie_assignment_defaults.... 1/28/2014 11:40 AM QDF File 56 KB
heart_beat.v 1/28/2014 11:40 AM V File 1 KB
output_file.map 1/28/2014 11:40 AM MAP File 1 KB
output_file.pof 1/28/2014 11:40 AM POF File 8,193 KB
PLLJ_PLLSPE_INFO.txt 1/28/2014 11:40 AM Text Document 2 KB
31 items


dit View Project Assignments Processing Tools Window Help
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de2i_150_qsys_pcie
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Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
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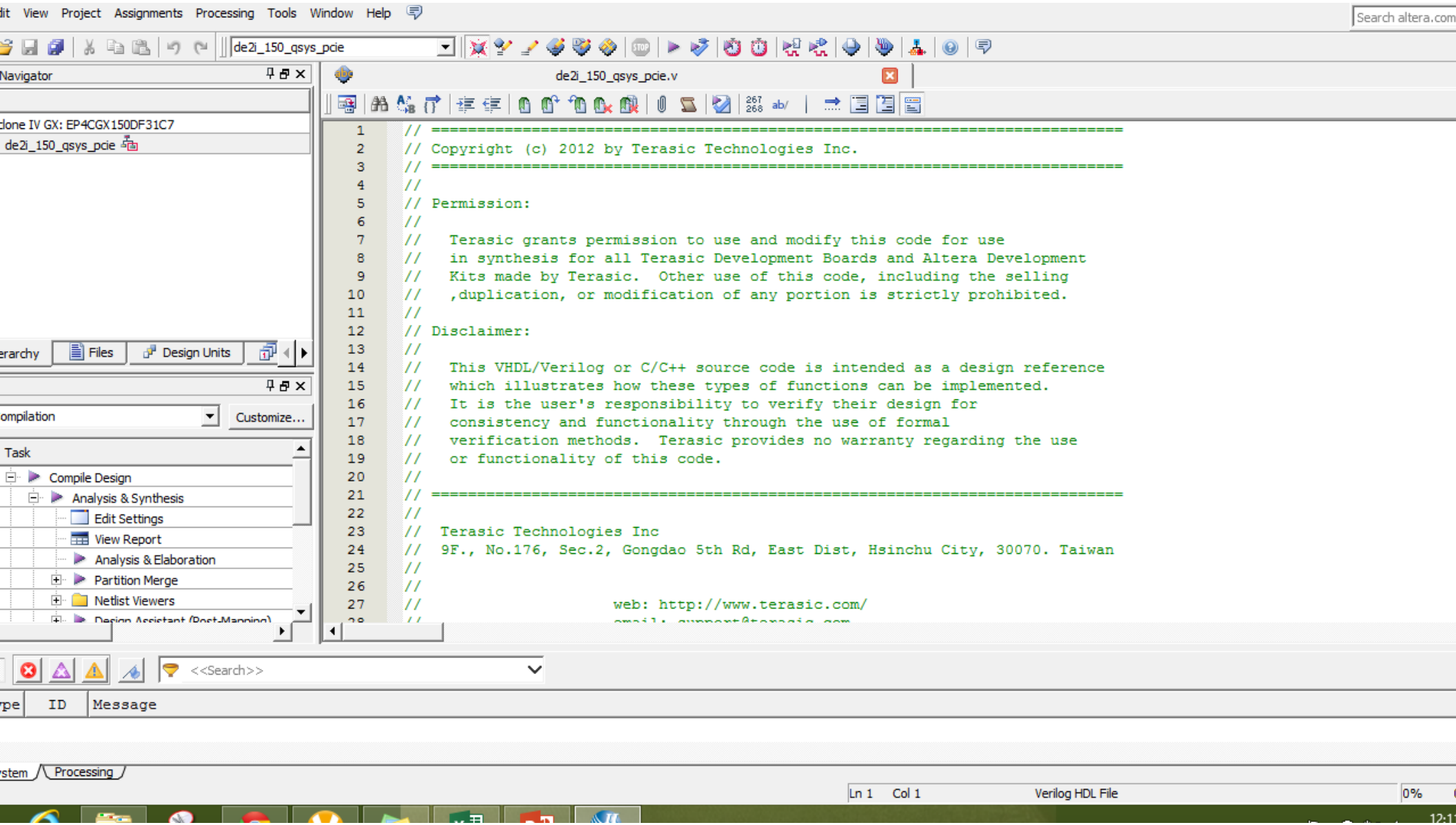
ALTERNATIVES

- You can always write your own code
- You can always use the code as a foundation and build from it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Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
de2i_150_qsys_pcie.v
1 // ==========
2 // Copyright (c) 2012 by Terasic Technologies Inc.
3 // ==========
4 //
5 // Permission:
6 //
7 // Terasic grants permission to use and modify this code for use
8 // in synthesis for all Terasic Development Boards and Altera Development
9 // Kits made by Terasic. Other use of this code, including the selling
10 // ,duplication, or modification of any portion is strictly prohibited.
11 //
12 // Disclaimer:
13 //
14 // This VHDL/Verilog or C/C++ source code is intended as a design reference
15 // which illustrates how these types of functions can be implemented.
16 // It is the user's responsibility to verify their design for
17 // consistency and functionality through the use of formal
18 // verification methods. Terasic provides no warranty regarding the use
19 // or functionality of this code.
20 //
21 // ==========
22 //
23 // Terasic Technologies Inc
24 // 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan
25 //
26 //
27 // web: http://www.terasic.com/
<<Search>>
ID
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Ln 1 Col 1
Verilog HDL File
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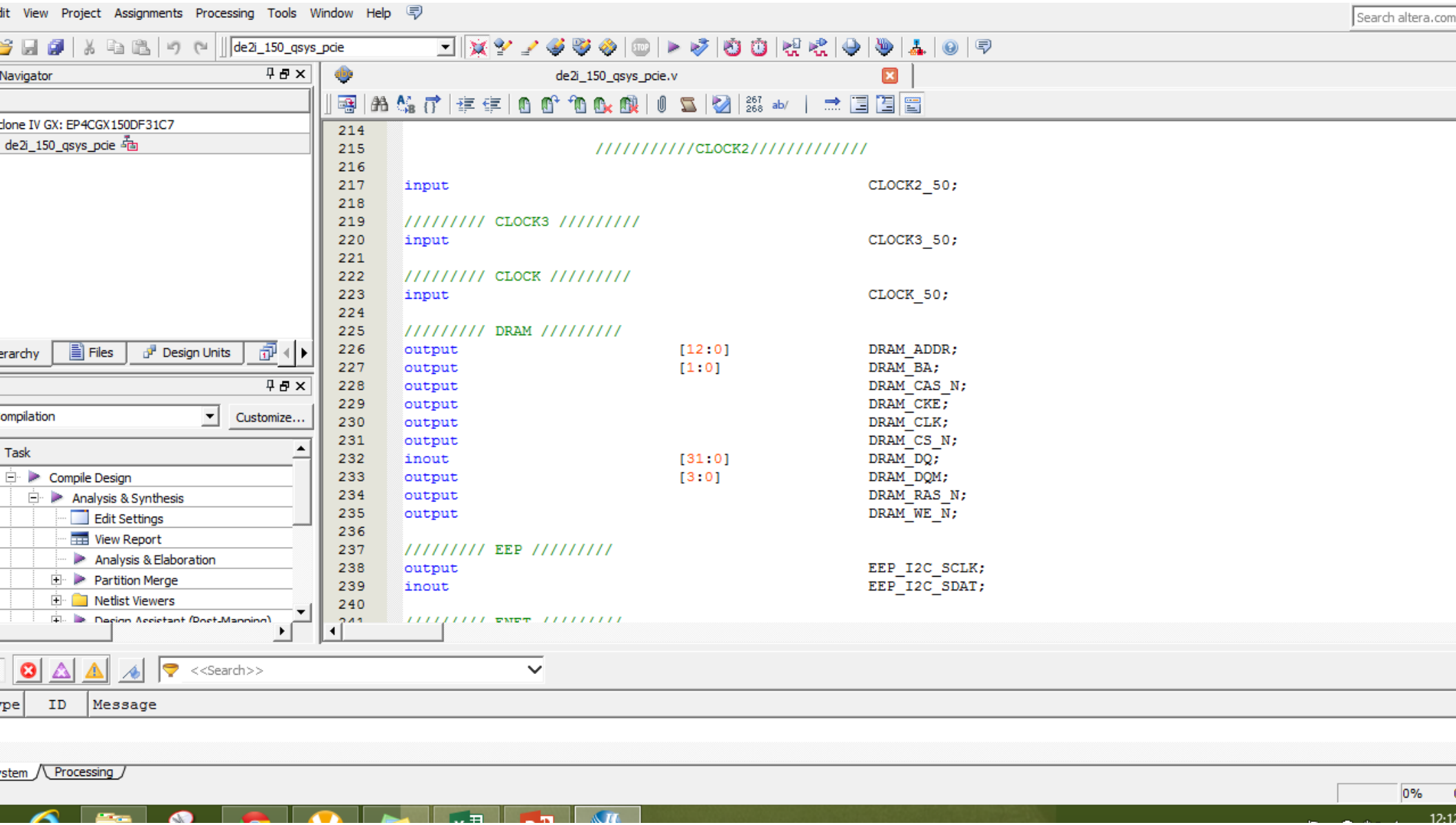
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Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
de2i_150_qsys_pcie.v
214
215 //////////CLOCK2//////////////
216
217 input CLOCK2_50;
218
219 ///////// CLOCK3 /////////
220 input CLOCK3_50;
221
222 ///////// CLOCK /////////
223 input CLOCK_50;
224
225 ///////// DRAM /////////
226 output [12:0] DRAM_ADDR;
227 output [1:0] DRAM_BA;
228 output DRAM_CAS_N;
229 output DRAM_CKE;
230 output DRAM_CLK;
231 output DRAM_CS_N;
232 inout [31:0] DRAM_DQ;
233 output [3:0] DRAM_DQM;
234 output DRAM_RAS_N;
235 output DRAM_WE_N;
236
237 ///////// EEP /////////
238 output EEP_I2C_SCLK;
239 inout EEP_I2C_SDAT;
240
<<Search>>
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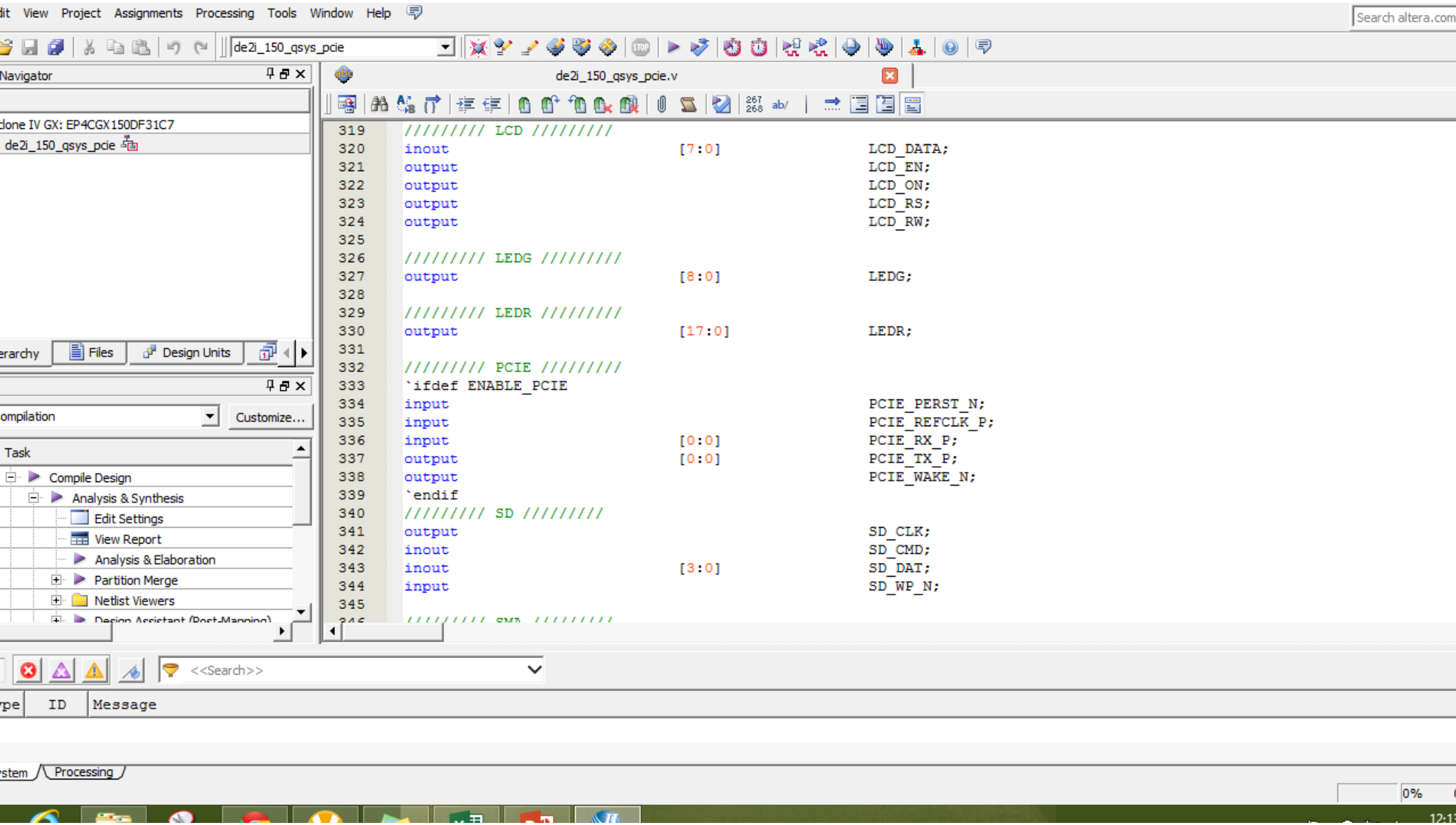
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Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
de2i_150_qsys_pcie.v
319 //////// LCD ////////
320 inout [7:0] LCD_DATA;
321 output LCD_EN;
322 output LCD_ON;
323 output LCD_RS;
324 output LCD_RW;
325
326 //////// LEDG ////////
327 output [8:0] LEDG;
328
329 //////// LEDR ////////
330 output [17:0] LEDR;
331
332 //////// PCIE ////////
333 `ifdef ENABLE_PCIE
334 input PCIE_PERST_N;
335 input PCIE_REFCLK_P;
336 input [0:0] PCIE_RX_P;
337 output [0:0] PCIE_TX_P;
338 output PCIE_WAKE_N;
339 `endif
340 //////// SD ////////
341 output SD_CLK;
342 inout SD_CMD;
343 inout [3:0] SD_DAT;
344 input SD_WP_N;
345
<<Search>>
ID
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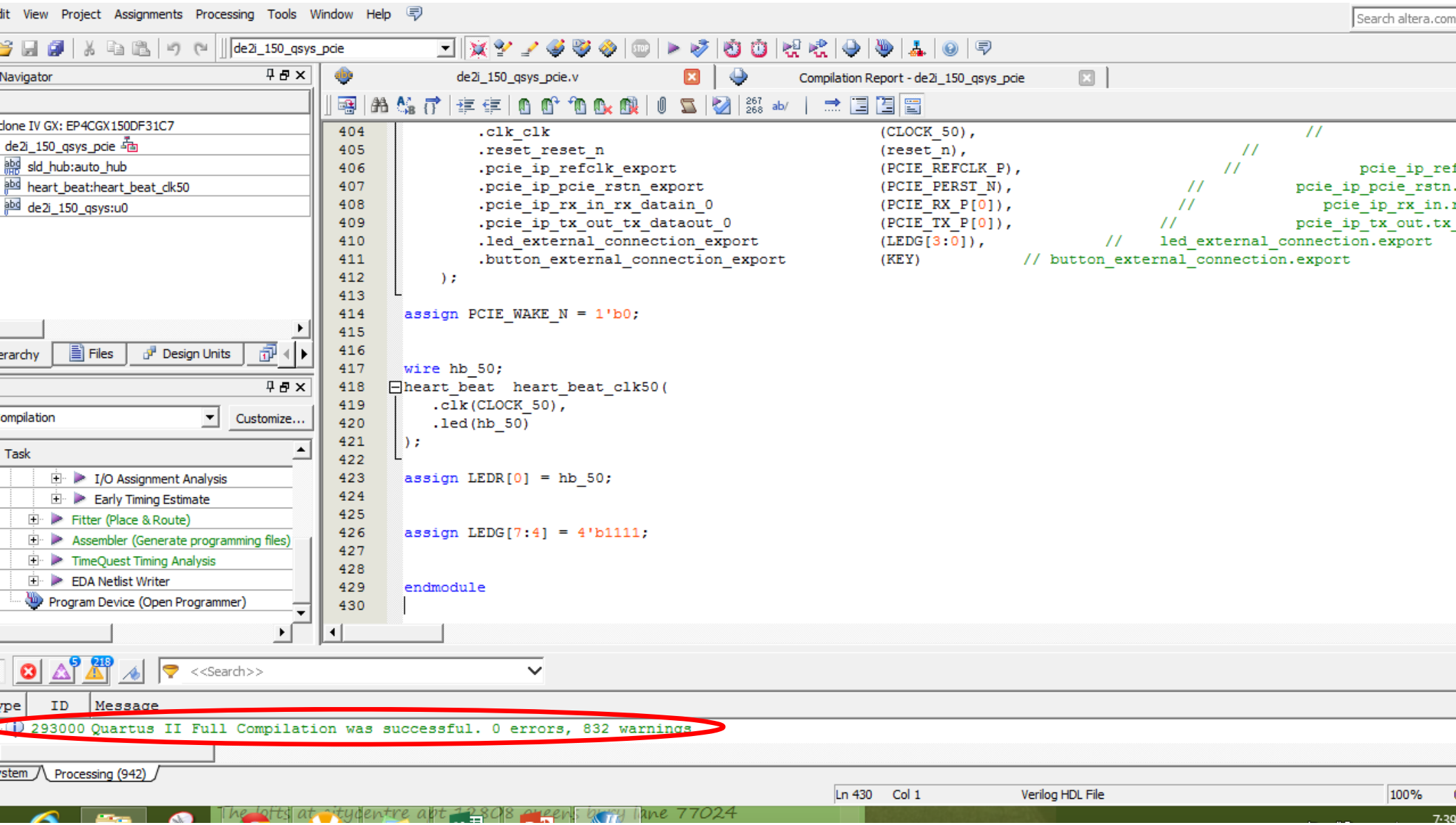
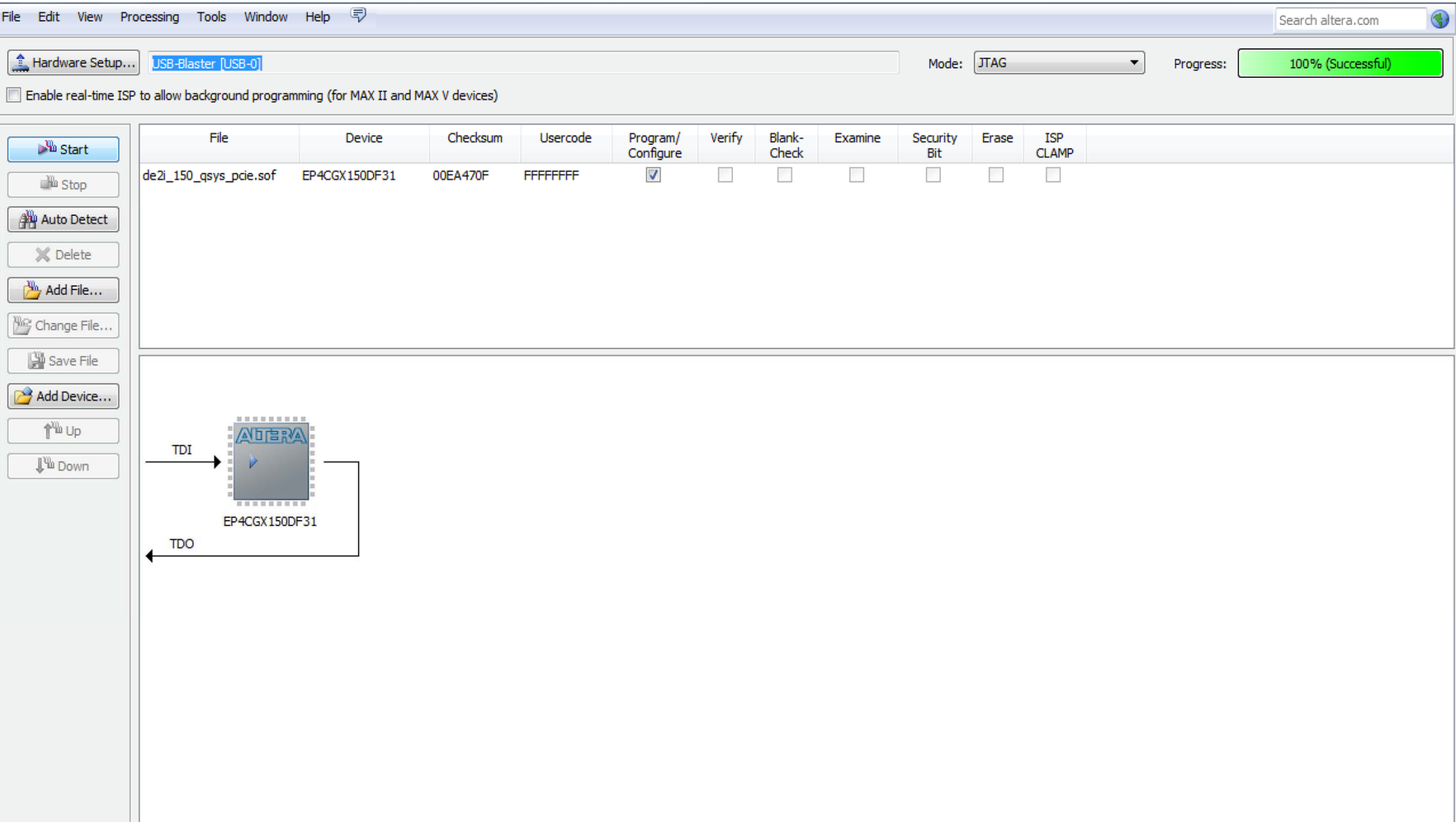

View Project Assignments Processing Tools Window Help
de2i_150_qsys_pcie
Navigator
Cyclone IV GX: EP4CGX150DF31C7
de2i_150_qsys_pcie
sld_hub:auto_hub
heart_beat:heart_beat_clk50
de2i_150_qsys:u0
Files
Design Units
Customize...
Task
I/O Assignment Analysis
Early Timing Estimate
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
de2i_150_qsys_pcie.v
Compilation Report - de2i_150_qsys_pcie
.clk_clk (CLOCK_50),
.reset_reset_n (reset_n),
.pcie_ip_refclk_export (PCIE_REFCLK_P),
.pcie_ip_pcie_rstn_export (PCIE_PERST_N),
.pcie_ip_rx_in_rx_datain_0 (PCIE_RX_P[0]),
.pcie_ip_tx_out_tx_dataout_0 (PCIE_TX_P[0]),
.led_external_connection_export (LEDG[3:0]),
.button_external_connection_export (KEY)
);
assign PCIE_WAKE_N = 1'b0;
wire hb_50;
heart_beat heart_beat_clk50(
.clk(CLOCK_50),
.led(hb_50)
);
assign LEDR[0] = hb_50;
assign LEDG[7:4] = 4'b1111;
endmodule
<<Search>>
Type ID Message
293000 Quartus II Full Compilation was successful. 0 errors, 832 warnings
System Processing (942)
Ln 430 Col 1 Verilog HDL File 100%


File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress: 100% (Successful)
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
de2i_150_qsys_pcie.sof
EP4CGX150DF31
00EA470F
FFFFFFFF
TDI
TDO
EP4CGX150DF31

IMPLEMENTATION

- Connect Atom Board to a monitor
- Use the Yocto OS to communicate with board
- Search for program assigned to board
- Use prompts to control LEDs

```c

#include <stdio.h>
#include <stdlib.h>
#include <memory.h>
#include "PCIE.h"


#define DEMO_PCIE_USER_BAR          PCIE_BAR0
#define DEMO_PCIE_IO_LED_ADDR       0x00
#define DEMO_PCIE_IO_BUTTON_ADDR    0x20
#define DEMO_PCIE_FIFO_WRITE_ADDR   0x40
#define DEMO_PCIE_FIFO_STATUS_ADDR  0x60
#define DEMO_PCIE_FIFO_READ_ADDR    0x80
#define DEMO_PCIE_MEM_ADDR          0x20000

#define MEM_SIZE            (128*1024) //128KB
#define FIFO_SIZE           (16*1024) // 2KBx8



typedef enum{
    MENU_LED = 0,
    MENU_BUTTON,
    MENU_DMA_MEMORY,
    MENU_DMA_FIFO,
    MENU_QUIT = 99
}MENU_ID;

void UI_ShowMenu(void){
    printf("============================\r\n");
    printf("[%d]: Led control\r\n", MENU_LED);
    printf("[%d]: Button Status Read\r\n", MENU_BUTTON);
    printf("[%d]: DMA Memory Test\r\n", MENU_DMA_MEMORY);
    printf("[%d]: DMA FifoTest\r\n", MENU_DMA_FIFO);
    printf("[%d]: Quit\r\n", MENU_QUIT);
    printf("Plesae input your selection:");
}

int UI_UserSelect(void){
    int nSel;
```

```c
int UI_UserSelect(void){
    int nSel;
    scanf("%d",&nSel);
    return nSel;
}


BOOL TEST_LED(PCIE_HANDLE hPCIe){
    BOOL bPass;
    int Mask;

    printf("Please input led conrol mask:");
    scanf("%d", &Mask);

    bPass = PCIE_Write32(hPCIe, DEMO_PCIE_USER_BAR, DEMO_PCIE_IO_LED_ADDR,(DWORD)Mask);
    if (bPass)
        printf("Led control success, mask=%xh\r\n", Mask);
    else
        printf("Led conrol failed\r\n");


    return bPass;
}

BOOL TEST_BUTTON(PCIE_HANDLE hPCIe){
    BOOL bPass = TRUE;
    DWORD Status;

    bPass = PCIE_Read32(hPCIe, DEMO_PCIE_USER_BAR, DEMO_PCIE_IO_BUTTON_ADDR,&Status);
    if (bPass)
        printf("Button status mask:=%xh\r\n", Status);
    else
        printf("Failed to read button status\r\n");


    return bPass;
}

char PAT_GEN(int nIndex){
```

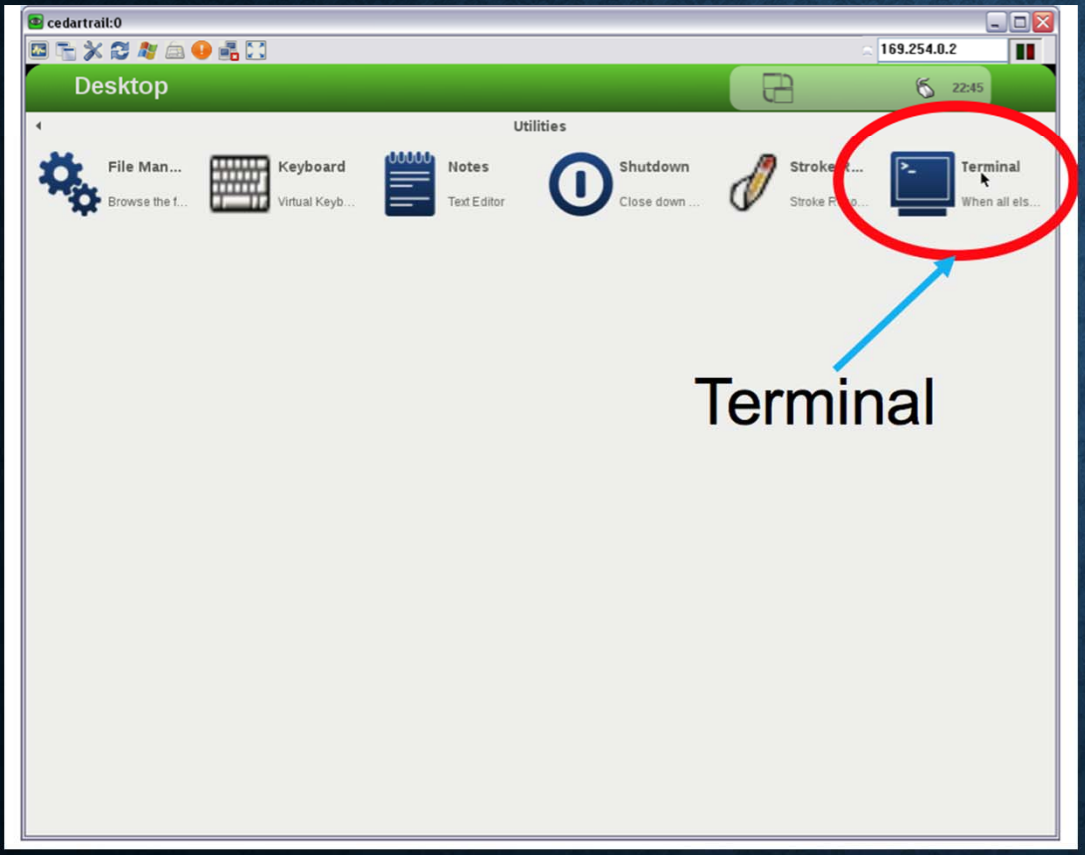
ASSUMPTIONS

- Some general background knowledge using of Linux
- Using Command line
- How to change directories
- How to create, copy, and edit files
- Run applications
- Compile C applications

IMPLEMENTATION ON YOCTO

- Reset Atom Board by hitting button next to Power Cord
- Copy demonstrations files to the Yocto environment
  Easiest way is with a USB flash drive
- Using Terminal navigate to PCIe_DriverInstall folder
  root#: ***cd /home/root/SystemCD/Demonstrations/PCIe_SW_KIT/ linux /PCIe_DriverInstall/***
- Run command root#: ***./load_terasic_qsys_pcie_driver.sh***
- Navigate to folder that contains application files

  root#: ***cd /home/root/SystemCD/Demonstrations/FPGA/PCIE_Fundamentals/linux_app***
- Run app: root@: ***./app***




```
/home/root/projects/Demonstrations/Demonstration
sh-4.2# cd linux_app/
Makefile                PCIE.h                  app
PCIE.c                  TERASIC_PCIE.h          app.c
sh-4.2# cd linux_app/
sh-4.2# ./app
== Terasic: PCIe Demo Program ==
==============================
[0]: Led control
[1]: Button Status Read
[2]: DMA Memory Test
[3]: DMA FifoTest
[99]: Quit
Plesae input your selection:0
Please input led conrol mask:5
Led control success, mask=5h
==============================
[0]: Led control
[1]: Button Status Read
[2]: DMA Memory Test
[3]: DMA FifoTest
[99]: Quit
Plesae input your selection:5
Invalid selection
==============================
[0]: Led control
[1]: Button Status Read
[2]: DMA Memory Test
[3]: DMA FifoTest
[99]: Quit
Plesae input your selection:99
Bye!
sh-4.2#
```

MODIFYING PCIE_FUNDAMENTALS

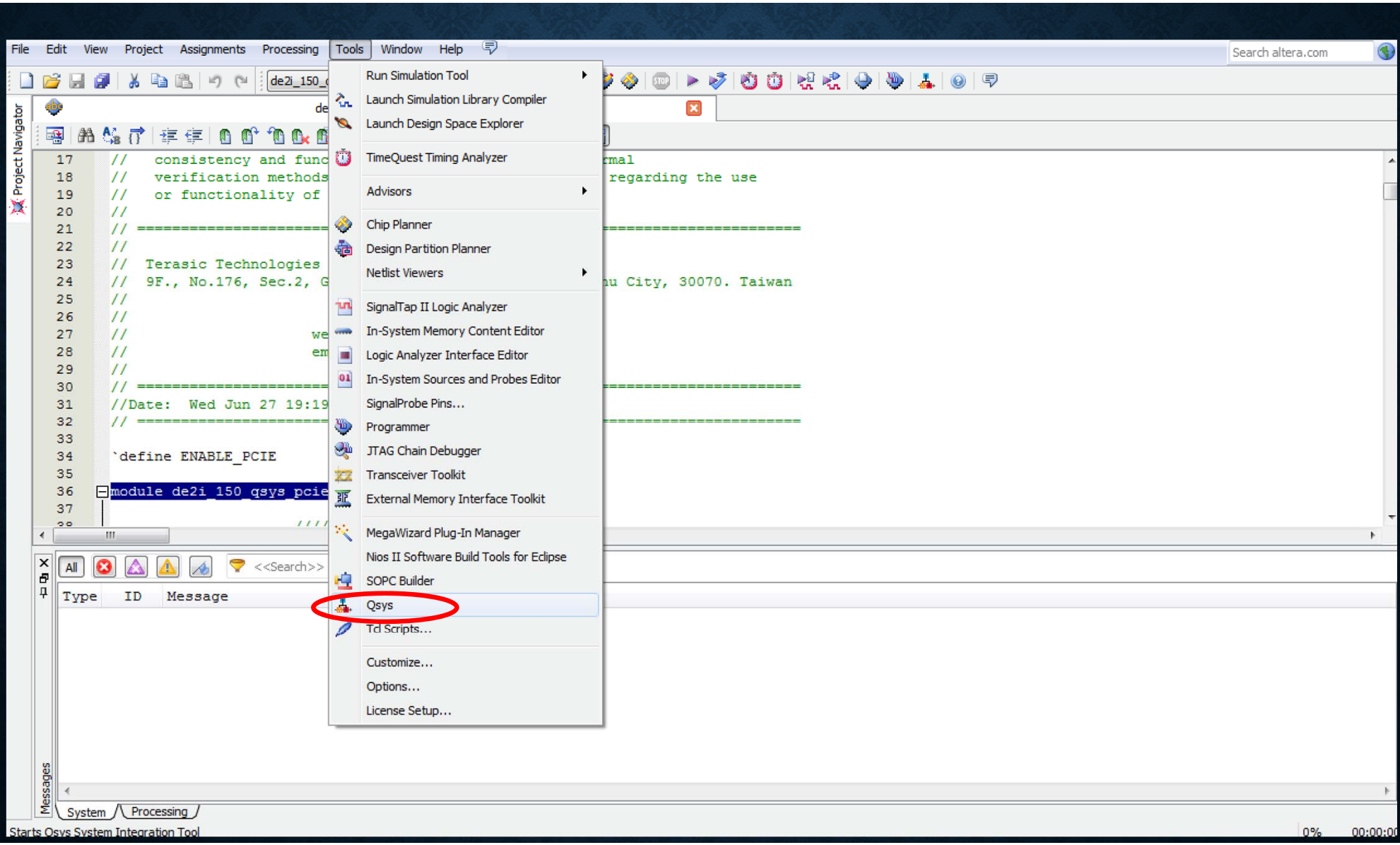
- Modifying the existing PCIe example to control the seven segment display
- Modify/add components to the existing Qsys File
- Modifying Verilog code to include new components
- Modify existing C application
- Program FPGA Board
- Compile and run program

IMPLEMENTATION

- Copy current PCIE_Fundamentals Folder
- Open project in Quartus II

WHY REUSE CODE?

- Sometimes easier to learn
- Most difficult parts already created
- Save time
- For PCIe example code uses shared object files and libraries that link to a kernel file
- Some things are difficult to recreate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Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
JTAG Chain Debugger
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
SOPC Builder
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Tcl Scripts...
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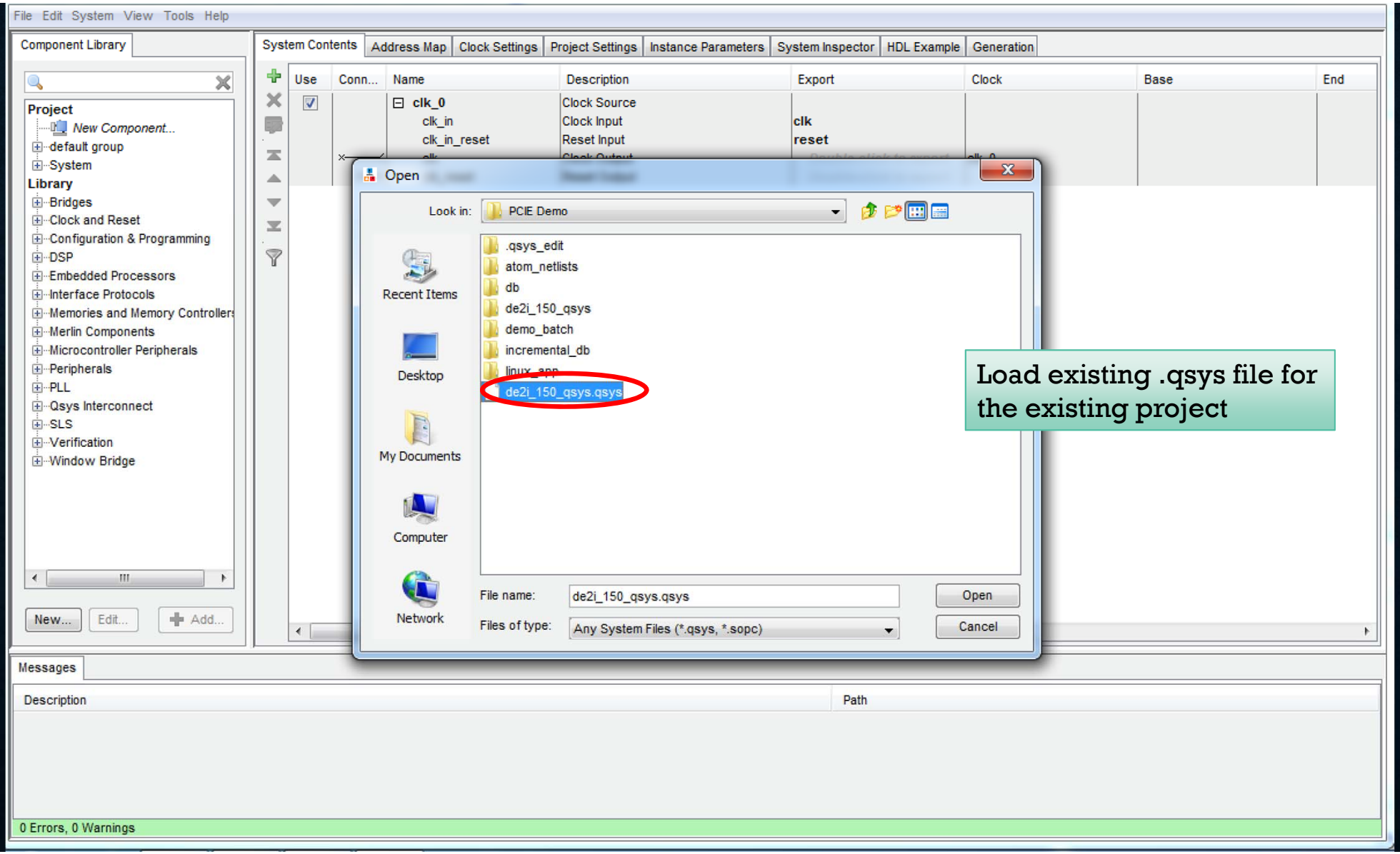
Starts Qsys System Integration Tool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Component Library
Project
New Component...
default group
System
Library
Bridges
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
Memories and Memory Controllers
Merlin Components
Microcontroller Peripherals
Peripherals
PLL
Qsys Interconnect
SLS
Verification
Window Bridge
New...
Edit...
Add...
System Contents
Address Map
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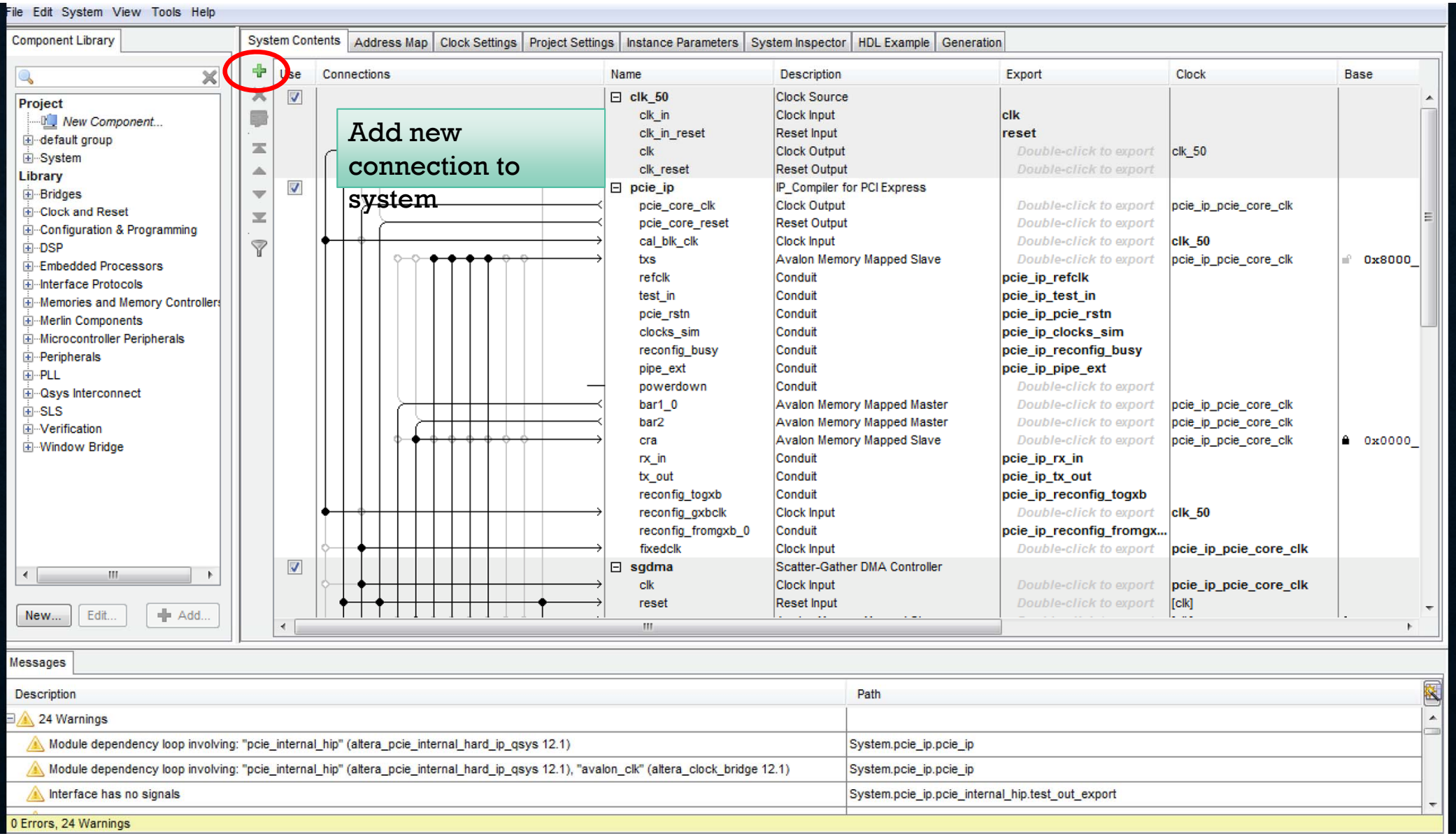
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Conn...
Name
Description
Export
Clock
Base
End
clk_0
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
Open
Look in:
PCIE Demo
Recent Items
Desktop
My Documents
Computer
Network
.qsys_edit
atom_netlists
db
de2i_150_qsys
demo_batch
incremental_db
de2i_150_qsys.qsys
File name:
de2i_150_qsys.qsys
Files of type:
Any System Files (*.qsys, *.sopc)
Open
Cancel
Load existing .qsys file for the existing project
Messages
Description
Path
0 Errors, 0 Warnings


File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
Add new connection to system
Project
New Component...
default group
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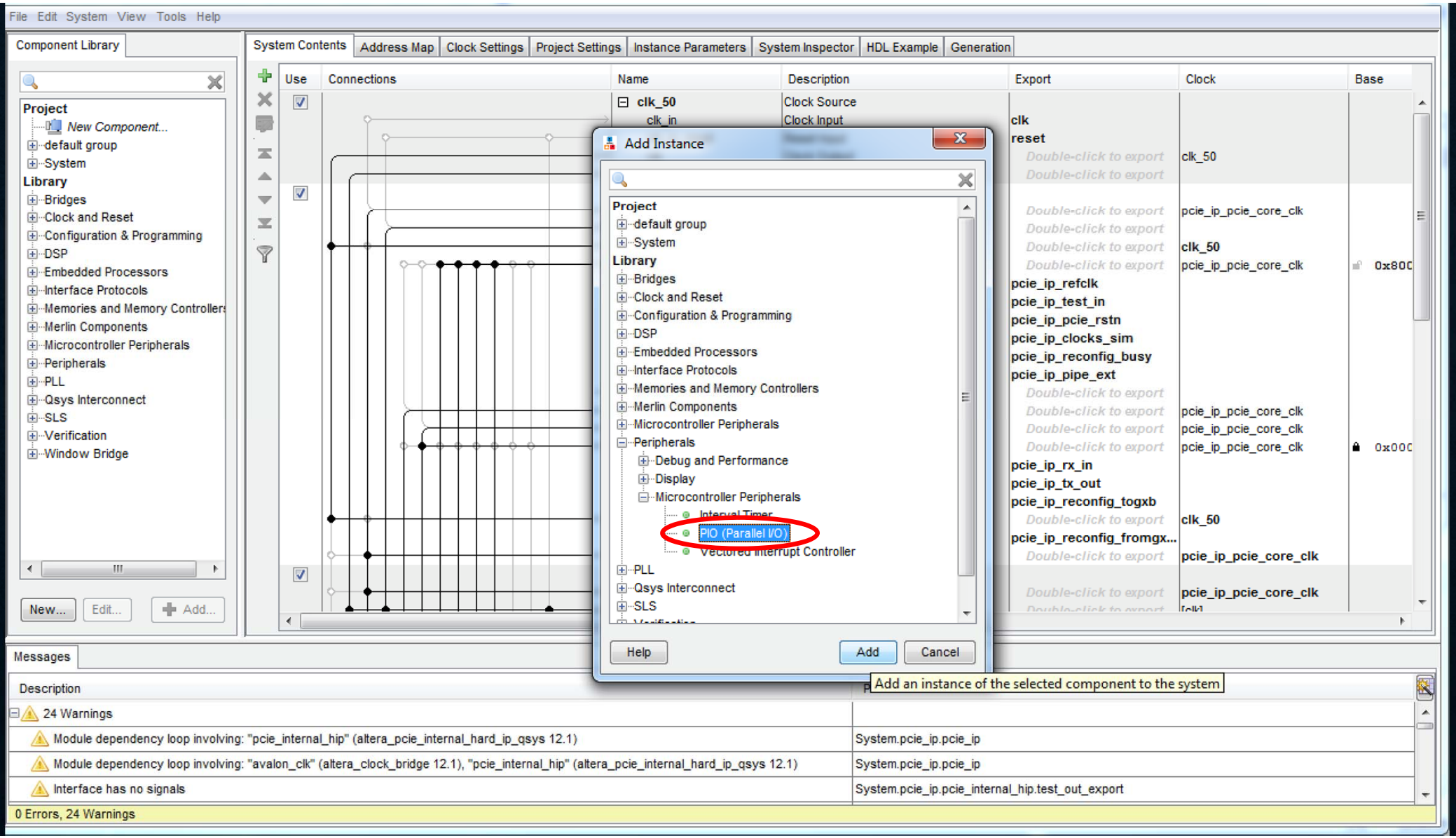
Verification
Window Bridge
New...
Edit...
Add...
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
Double-click to export
clk_50
clk_reset
Reset Output
Double-click to export
pcie_ip
IP_Compiler for PCI Express
pcie_core_clk
Clock Output
Double-click to export
pcie_ip_pcie_core_clk
pcie_core_reset
Reset Output
Double-click to export
cal_blk_clk
Clock Input
Double-click to export
clk_50
txs
Avalon Memory Mapped Slave
Double-click to export
pcie_ip_pcie_core_clk
0x8000_
refclk
Conduit
pcie_ip_refclk
test_in
Conduit
pcie_ip_test_in
pcie_rstn
Conduit
pcie_ip_pcie_rstn
clocks_sim
Conduit
pcie_ip_clocks_sim
reconfig_busy
Conduit
pcie_ip_reconfig_busy
pipe_ext
Conduit
pcie_ip_pipe_ext
powerdown
Conduit
Double-click to export
bar1_0
Avalon Memory Mapped Master
Double-click to export
pcie_ip_pcie_core_clk
bar2
Avalon Memory Mapped Master
Double-click to export
pcie_ip_pcie_core_clk
cra
Avalon Memory Mapped Slave
Double-click to export
pcie_ip_pcie_core_clk
0x0000_
rx_in
Conduit
pcie_ip_rx_in
tx_out
Conduit
pcie_ip_tx_out
reconfig_togxb
Conduit
pcie_ip_reconfig_togxb
reconfig_gxbclk
Clock Input
Double-click to export
clk_50
reconfig_fromgxb_0
Conduit
pcie_ip_reconfig_fromgx...
fixedclk
Clock Input
Double-click to export
pcie_ip_pcie_core_clk
sgdma
Scatter-Gather DMA Controller
clk
Clock Input
Double-click to export
pcie_ip_pcie_core_clk
reset
Reset Input
Double-click to export
[clk]
Messages
Description
Path
24 Warnings
Module dependency loop involving: "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1)
System.pcie_ip.pcie_ip
Module dependency loop involving: "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1), "avalon_clk" (altera_clock_bridge 12.1)
System.pcie_ip.pcie_ip
Interface has no signals
System.pcie_ip.pcie_internal_hip.test_out_export
0 Errors, 24 Warnings


File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
Add Instance
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default group
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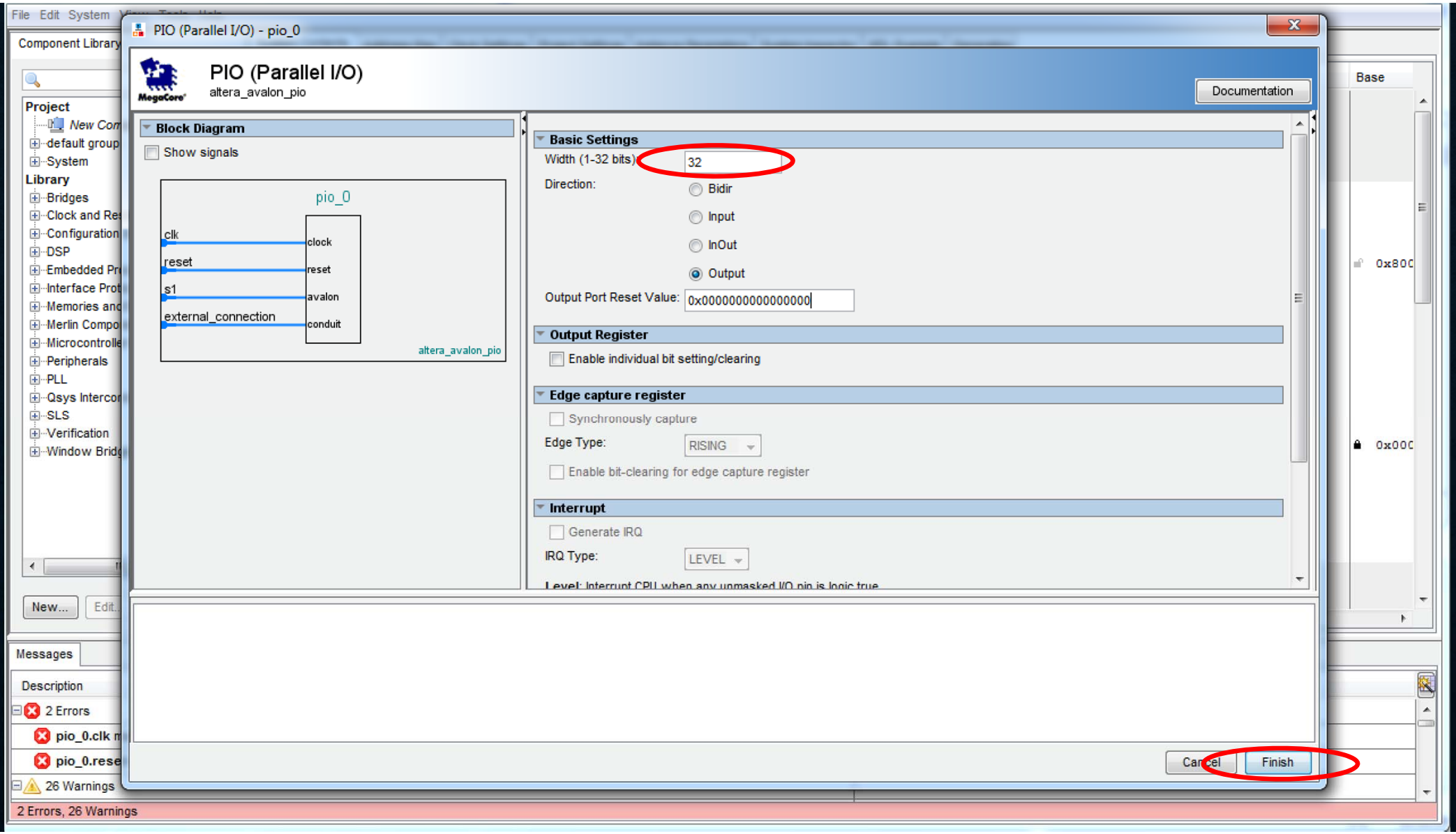
Peripherals
Debug and Performance
Display
Microcontroller Peripherals
PIO (Parallel I/O)
PLL
Qsys Interconnect
SLS
Help
Add
Cancel
Add an instance of the selected component to the system
Messages
Description
24 Warnings
Module dependency loop involving: "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1)
Module dependency loop involving: "avalon_clk" (altera_clock_bridge 12.1), "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1)
Interface has no signals
System.pcie_ip.pcie_ip
System.pcie_ip.pcie_ip
System.pcie_ip.pcie_internal_hip.test_out_export
0 Errors, 24 Warnings


File Edit System
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Clock and Re
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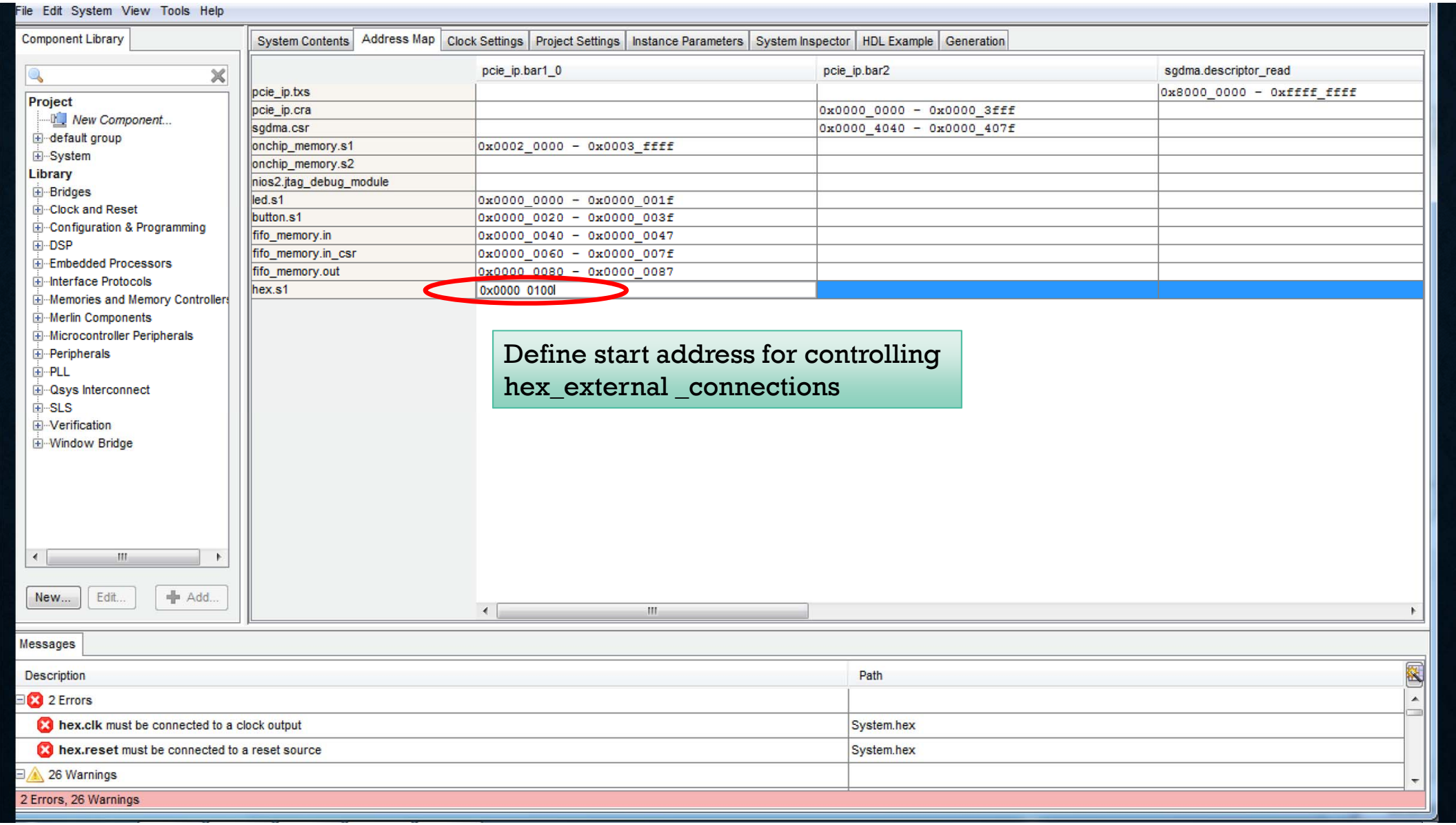
DSP
Embedded Pr
Interface Prot
Memories and
Merlin Compo
Microcontrolle
Peripherals
PLL
Qsys Intercor
SLS
Verification
Window Bridg
New...
Edit...
Base
0x800
0x000
Messages
Description
2 Errors
pio_0.clk
pio_0.rese
26 Warnings
2 Errors, 26 Warnings
PIO (Parallel I/O) - pio_0
PIO (Parallel I/O)
altera_avalon_pio
MegaCore
Documentation
Block Diagram
Show signals
pio_0
clk
reset
s1
external_connection
clock
reset
avalon
conduit
altera_avalon_pio
Basic Settings
Width (1-32 bits)
32
Direction:
Bidir
Input
InOut
Output
Output Port Reset Value:
0x0000000000000000
Output Register
Enable individual bit setting/clearing
Edge capture register
Synchronously capture
Edge Type:
RISING
Enable bit-clearing for edge capture register
Interrupt
Generate IRQ
IRQ Type:
LEVEL
Level: Interrupt CPU when any unmasked I/O pin is logic true
Cancel
Finish


File Edit System View Tools Help
Component Library
Project
New Component...
default group
System
Library
Bridges
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
Memories and Memory Controllers
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Peripherals
PLL
Qsys Interconnect
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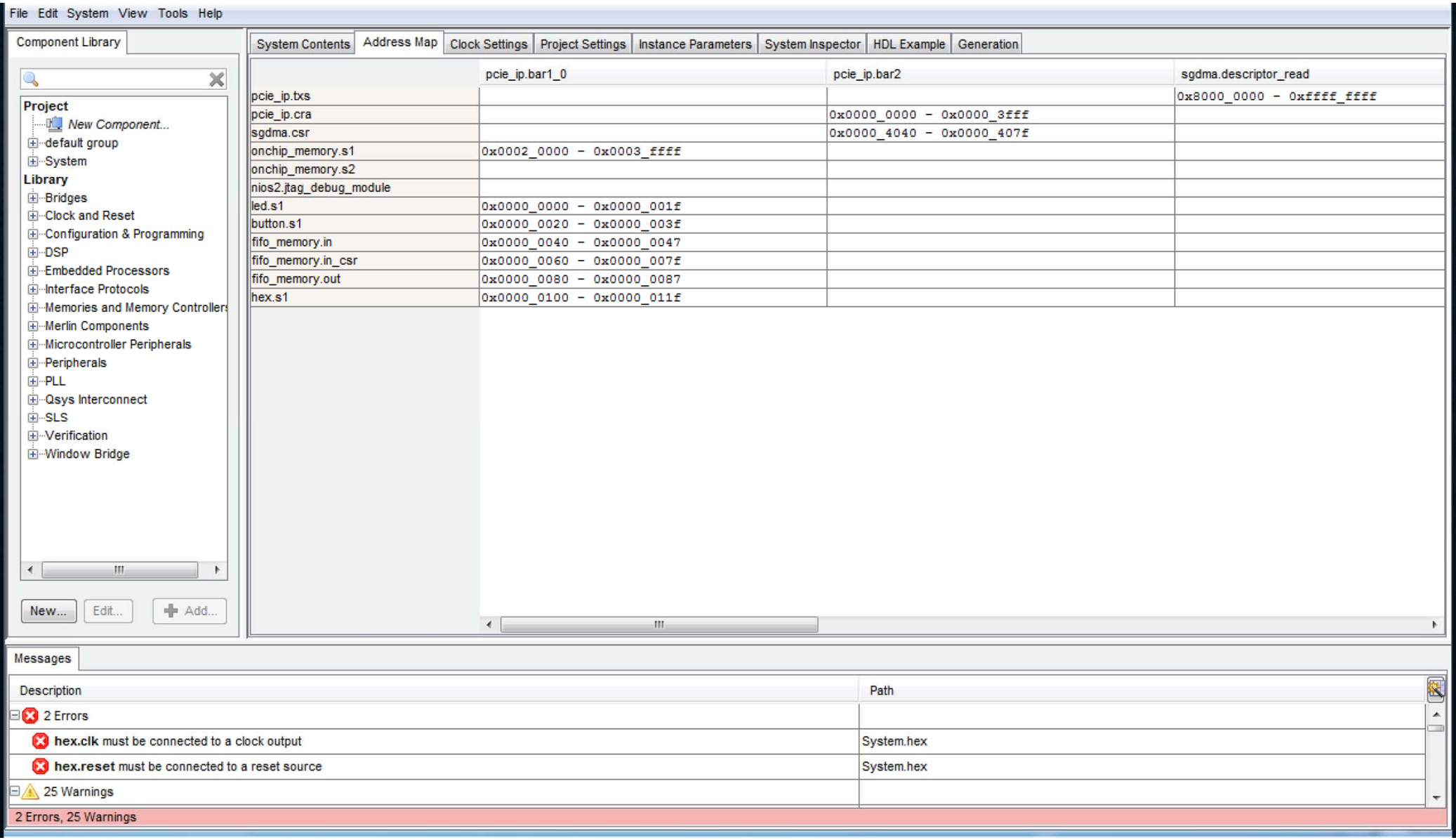
Verification
Window Bridge
New...
Edit...
Add...
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
pcie_ip.bar1_0
pcie_ip.bar2
sgdma.descriptor_read
pcie_ip.txs
0x8000_0000 - 0xffff_ffff
pcie_ip.cra
0x0000_0000 - 0x0000_3fff
sgdma.csr
0x0000_4040 - 0x0000_407f
onchip_memory.s1
0x0002_0000 - 0x0003_ffff
onchip_memory.s2
nios2.jtag_debug_module
led.s1
0x0000_0000 - 0x0000_001f
button.s1
0x0000_0020 - 0x0000_003f
fifo_memory.in
0x0000_0040 - 0x0000_0047
fifo_memory.in_csr
0x0000_0060 - 0x0000_007f
fifo_memory.out
0x0000_0080 - 0x0000_0087
hex.s1
0x0000_0100
Define start address for controlling hex_external _connections
Messages
Description
Path
2 Errors
hex.clk must be connected to a clock output
System.hex
hex.reset must be connected to a reset source
System.hex
26 Warnings
2 Errors, 26 Warnings


File Edit System View Tools Help
Component Library
Project
New Component...
default group
System
Library
Bridges
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
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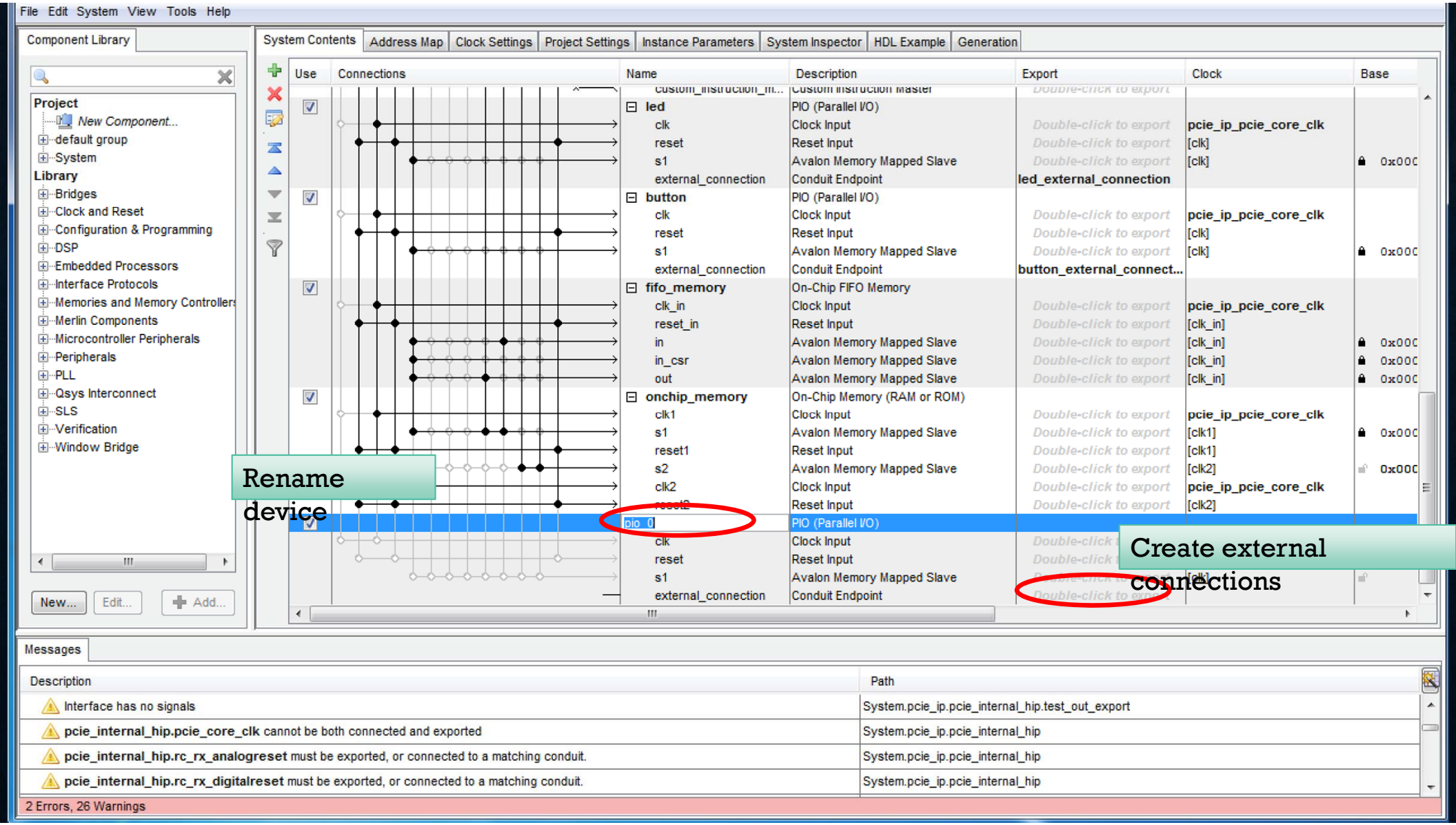
Window Bridge
New...
Edit...
Add...
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
pcie_ip.bar1_0
pcie_ip.bar2
sgdma.descriptor_read
pcie_ip.txs
0x8000_0000 - 0xffff_ffff
pcie_ip.cra
0x0000_0000 - 0x0000_3fff
sgdma.csr
0x0000_4040 - 0x0000_407f
onchip_memory.s1
0x0002_0000 - 0x0003_ffff
onchip_memory.s2
nios2.jtag_debug_module
led.s1
0x0000_0000 - 0x0000_001f
button.s1
0x0000_0020 - 0x0000_003f
fifo_memory.in
0x0000_0040 - 0x0000_0047
fifo_memory.in_csr
0x0000_0060 - 0x0000_007f
fifo_memory.out
0x0000_0080 - 0x0000_0087
hex.s1
0x0000_0100 - 0x0000_011f
Messages
Description
Path
2 Errors
hex.clk must be connected to a clock output
System.hex
hex.reset must be connected to a reset source
System.hex
25 Warnings
2 Errors, 25 Warnings


File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
Project
New Component...
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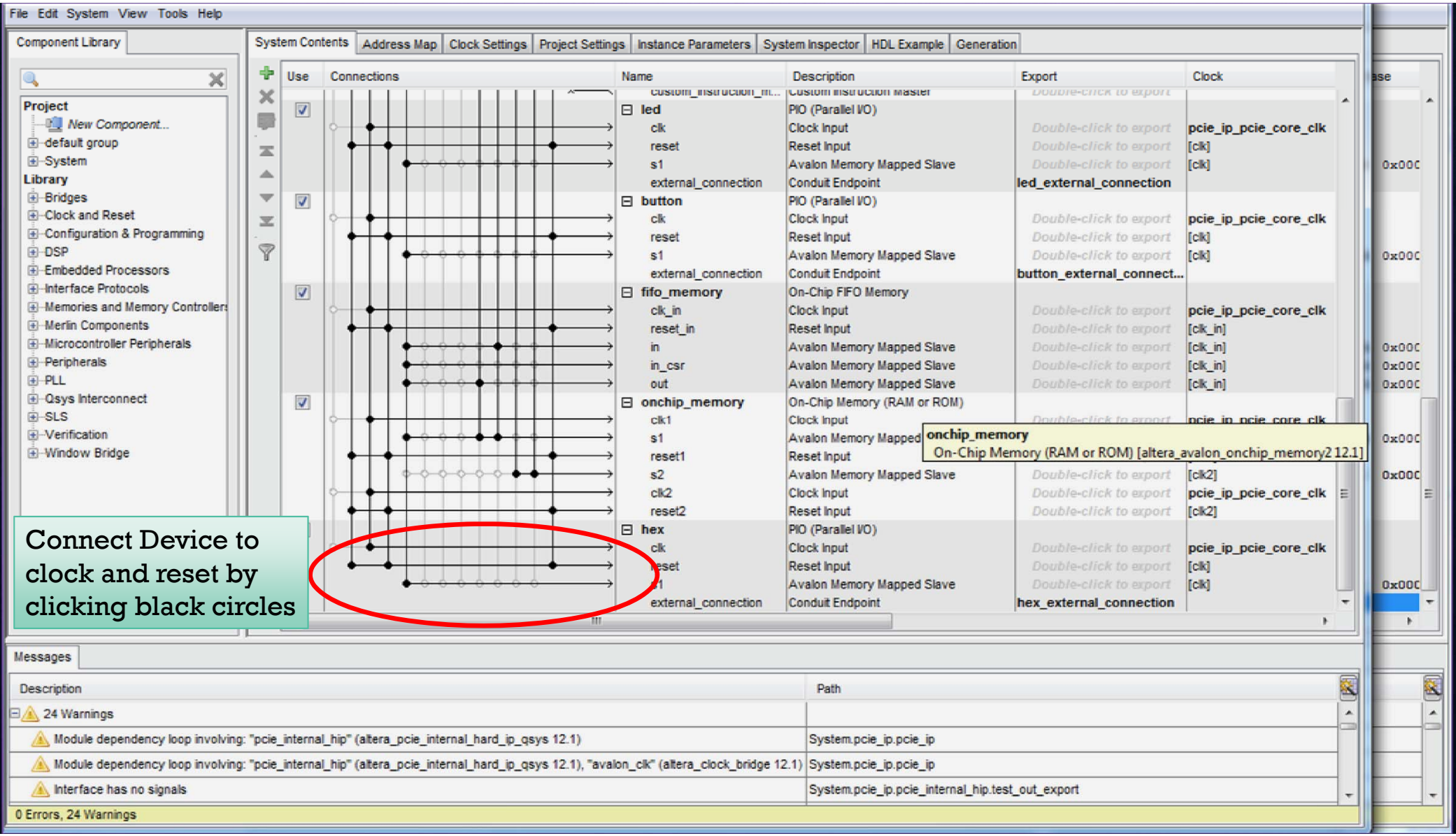
Window Bridge
New...
Edit...
Add...
led
clk
reset
s1
external_connection
button
fifo_memory
clk_in
reset_in
in
in_csr
out
onchip_memory
clk1
s1
reset1
s2
clk2
pio_0
Rename device
Create external connections
Messages
Description
Path
Interface has no signals
System.pcie_ip.pcie_internal_hip.test_out_export
pcie_internal_hip.pcie_core_clk cannot be both connected and exported
System.pcie_ip.pcie_internal_hip
pcie_internal_hip.rc_rx_analogreset must be exported, or connected to a matching conduit.
pcie_internal_hip.rc_rx_digitalreset must be exported, or connected to a matching conduit.
2 Errors, 26 Warnings


File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
led
button
fifo_memory
onchip_memory
hex
clk
reset
s1
external_connection
in
in_csr
out
clk1
reset1
s2
clk2
reset2
clk_in
reset_in
PIO (Parallel I/O)
Clock Input
Reset Input
Avalon Memory Mapped Slave
Conduit Endpoint
On-Chip FIFO Memory
On-Chip Memory (RAM or ROM)
Double-click to export
pcie_ip_pcie_core_clk
[clk]
[clk_in]
[clk2]
led_external_connection
button_external_connect...
hex_external_connection
onchip_memory
On-Chip Memory (RAM or ROM) [altera_avalon_onchip_memory2 12.1]
Project
New Component...
default group
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Library
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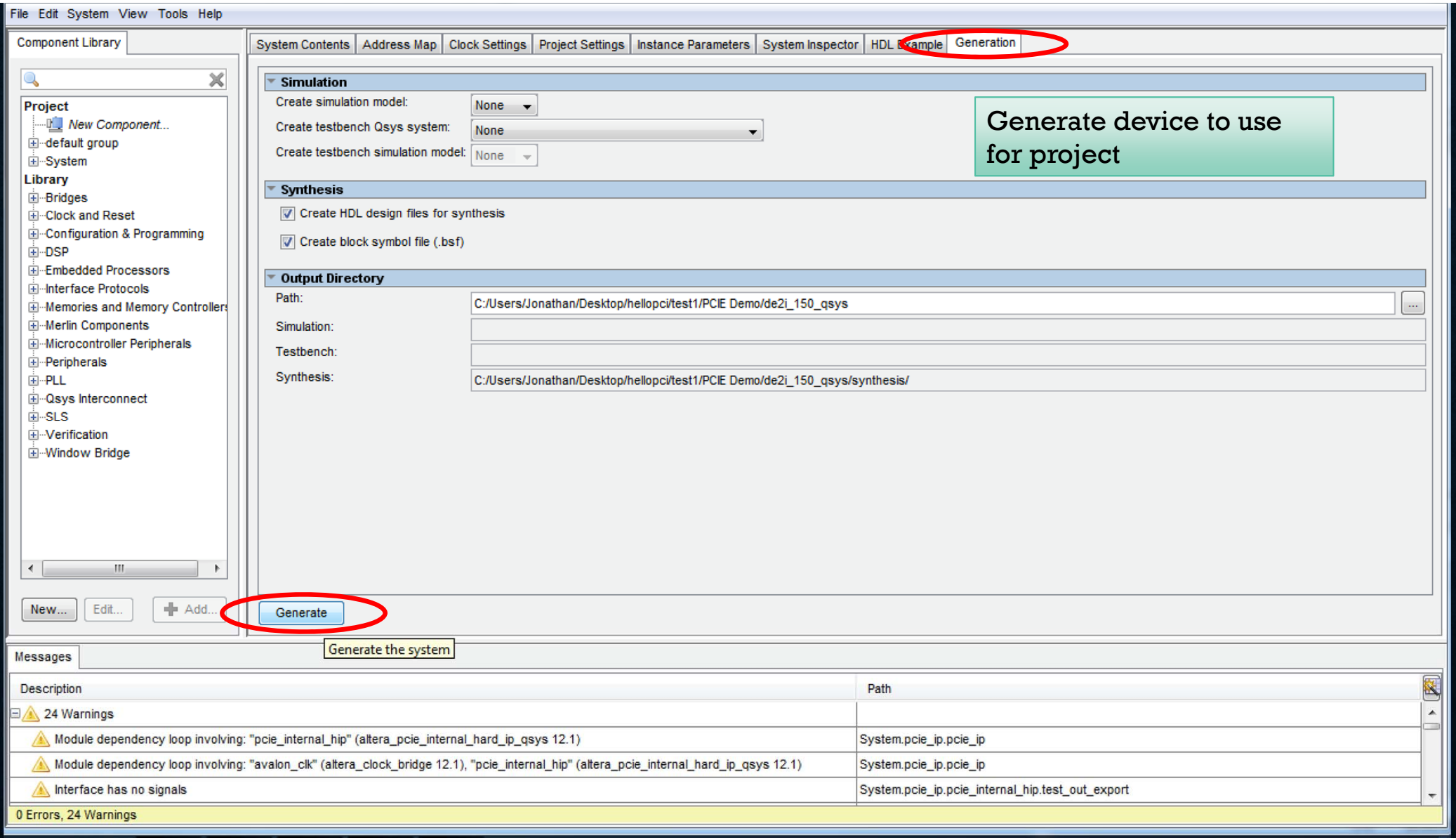
Peripherals
PLL
Qsys Interconnect
SLS
Verification
Window Bridge
Connect Device to clock and reset by clicking black circles
Messages
Description
Path
24 Warnings
Module dependency loop involving: "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1)
System.pcie_ip.pcie_ip
Module dependency loop involving: "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1), "avalon_clk" (altera_clock_bridge 12.1)
System.pcie_ip.pcie_ip
Interface has no signals
System.pcie_ip.pcie_internal_hip.test_out_export
0 Errors, 24 Warnings


File Edit System View Tools Help
Component Library
System Contents
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New Component...
default group
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Qsys Interconnect
SLS
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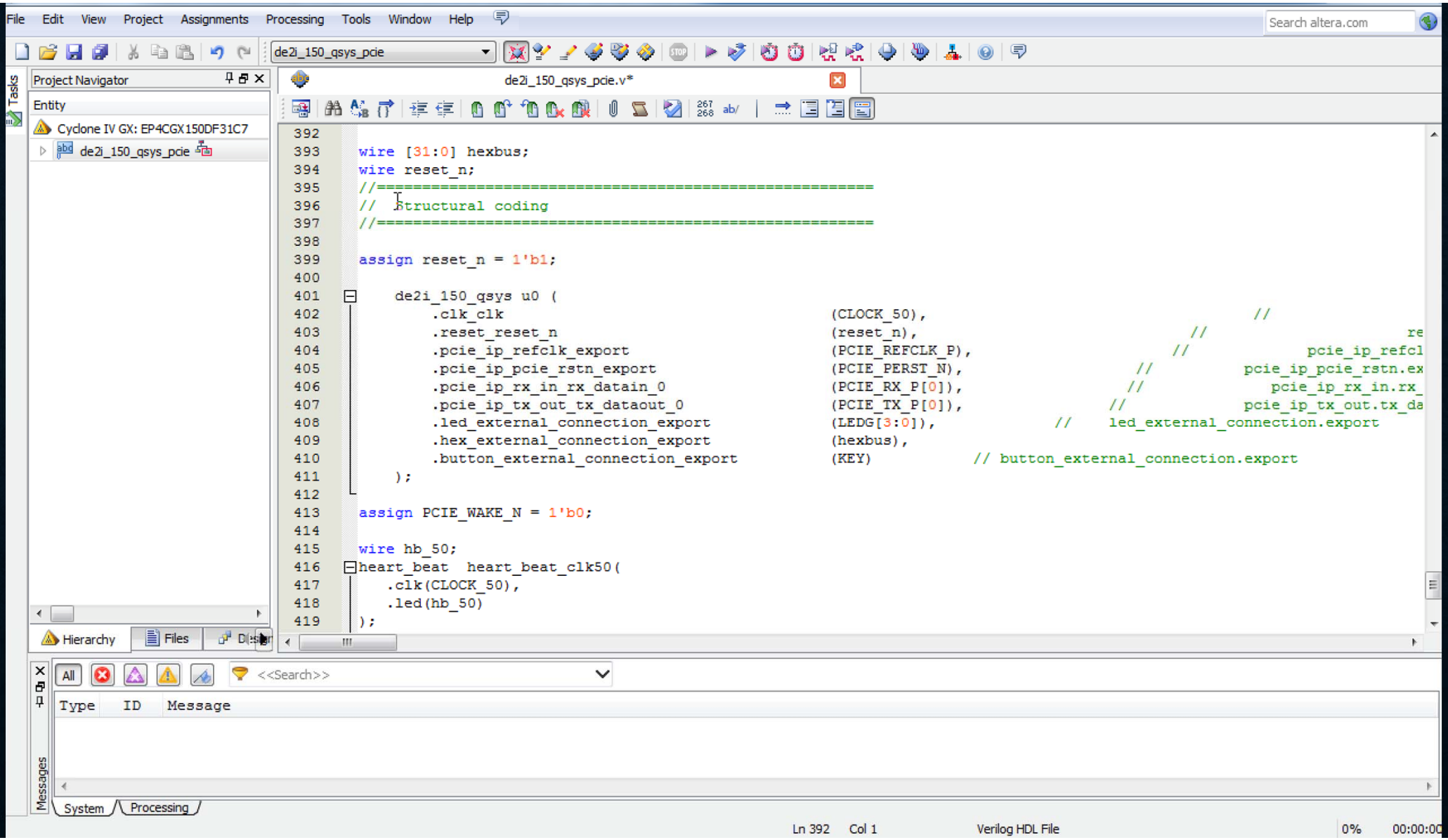
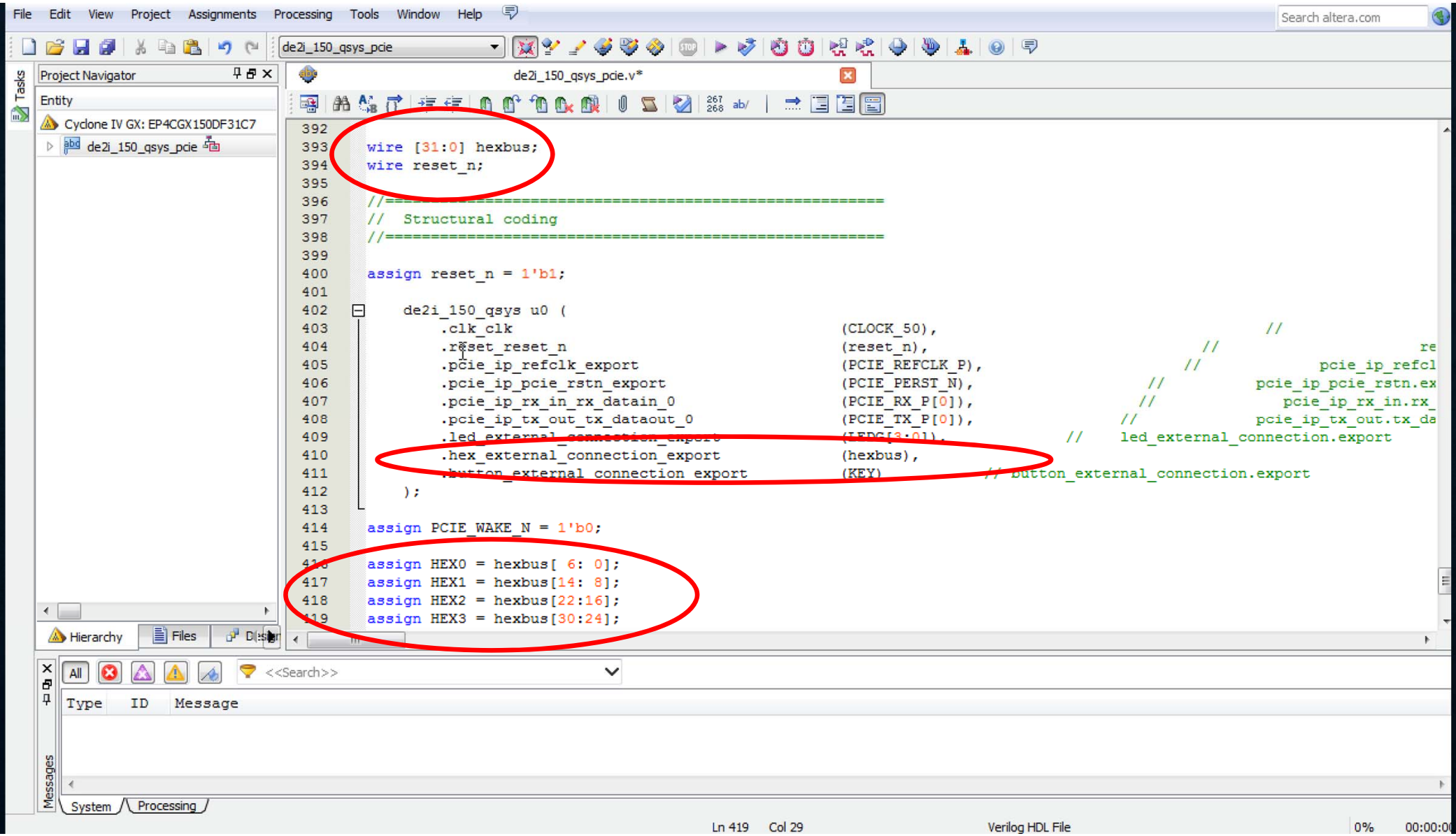
Window Bridge
New...
Edit...
Add...
Simulation
Create simulation model:
None
Create testbench Qsys system:
None
Create testbench simulation model:
None
Generate device to use for project
Synthesis
Create HDL design files for synthesis
Create block symbol file (.bsf)
Output Directory
Path:
C:/Users/Jonathan/Desktop/hellopci/test1/PCIE Demo/de2i_150_qsys
Simulation:
Testbench:
Synthesis:
C:/Users/Jonathan/Desktop/hellopci/test1/PCIE Demo/de2i_150_qsys/synthesis/
Generate
Generate the system
Messages
Description
Path
24 Warnings
Module dependency loop involving: "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1)
System.pcie_ip.pcie_ip
Module dependency loop involving: "avalon_clk" (altera_clock_bridge 12.1), "pcie_internal_hip" (altera_pcie_internal_hard_ip_qsys 12.1)
System.pcie_ip.pcie_ip
Interface has no signals
System.pcie_ip.pcie_internal_hip.test_out_export
0 Errors, 24 Warnings


File Edit View Project Assignments Processing Tools Window Help
Search altera.com
de2i_150_qsys_pcie
Project Navigator
Entity
Cyclone IV GX: EP4CGX150DF31C7
de2i_150_qsys_pcie
de2i_150_qsys_pcie.v*
wire [31:0] hexbus;
wire reset_n;
//===
// Structural coding
//===
assign reset_n = 1'b1;
de2i_150_qsys u0 (
.clk_clk (CLOCK_50),
.reset_reset_n (reset_n),
.pcie_ip_refclk_export (PCIE_REFCLK_P),
.pcie_ip_pcie_rstn_export (PCIE_PERST_N),
.pcie_ip_rx_in_rx_datain_0 (PCIE_RX_P[0]),
.pcie_ip_tx_out_tx_dataout_0 (PCIE_TX_P[0]),
.led_external_connection_export (LEDG[3:0]),
.hex_external_connection_export (hexbus),
.button_external_connection_export (KEY)
);
assign PCIE_WAKE_N = 1'b0;
wire hb_50;
heart_beat heart_beat_clk50(
.clk(CLOCK_50),
.led(hb_50)
);
// led_external_connection.export
// button_external_connection.export
Hierarchy
Files
All
<<Search>>
Type ID Message
Messages
System
Processing
Ln 392 Col 1
Verilog HDL File
0%


File Edit View Project Assignments Processing Tools Window Help
Search altera.com
de2i_150_qsys_pcie
Project Navigator
Entity
Cyclone IV GX: EP4CGX150DF31C7
de2i_150_qsys_pcie
de2i_150_qsys_pcie.v*
wire [31:0] hexbus;
wire reset_n;
//===
// Structural coding
//===
assign reset_n = 1'b1;
de2i_150_qsys u0 (
.clk_clk (CLOCK_50),
.reset_reset_n (reset_n),
.pcie_ip_refclk_export (PCIE_REFCLK_P),
.pcie_ip_pcie_rstn_export (PCIE_PERST_N),
.pcie_ip_rx_in_rx_datain_0 (PCIE_RX_P[0]),
.pcie_ip_tx_out_tx_dataout_0 (PCIE_TX_P[0]),
.led_external_connection_export (LEDG[3:0]),
.hex_external_connection_export (hexbus),
.button_external_connection_export (KEY)
);
assign PCIE_WAKE_N = 1'b0;
assign HEX0 = hexbus[6: 0];
assign HEX1 = hexbus[14: 8];
assign HEX2 = hexbus[22:16];
assign HEX3 = hexbus[30:24];
led_external_connection.export
button_external_connection.export
Hierarchy
Files
Type ID Message
System Processing
Ln 419 Col 29
Verilog HDL File
0%

PROGRAM BOARD

- After changes are made to the Quartus II files, compile all files
- After compiling files, program the board with the newly generated .sof file
- Once the board is program perform soft reset to board

MODIFYING APPLICATION

- Add addition code to include changes to the seven segment display
- Copy code files to the Yocto OS
- Load PCIe Drivers on Yocto
- Navigate to code files
  - Make sure all code files are together, ie: PCIE.h, PCIE.c, TERASIC_PCIE.h, teraisc_pcie_qsys.so,
  - Tip: Making the PCIe drivers close by to your program makes loading them quicker
- Compile program
  - root#: ***gcc –g –Wall –c app.c –o app.o***
  - root#: ***gcc –g –Wall –c PCIE.C –o PCIE.o***
  - root#: ***gcc –g –Wall app.o PCIE.o app ldl***

APPENDIX

- References to helloPCIex:

  http://rijndael.ece.vt.edu/de2i150/designs/hellopcislides.pdf

- References to Module document files:

  http://humanslab.ece.gatech.edu/IntelCurriculum

- References System CD files documents from Terasic DE2i-150

  http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=163&No=529&PartNo=5

QUESTIONS