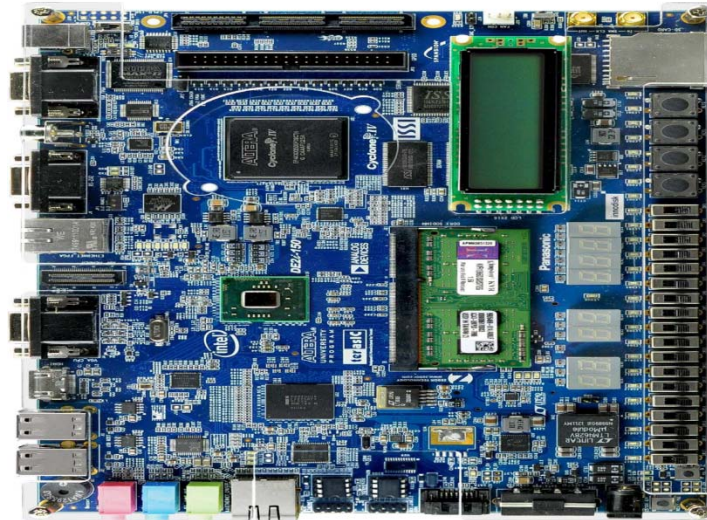


# EECE494: Computer Bus and SOC Interfacing

## DE2i-150 Development Kit



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# DE2i-150

- Charles Kim's Personal Etymology on the name DE2i-150
  - DE2: Altera's Development and Education Board - Kit made by Terasic
  - DE2i: DE2 + Intel Atom Processor - Kit made by Terasic
  - 150: 150k logic elements (149,760 LEs in the FPGA)



# DE2i-150 Kit



- Development Board
- System CD
- Quartus II CD
- Quick Start Guide
- USB Cable
- Power Cable
- IR Remote
- Loopback Board

- ⌘ Quartus: FPGA Software from Altera
- ⌘ Loopback: Feeding the output back to its inputs for testing and debugging

# DE2i-150 Kit Accesories



64GB mSATA  
SSD



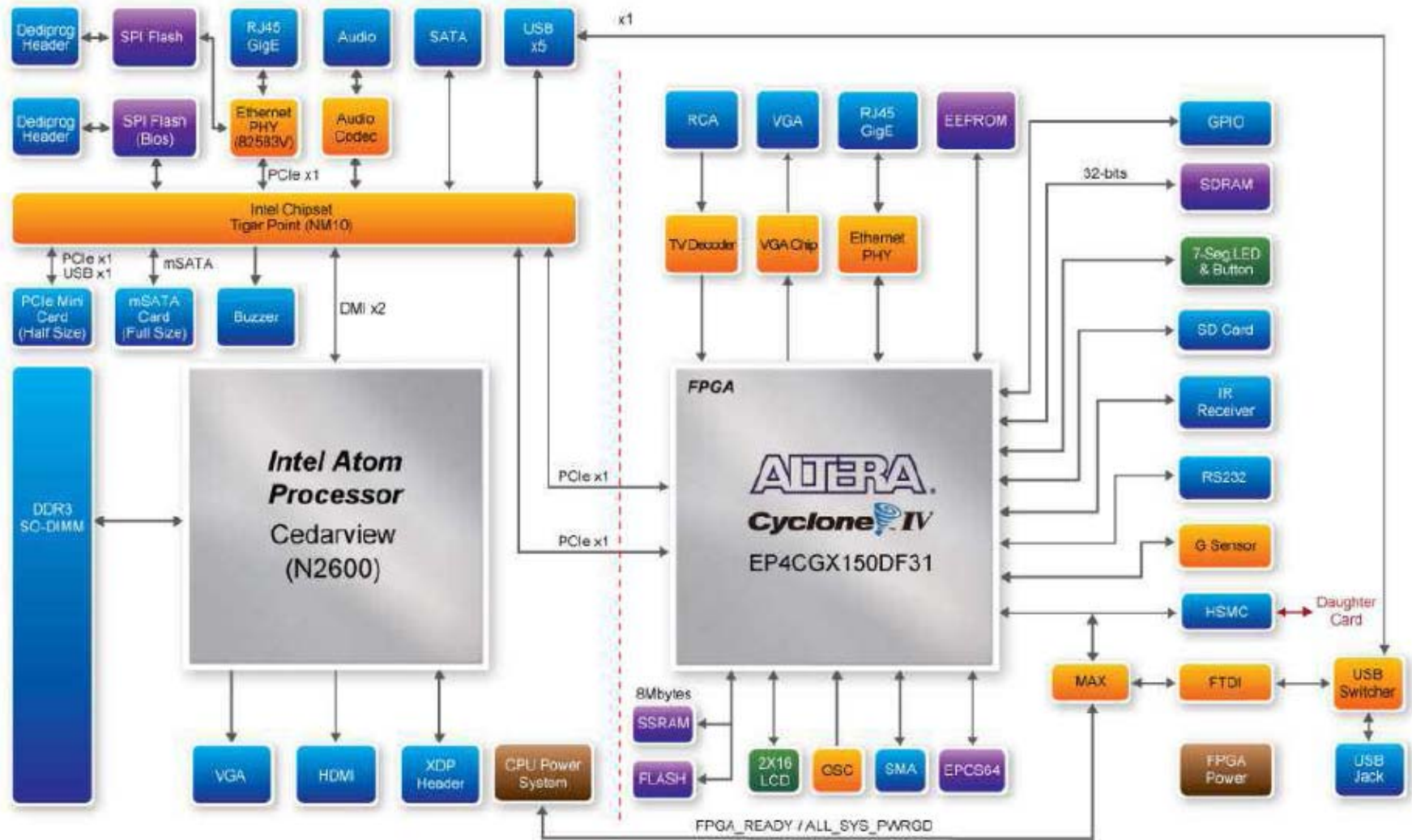
802.11a/g/n  
Wi-Fi Module



DDR3 Memory

- ⌘ ATA: Advanced Technology Attachment (Host  $\leftrightarrow$  Mass Storage Device)
- ⌘ SATA: Serial ATA
- ⌘ mSATA: Mini-SATA (for netbooks and laptops)
- ⌘ Wi-Fi: Wireless Fidelity “Wireless LAN products that are based on IEEE 802.11 standards”
- ⌘ DDR: Double Data Rate Synchronous Dynamic Random Access Memory
- ⌘ DDR2: Double Data Rate
- ⌘ DDR3: Double Data Rate Type-3

# DE2i-150 Kit Block Diagram



## Peripheral Interface --- Atom Processor N2600 and Express Chipset NM10

<i>Feature</i>	<i>Usage</i>
<i>DDR3 SO-DIMM/N2600</i>	Equipped with a 2Gbyte memory module
<i>HDMI 1.3a/N2600</i>	To attach a monitor
<i>VGA/N2600</i>	To attach a monitor
<i>XDP/N2600 – software debug port</i>	To use as software debug port
<i>SPI Flash/NM10</i>	Contains system BIOS, programming header available
<i>Buzzer/NM10</i>	Note: used during BIOS boot to indicate successful initial load
<i>Ethernet PHY/NM10</i>	Equipped with an Intel® 82583 Gigabit Ethernet Controller – (10/100/1000 M) Ethernet connection
<i>Audio Codec/NM10</i>	For audio input and output
<i>Mic In port</i>	
<i>SATA Gen2/NM10</i>	To connect external devices
<i>mSATA/NM10</i>	Equipped with a 60Gbyte SSD
<i>USB Port 1/ NM10</i>	To connect external USB 2.0 devices
<i>USB Port 2/NM10</i>	To connect external USB 2.0 devices
<i>USB Port 3/NM10</i>	To connect external USB 2.0 devices
<i>USB Port 4/NM10</i>	To connect external USB 2.0 devices
<i>PCIe Mini Card (Half size)/NM10</i>	Equipped with Intel® WiFi Link 6205 62205AN.HMWWG Half Height MiniCard and a WLAN Dual Band Antenna Assembly
<i>PCIe/NM10</i>	1x connection to FPGA hard PCIe IP block
<i>PCIe/NM10</i>	1x connection to FPGA soft PCIe IP block
<i>Reset Button</i>	
<i>Battery Holder</i>	

# Intel Chipset Interface

- ⌘ HDMI: High-Definition Multimedia Interface – A/V Interface for transferring video data and digital audio data
- ⌘ VGA: Video Graphics Array – 3 row 15 pin connector display hardware introduced with IBM PS/2 line of computers
- ⌘ XDP: Intel eXtended Debug Port
- ⌘ SPI: Serial Peripheral Interface Bus --- Synchronous Serial data link in full duplex mode
- ⌘ USB: Universal Serial Bus --- data and power
- ⌘ PCI: Peripheral Component Interconnect – an Intel local bus standard for network cards, sound cards, modem, etc
- ⌘ PCIe: PCI express – high speed serial expansion bus
- ⌘ PCI-X: PCI eXtended for higher bandwidth

# Peripheral Interface --- Altera FPGA Cyclone IV

- VGA Display, TV Decoder (Composite Input)
- Gigabit Ethernet
- SD Card Socket
- IR Receiver, RS232
- Accelerometer
- HSMC & GPIO Expansion Connector
- EEPROM, Flash, SSRAM, SDRAM, and EPCS64(for FPGA Configure)
- Two PCIe x1 (Connected to Intel Atom)
- On board Oscillator and SMAx2 for External Clock Input & Output
- LED, 2x16 LCD, Button, Switch & 7-Segment
- On-board USB Blaster





## FPGA Interface

- ⌘ SD: Secure Digital (card) – non-volatile memory card format for use in portable device
- ⌘ HSMC: High Speed Mezzanine Card – Altera’s high speed interface
- ⌘ GPIO: General Purpose Input/Output
- ⌘ RS232: EIA( Electronic Industry Association) standard for serial binary single-ended data and control signals for computer serial ports. RS comes from the “Radio Sector” of the EIA.
- ⌘ G Sensor (Accelerometer)
- ⌘ OSC: Oscillator
- ⌘ SMA: Series Master Clock
- ⌘ USB Blaster: USB download cable for Altera USB-Blaster Programming cable (with Quartus II software)
- ⌘ JTAG: Joint Test Action Group – IEEE1149.1 standard test access port and boundary scan architecture --- “FPGA programming cable”
- ⌘ EPCS64: Altera’s (In-System Programmable) Serial Configuration Chip
- ⌘ RCA: electrical connector for audio video signal “Radio Corporation of America”. A/V Jack.
- ⌘ RJ45: Register Jack 45 for a physical network interface /Ethernet Connector
- ⌘ VGA

# Mezzanine?

## ⌘ Mezzanine

- ☒ Entresol
- ☒ Intermediate floor between main floors
- ☒ Low-ceilinged and projects in the form of balcony
- ☒ Lowest balcony in a theater
- ☒ “mezzano” ---”middle”

## ⌘ Mezzanine Card

- ☒ Smaller form of the usual peripheral interface cards
- ☒ “daughter board”
- ☒ For rugged industry use
- ☒ FMC (FPGA Mezzanine Card)
- ☒ PMC (PCI Mezzanine Card)

# Daughter Cards



Capacitive Touch  
Screen



CameraLink Adapter



5 Megapixel Camera



HDMI Input



DVI Input/Output



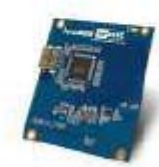
Ethernet



Serial Digital  
Interface



Altera Industrial  
Communications



HDMI Output



Aptina Adapter



AD/DA



Mass Storage and  
Video



High Speed AD/DA



Communication



SATA/SAS

# EECE 494 Computer Bus and SoC Interfacing

## Spring 2014

- ⌘ Team-based labs
- ⌘ Major Platform: DE2i-150 Kit
- ⌘ Other platforms:
  - ☒ Intel Galileo
  - ☒ Arduino
  - ☒ Raspberry Pi
- ⌘ Computer Bus
- ⌘ Interfacing with external devices and daughter boards