

		<b>3rd Version: 11/19/2007</b>
Marlon Winder Hassan Ayinde Tolu Onibiyo Laurence Wilson Idris Ozoya	<b>REQUIREMENT LIST</b> FOR THE NETWORK PACKET INSPECTOR & INTRUSION DETECTOR	
<b>DATE UPDATE</b>	<b>REQUIREMENTS</b>	<b>SOURCES</b>
	<b>Overall Function:</b> <i>A microprocessor that is capable of deep packet inspection at wire speed.</i>	
10/01/2007	<b>SIZE</b> <ul style="list-style-type: none"> <li>Processor would be implemented on a single Virtex4 XC4VLX25 FPGA board.</li> </ul>	The Team
10/17/2007	<b>PERFORMANCE</b> <u>Hardware:</u> <ul style="list-style-type: none"> <li>Processor must be dynamically configurable.</li> </ul>	Marlon
10/17/2007	<ul style="list-style-type: none"> <li>Ability of the processor to search for patterns contained in the payload portion of IEEE 802.3 Ethernet frames.</li> </ul>	Marlon, IEEE Standard
10/17/2007	<ul style="list-style-type: none"> <li>Support of relational operations and expressions in accordance with the Portable Operating System Interface (POSIX) expression lexicon.</li> </ul>	Marlon
10/17/2007	<ul style="list-style-type: none"> <li>Ability to search for “don’t care” bytes within frames.</li> </ul>	
10/20/2007	<ul style="list-style-type: none"> <li>Provides signals at the top/UI level to indicate expression match, prescribed action to be taken, and frame location where match was found.</li> </ul>	Laurence Tolu
10/23/2007	<ul style="list-style-type: none"> <li>Processor must have the ability to search for matches given data input at a rate in excess of 100 Mbps.</li> </ul>	Hassan
10/17/2007	<ul style="list-style-type: none"> <li>Ability to provide audible notification when match found.</li> </ul>	
10/20/2007	<u>Software:</u> <ul style="list-style-type: none"> <li>The UI must allow configuration and manipulation of search patterns.</li> </ul>	Tolu
10/20/2007	<ul style="list-style-type: none"> <li>Ability to receive signals from the hardware device indicating an expression match, prescribed action to be taken, and frame location where match was found.</li> </ul>	Hassan
		Laurence, Tolu & Marlon I

10/20/2007	<ul style="list-style-type: none"> <li>• Provide statistics regarding match count.</li> </ul>	dris
10/19/2007	<p><b>SAFETY</b></p> <ul style="list-style-type: none"> <li>• Device must not generate heat in the excess of 40°C from 6 inches away</li> </ul>	The Team
10/20/2007 10/23/2007	<p><b>COST AND SCHEDULE</b></p> <ul style="list-style-type: none"> <li>• FPGA board must cost less than \$1000</li> <li>• Content Process design must be completed and ready for testing by 3/1/2008</li> </ul>	Team
10/23/2007 10/01/2007	<p><b>INTERFACES</b></p> <ul style="list-style-type: none"> <li>• FPGA board must interface with user via EIA232 RS232 serial communication port.</li> <li>• FPGA board must interface with internet via standard Ethernet Port.</li> </ul>	Marlon Hassan Tolu IEEE Standard
11/09/2007 11/09/2007	<p><b>COMPLIANT STANDARDS</b></p> <ul style="list-style-type: none"> <li>• IEEE 802.3 Ethernet</li> <li>• EIA232 RS232 Serial Port</li> <li>• IEEE 1003 POSIX expression lexicon.</li> </ul>	IEEE Standard