Development of an Economical Bit Error Rate Tester

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Outline

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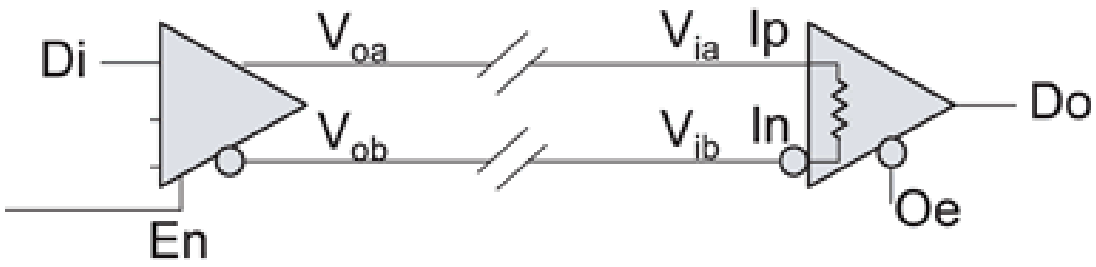
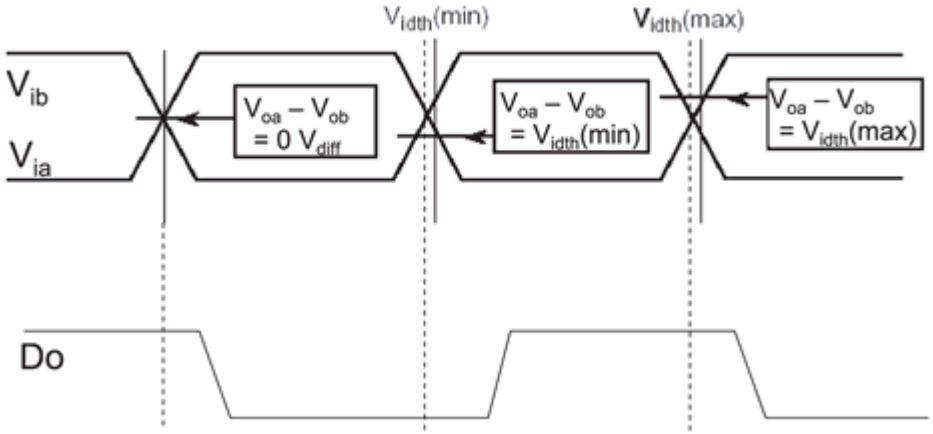
Introduction

- Our objective is the development of an economical Bit Error Rate Tester (BERT) that has the ability to determine if the receiver component of the Device Under Test (DUT) is working satisfactorily.
- The signal must be transmitted through the LVDS Signal Specifications.

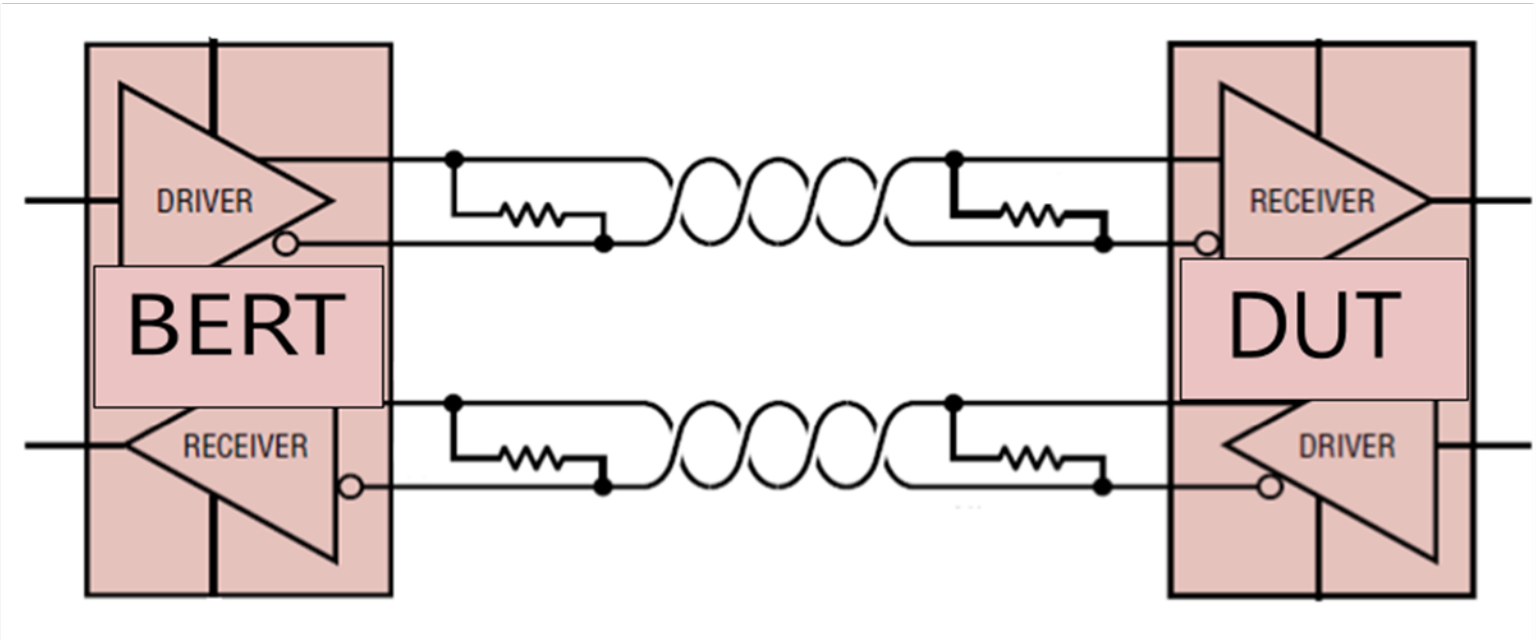
Introduction

driver interconnect receiver





Introduction



Picture From LVDS Transceiver device specification sheet by Linear Technologies

Introduction

- BER is a ratio between the number of bit errors transmitted and the number of bits received.

$$BER = \frac{N_{Err}}{N_{bits}}$$

- You must determine a confidence level (CL) at which you would like to operate at. you must find out the number of bits you need to transmit based on your CL.

$$N_{bits} = \frac{-\ln(1-CL)}{BER}$$

Introduction

- We then need to determine how much time we the device will needed to run in order to meet our BER and confidence level.

$$Time(seconds) = \frac{-\ln(1-CL)}{\text{bps} * BER}$$

Introduction

- DUT (Device Under Test)
  - DUT is used to reference any Device currently tested by our BERT system.
- DUT Types in order of preference
  - Built DUT
    - Designed From Analog Components
  - FPGA
    - An FPGA capable of being an LVDS receiver
    - Not ideal because the device normally has to undergo a certain number of tests

Problem Definition

- J-Bert cost about (350K) and there are times when analysis can be done before requiring such an expensive system.
- Cause: Extremely High Levels of Accuracy and, exotic jitter injection methods drive of the cost of the device.

Current State of the Art

- The closest devices on the market two ours are the AGILENT BERT N4903A/B and the Tektronix BertScope are on the market.
- These are the complete BERT systems that cost 350K + that we would like our systems to sit alongside with.

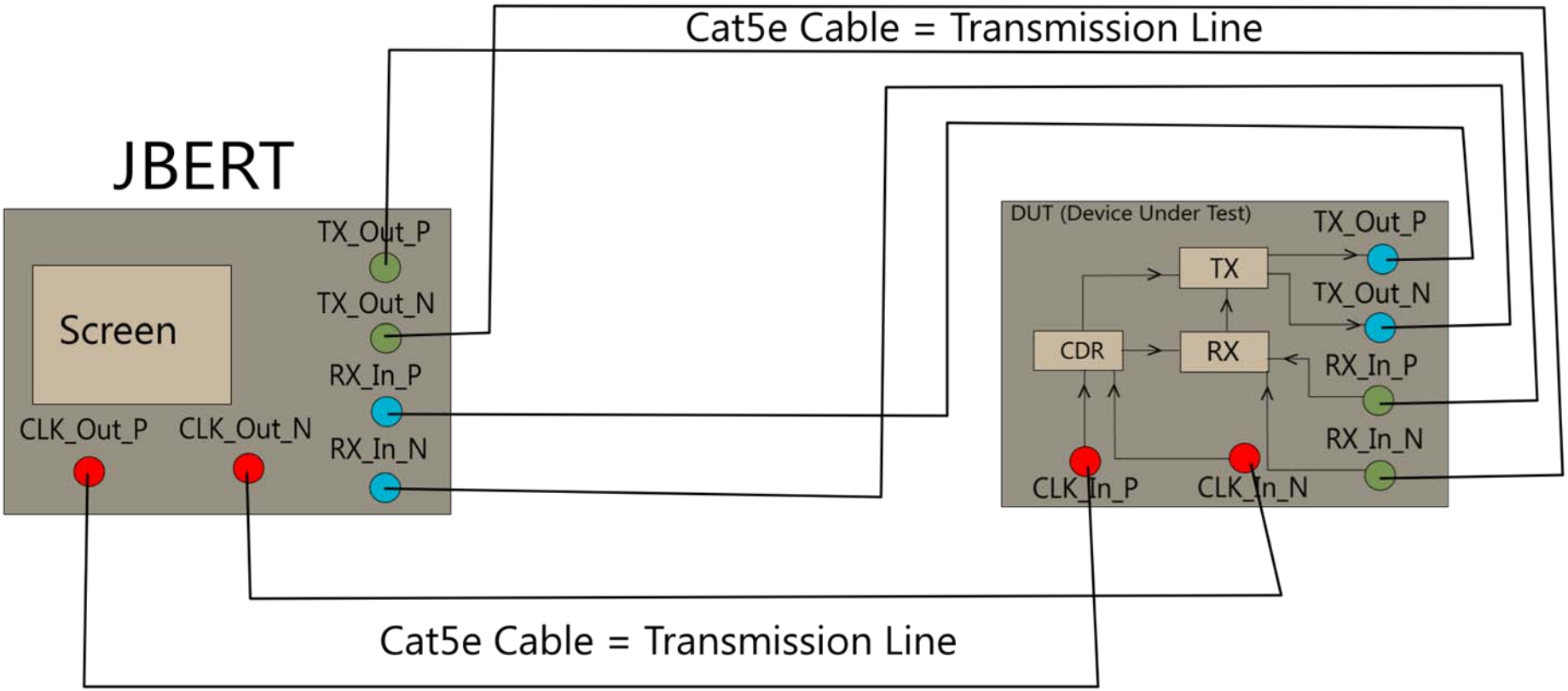
Current State of the Art

- There does not exist a smaller and cheaper device that could be used for quicker lab tests and for placement on a general lab debug station. There for the current market has a hole which we would like to cover.

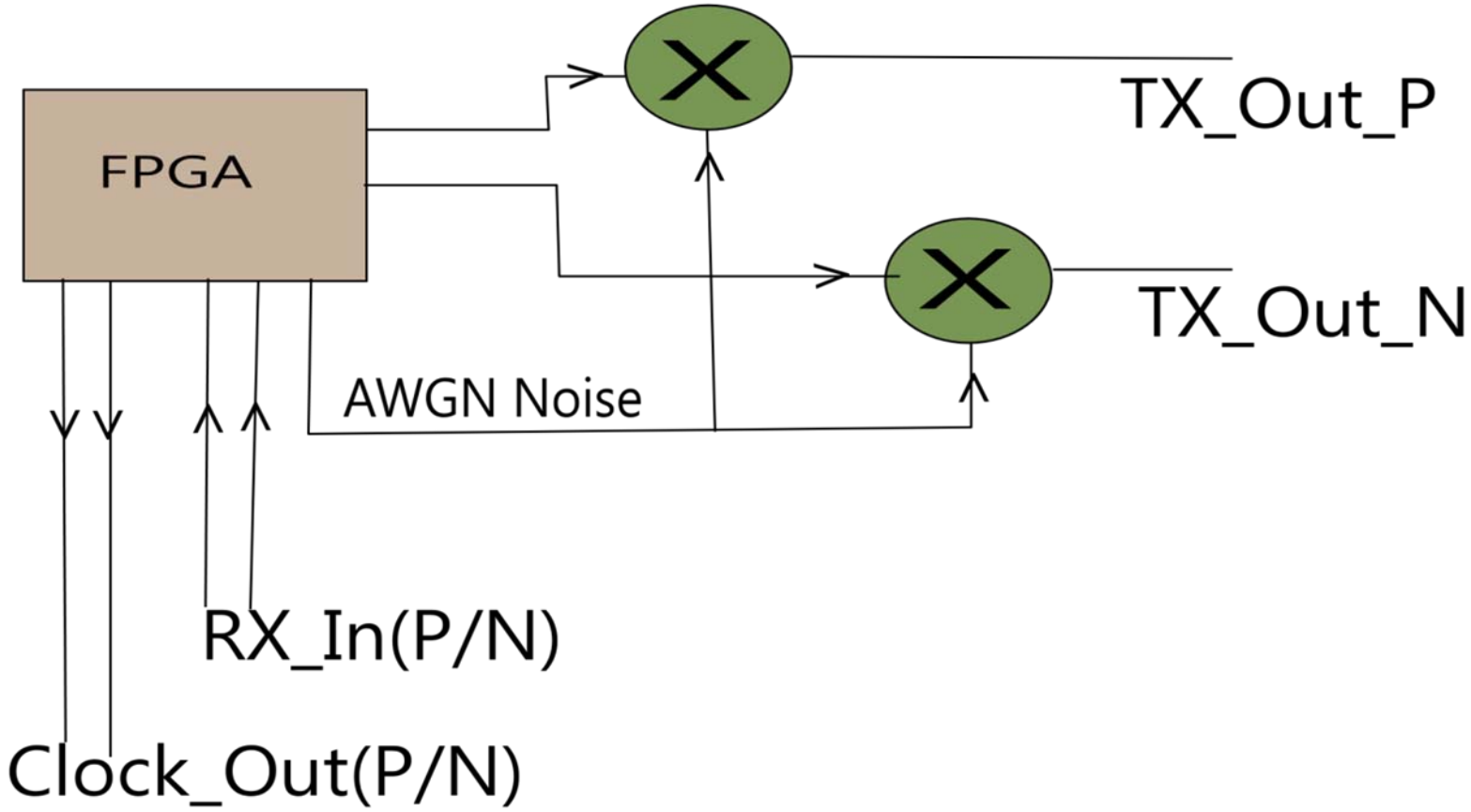
Engineering Approaches

- We propose an FPGA based Bit Error Rate tester which is composed of two main parts; the BERT; and the Additive White Gaussian Noise (AWGN) Generator.

Engineering Approaches



Engineering Approaches



Test Conditions

- The testing setup for our test environment has been heavily explored and some methods have been determined. The setup is as follows:
- Transmitter with 100 Ohm termination
- Transmission Line with 100 Ohm differential impedance (Cat3e/Cat5 cables)
- Receiver with 100 Ohm termination

Test Conditions

4.4 Common-mode noise rejection

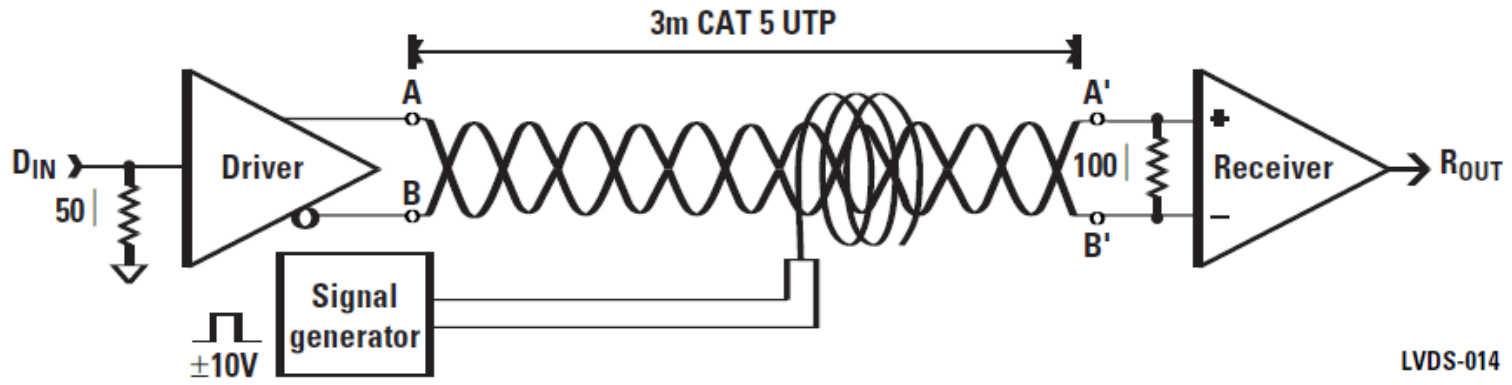


Figure 4.5. Common-mode noise rejection test setup

Picture From LVDS Owner's Manual Low-Voltage Differential Signaling by National Semiconductor

Tasks and Deliverables

No.	Task	Start Date
1	Look into current state of art	10/27/2010
2	Select most appropriate solution	11/03/2010
3	Consult with Faculty initial solution	11/03/2010
4	1st. Draft of Proposal Writing	11/10/2010
5	Submission of 1st Draft of Proposal	11/17/2010
6	Revision of Proposal	11/17/2010
7	2nd Electronic submission of Presentation	11/17/2010
8	Submission of Proposal (Hard Copy)	12/01/2010
9	Perform software simulations using Simulink	11/29/2010
10	Seek applicable hardware	12/05/2010
11	Purchase identified hardware	01/09/2010
12	Commence development of design	01/15/2010
13	Have a working prototype	03/01/2010
15	Product improvement/validation	03/08/2010
14	Presentation of final design	04/14/2011

Tasks and Deliverables

Gerard	Dotun
Research current BERT implementation methods	Research applicable hardware
Research IEEE LVDS specifications	Purchase identified hardware
IEEE grant proposal	Learn AWGN modeling and generation methods
VHDL programming of the FPGA	Build the physical circuit

Tasks and Deliverables

Deliverables:

A working prototype which:

- Outputs a Bit Error Rate
- Outputs a status (Pass/Fail/Intermediate)
- Refreshes the BER and status displayed on the user interface at least every 15 seconds.
- Allows the user to start, pause, and restart the BERT

Conclusion

- We have identified a hole within the current state of art and we intend to create a product that can fill this gap. From that point key concepts like Bit Error Rate and Additive White Gaussian Noise have been explored in order to understand the feasibility of our Idea.

Conclusion

- Based on the requirements and core concepts we believe our project is not only feasible but will become a new necessity in the market.

References

- [1] Agilent Technologies, *How do I measure Bit Error Rate (BER) to a given confidence level,* Palo Alto, California
- [2] IEEE, *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) IEEE Std 1596.3-1996*
- [3] Linear Technologies, *Differential Driver and Receiver Pair LTC491 Device Manual*
- [4] Yongquan Fan, Zeljko Zilic, and Man Wah Chiang, *A Versatile High Speed Bit Error Rate Testing Scheme*