Development of an Economical Bit Error Rate Tester

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Advisor's Signature _____ DATE_____

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Revision History

Version	Updates	Date
Design Requirements Submitted		10/26/10
Project Proposal Version 1	o First Full Proposal	10/26/10
Project Proposal Version 2	o Made a clear that receiver is being tested rather than transmission line o Defined what the DEVICE UNDER TEST is (DUT)	11/24/10
Project Proposal Version 3	o Changed Title o Use of Microsoft Generated Outline o Design Requirements Table added o Sections added: Goals o Added an alternative solution o Added dates to the deliverables	11/29/10
Project Proposal Version 4	o Check FCC regulation on AWGN EMI radiation o Understand if shielded cables are needed o If shielded cables are needed understand how to terminate them o Include Cost of the Design o Signature Page added	12/8/10

Introduction

Objective

Our objective is the development of an economical Bit Error Rate Tester (BERT) that has the ability to determine if the receiver component of the Device Under Test (DUT) id working satisfactorily. The signal must be transmitted through the LVDS Signal Specifications.

Goal

To develop a JBERT system that could enter the market a 6% of the cost of current systems, and become useful enough to be placed on any transceiver debug station.

Background

Transceiver testing encompasses three main tests: measuring rise time at the load, measuring jitter in an eye pattern, and bit error testing. Our device focuses only on the receiver and therefore only uses one of three test methodologies which is the bit error testing.[1] A key point in BERT technology is that they are built to test receivers of devices. Meaning when it comes to a BERT specifically we are not interested in particular transmission line effects or transmitter characteristics.

A Jitter Bit Error Rate (JBERT) is a machine that has the ability to test the receiver side of a communication interface by transmitting a pseudo-random bit sequence along with jitter along the line. After the device retimes and retransmits the data it will be analyzed to determine the Bit Error Rate (BER). First you must know that the BER is a ratio between the number of errors transmitted and the number of errors received.

$$BER = \frac{N_{Err}}{N_{bits}}$$

Next you must determine a confidence level at which you would like to operate at. This is determined by the following formula. Once you have determined your confidence level you must find out the number of bits you need to transmit but substituting your ideal confidence level into CL. (Ex: 98% percent confident level would be .98)

$$N_{bits} = \frac{-\ln(1-CL)}{BER}$$

[1] Clarified that the receiver of the DUT is what will be tested. 11/17/10

Lastly we need to determine how much time we the device will needed to run in order to meet our BER and confidence level.

$$Time(seconds) = \frac{-\ln(1-CL)}{f*BER}$$

In order for our system to be usable in the real world we need some form of jitter injection. We have determined that Additive White Gaussian Noise (AWGN) would be the best method for us since it is regularly used in communication interfaces as a jitter injection source.

Our transmission line will be transmitted under Low Voltage Differential Signal (LVDS) standard in order to fall under some well defined guidelines that have already been heavily tested for their accuracy and validity.

The testing setup for our test environment has been heavily explored and some methods have been determined. The setup is as follows:[2]

- Transmitter with 100 Ohm termination
- Transmission Line with 100 Ohm differential impedance (Cat3e/Cat5 cables)
- Receiver with 100 Ohm termination

A big problem has been identified with the setup, you must route your signals very close and short to the transmission medium else you can receive high levels of interference (this is true for any differential signal).

Customer Needs

Customer needs a system that can give some general information (Pass/Fail) about the interface for a significantly smaller price than the currently commercial BERT deceives. Currently if an engineer is experiencing problems with his device receiving or transmitting signals he must narrow down which part of the communication interface is having issues. Methods used for checking the transmitter are out of the scope of the proposal because the proposal does not propose any advantages to that side of the transceiver. We are proposing a device that can help with the debug side of the receiver. Currently if you are trying to identify if whether your receiver is working properly you or your company must buy a JBERT at 350K or rent one at 18K a month.

What the Proposal Intends to do

Create an economical JBERT system that can mirror the normal system on a smaller scale. Our JBERT must cost 20K or less for the total system, and be able to sit side by side with current BERT technology to help increase productivity, and add capabilities to companies.

[2] Identified industry standardized testing procedures 11/17/10

Problem Definition

Clear/Refined Problem Definition

The JBERT costs about (350K) and there are times when some analysis can be done before requiring such an expensive system. There exists no device on the market that is extremely cost effective that could be used to rule out receiver side errors in a communication line. A system like this could save money in the form of wasted idle man hours, project delays, and unnecessary rental cost of full JBERT system.

Cause of the Problem

Extremely High Levels of Accuracy and, exotic jitter injection methods drive of the cost of the device. We have seen that jitter can be injected via hardware and use only an Additive White Gaussian Noise (AWGN) generation, and the system can still follow a normal JBERT BER curve. We have identified that some of the features of mainstream JBERT's are "overkill" for a lot of general tests that are done. Although the major systems have created a need for smaller systems they are not meant to replace their larger cousins.

Design Requirements

There are a suite of design requirements that must be met in order for the system:

- Design a system that can generate and check an LVDS signal.
- Transmit a pseudo-random sequence through a transmission line loop.
- Add random noise to the transmission line. (Gaussian White Noise)
- Identify any mismatches in bits
- Use different transmission lines (This will hold the designed system constant)
- The entire system must run off the same clock and must be able to supply the clock to a device being tested
- Rate the receivers performance (develop a metric of success)
- Use IEEE LVDS Spec 1596.3

- A major assumption that we will use under our test environment is that there are no errors with our transmit line. Our goal is not to test the integrity of the transmitter or transmission line, because there are already methods for those, and we are not offering alternatives to them.

Design Requirement		
Design Project Title:	Development of an Economical Bit Error Rate Tester	
Team Name:	Summit	
Team Members:	Oludotun Ode, Gerard Spivey	
Date:	10/26/2010	
Requirements	**Descriptions**	**Source**
Background (NEED)	A very affordable JBERT system that can be used during the debug process of receivers	
Objective (Problem)	Build a JBERT system that can generate a high frequency signal (LVDS) and give some quantitative performance information about the system.	
Performance	The JBERT should: • Generate an LVDS signal (Between 250mv and 400mv voltage swing, differential signal, uniform ground, and self terminated). • Transmit a clock that the receiver device uses to retime the data (100 MHz). • Transmit data at 100Mbps • The system must detect a Bit Error Rate of 10^-8 or more	IEEE Std. 1596.3 From HP Bert HP E4829B
Cost	The JBERT design: • The device must cost less than $10000. • Comes with a lifetime firmware upgrade (HDL/Software).	
Safety	Not known to be a harmful device	
Compliance	The JBERT should meet electrical specifications for the IEEE standard 1596.3. Any relevant connector standard by EIC	

JBERT Interface:	The JBERT interface should: • Allow the user to start, pause, and reset the JBERT • Output a Bit Error Rate (BER) • Output a status (Pass/Fail/Intermediate) • Use a visual indicator to show the test is in progress. • Refresh the BER and status at least every 15 seconds	Team requirements
Power	110-120 V supply for 50W power	Team requirements
Size and Weight	The total system should amount to no more than 10 lbs	
Deliverables	A JBERT able to provide metrics identified within the performance section	

Performance Measures

The will be two major performance metric's, first we must be able to generate the AWGN via hardware, and we must be able to determine a BER of 10^-8 or greater.

Required Compliance

Since the signals we are transmitting are LVDS we must comply with the IEEE 1596.3 specification.

Current Status of the Art

What are similar products in the market?

The closest devices on the market to ours are the AGILENT BERT N4903A/B and the Tektronix BertScope. These are the complete BERT systems that cost 350K + that we would like our systems to sit alongside with. Our system should be much more readily available due to cost and usability.

Is the problem already solved?

No. We have not found a BERT system that is current marketed at less than 20K per unit that could give some general information on the integrity of the receiver within the transceiver channel.

Weakness of current status of Art

There does not exist a smaller and cheaper device that could be used for quicker lab tests and for placement on a general lab debug station. Therefore the current market has a hole which we would like to cover.

What is available technology?

We have been looking into different technology that could be used within our system. We have determined that the Cyclone 3 FPGA created by Altera would be the best device due to its low cost and built in LVDS capabilities. The FPGA would be used to generate the transmitted sequence and the AWGN that will be added to the signal. We have also determined various Linear Technology analog circuits that could be used to create the receiver device.

Engineering Approaches

Initial Solution

Many Bit Error Rate testers (BERTs) have been made using software simulations, but these testers have speed limitations. We propose an FPGA based Bit Error Rate tester which is composed of two main parts; the BERT; and the Additive White Gaussian Noise (AWGN) Generator.

AWGN:

Physical communications channels add noise to transmitted signals, and this noise can be modeled as AWGN. We intend to use the central limit theorem to generate AWGN. The following algorithm will be used to generate the Gaussian (we have verified the Normal distribution of the random variables by software implementation of this algorithm):

Do

a. Generate two UDRVs, U_1 and U_2, between [0, 1]
b. Set: $V_1 = (2 * U_1) - 1$ *and* $V_2 = (2 * U_2) - 1$
c. Set: $S = V_1^2 + V_2^2$
d. If $S \geq 1$, go back to line 2
e. Loop until $S < 1$
f. Set: $W = \sqrt{-\frac{2\ln(s)}{s}}$
g. Generate two Gaussian variable

h. $X_1 = V_1 * W \qquad X_2 = V_2 * W$

We generate the two uniformly distributed random variables by using normalized outputs of pseudo random bit sequence generators (PRBS). We also plan to adjust the variances of the AWGN (therefore the signal to noise ratio (SNR) of the transmitted signal), by using an operational amplifier of variable gain.

We chose our FPGA based solution using the following decision matrix to determine the most feasible implementation.

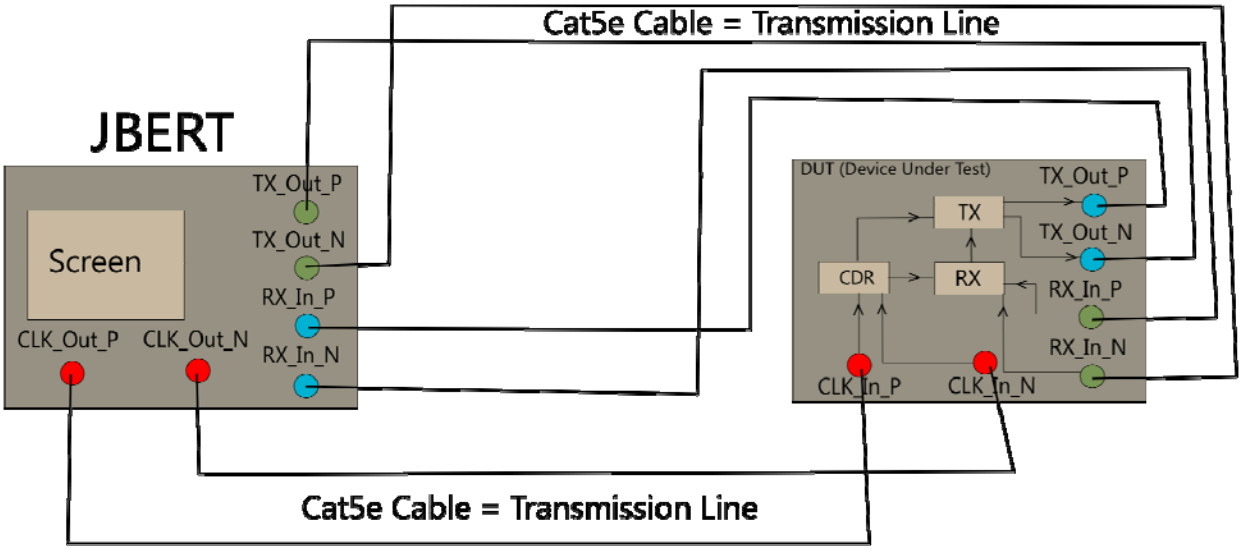
Decision		**FPGA**	**Microprocessor**
Usage	10	8	4
Ease of Generation	10	6	3
Speed	20	20	5
LVDS	25	19	3
Learning Curve	25	20	15
Cost	10	3	10
Total:		76	40

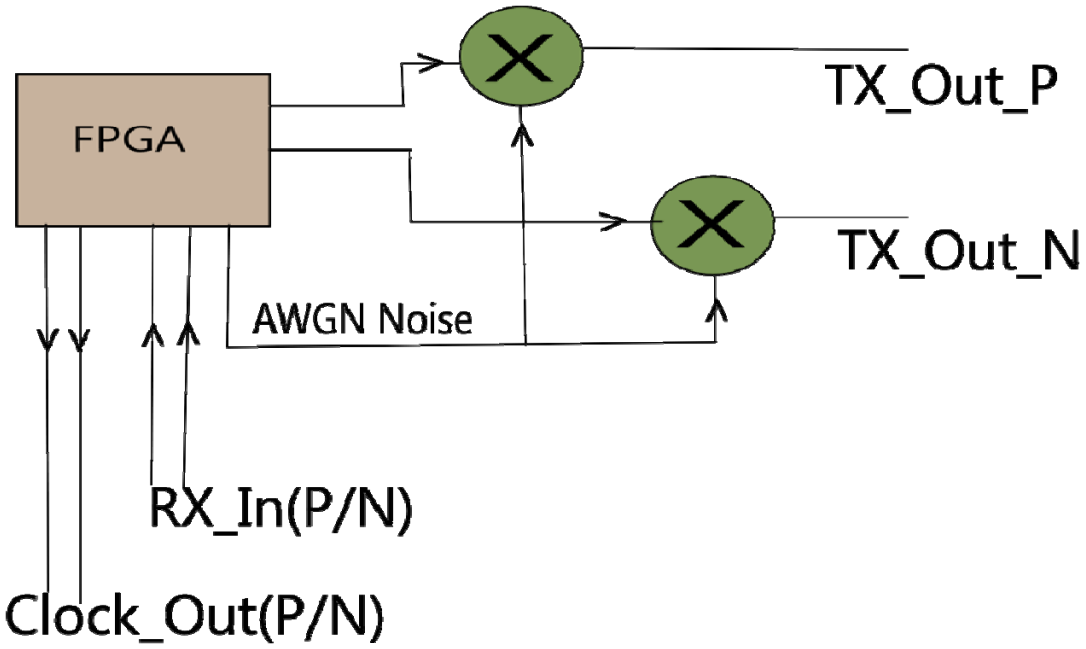
Nevertheless, although we prefer an FPGA based design, a software implementation of the BERT using microprocessors is in our estimation, a suitable alternative to our proposed initial solution.

NOTE: No FCC EMI violation due to the use of shielded twisted pair cables (Cat5e), whose shield line will be terminated by connecting its drain line directly to ground or using the RJ45 socket.[3]

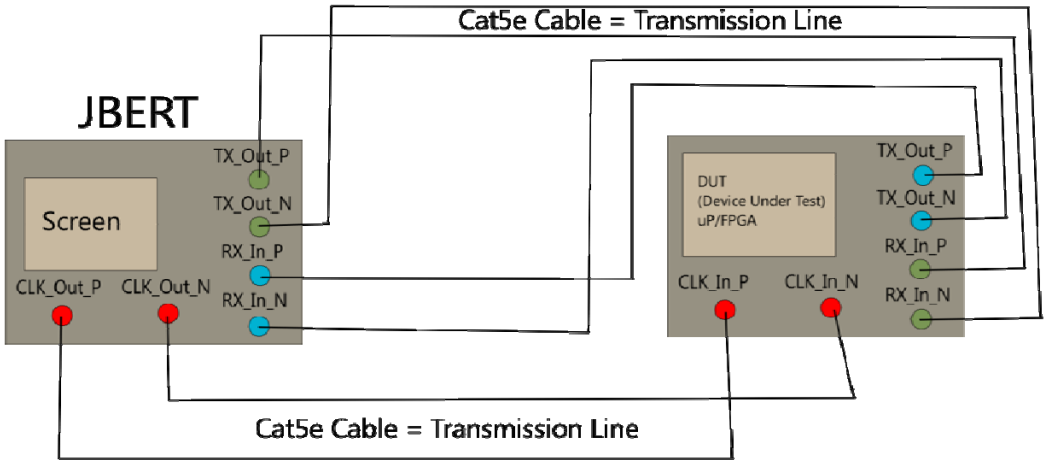
[3] Dr. Kim Comment Addressed. Comment given on 12/1/10

Provide schematics





Alternative Solution:



Systematic Process for solution:

Relevant knowledge and coursework

1) A technical competence in programming FPGAs, using hardware description language (HDL), is required (Digital systems and Advanced Digital systems).
2) A working knowledge of random variables and their probability density functions is also required (Probability and Random Variables).
3) A good understanding of LVDS specifications is also necessary for our design implementation (Electronics and circuit theory).
4) Proficiency in programming microprocessors may also be required, in the event that we decide to use our alternative solution (Microprocessors).
5) Current interfacing standards and technique will need to be understood
6) Noise addition methods will also be learned

Tasks and Deliverables

Tasks assigned to team members:

Gerard	Dotun
Research current BERT implementation methods	Research applicable hardware
Research IEEE LVDS specifications	Purchase identified hardware
IEEE grant proposal	Learn AWGN modeling and generation methods
VHDL programming of the FPGA	Build the physical circuit

Deliverables:

A working prototype which:

1) Outputs a Bit Error Rate
2) Outputs a status (Pass/Fail/Intermediate)
3) Refreshes the BER and status displayed on the user interface at least every 15 seconds.
4) Allows the user to start, pause, and restart the BERT

Project Management

Timelines and
milestones

No.	Task	Start Date
1	Look into current state of art	10/27/2010
2	Select most appropriate solution	11/03/2010
3	Consult with Faculty initial solution	11/03/2010
4	1st. Draft of Proposal Writing	11/10/2010
5	Submission of 1st Draft of Proposal	11/17/2010
6	Revision of Proposal	11/17/2010
7	2nd Electronic submission of Presentation	11/17/2010
8	Submission of Proposal (Hard Copy)	12/01/2010
9	Perform software simulations using Simulink	11/29/2010
10	Seek applicable hardware	12/05/2010
11	Purchase identified hardware	01/09/2010
12	Commence development of design	01/15/2010
13	Have a working prototype	03/01/2010
15	Product improvement/validation	03/08/2010
14	Presentation of final design	04/14/2011

Resources and Budget[4]

[4] Dr. Kim asked us to include Cost, date asked 12/1/10

- We are Applying for the IEEE Mini-grant worth $500
- Two Versions of Cyclone 3 Kit (We will Decide on kit used)
  - Version 1 $125
  - Version 2 $250
- Various analog components (less than $5 a component)
  - CDR (Clock Data Recovery Unit)
  - LVDS Transceiver
- Cat5e Cables
  - 10ft $11
  - 20ft $16

Conclusion

We have identified a hole within the current state of art and we intend to create a product that can fill this gap. From that point key concepts like Bit Error Rate and Additive White Gaussian Noise have been explored in order to understand the feasibility of our Idea. Based on the requirements and core concepts we believe our project is not only feasible but will become a new necessity in the market.

References

[1] Agilent Technologies, *How do I measure Bit Error Rate (BER) to a given confidence level*, Palo Alto, California

[2] IEEE, *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) IEEE Std 1596.3-1996*

[3] Linear Technologies, *Differential Driver and Receiver Pair LTC491 Device Manual*

[4] Yongquan Fan, Zeljko Zilic, and Man Wah Chiang, *A Versatile High Speed Bit Error Rate Testing Scheme*