Development of an economical Bit Error Rate Tester (BERT)

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Outline

- Introduction/background
- Problem Definition
- Design Requirements
- Solution Generation
- Top Design Selection
- Tasks and Deliverables
- Completed Tasks
- Tasks to be completed
- Timeline of Tasks

Introduction

- Jitter-Bit Error Rate Tester (J-Bert) is an expensive machine used to test the receiver component of a transceiver device

- We are designing an economical version of the bert that can identify a confidence level of the receiver component

- J-Berts cost about (350K) and there are times when analysis can be done before requiring such an expensive system.

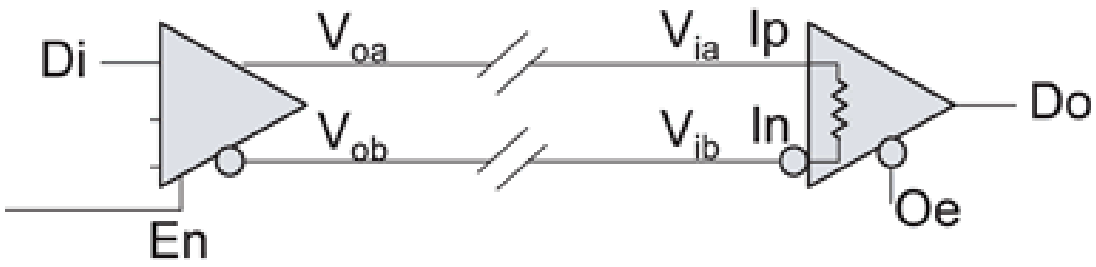
- Cause: Extremely High Levels of Accuracy and, exotic jitter injection methods drive of the cost of the device.

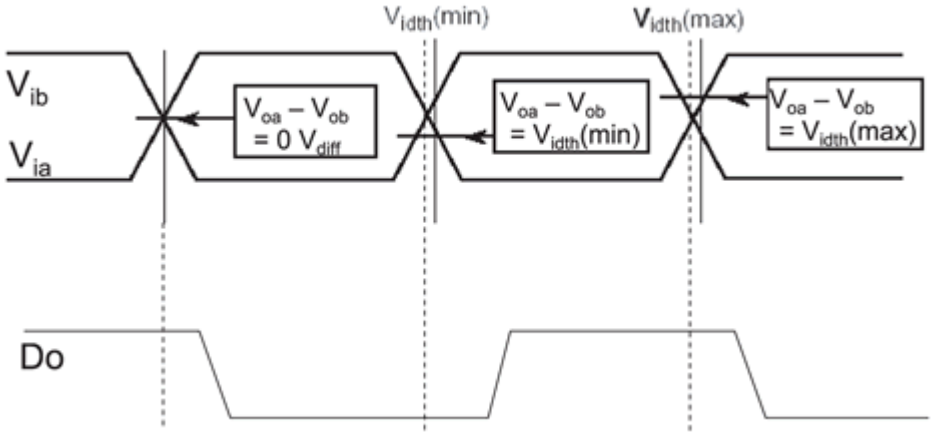
Introduction

- A typical environment for a J-Bert:
  - A driver
  - An interconnect (transmission line)
  - A receiver
- The J-Bert is used to test the receiver

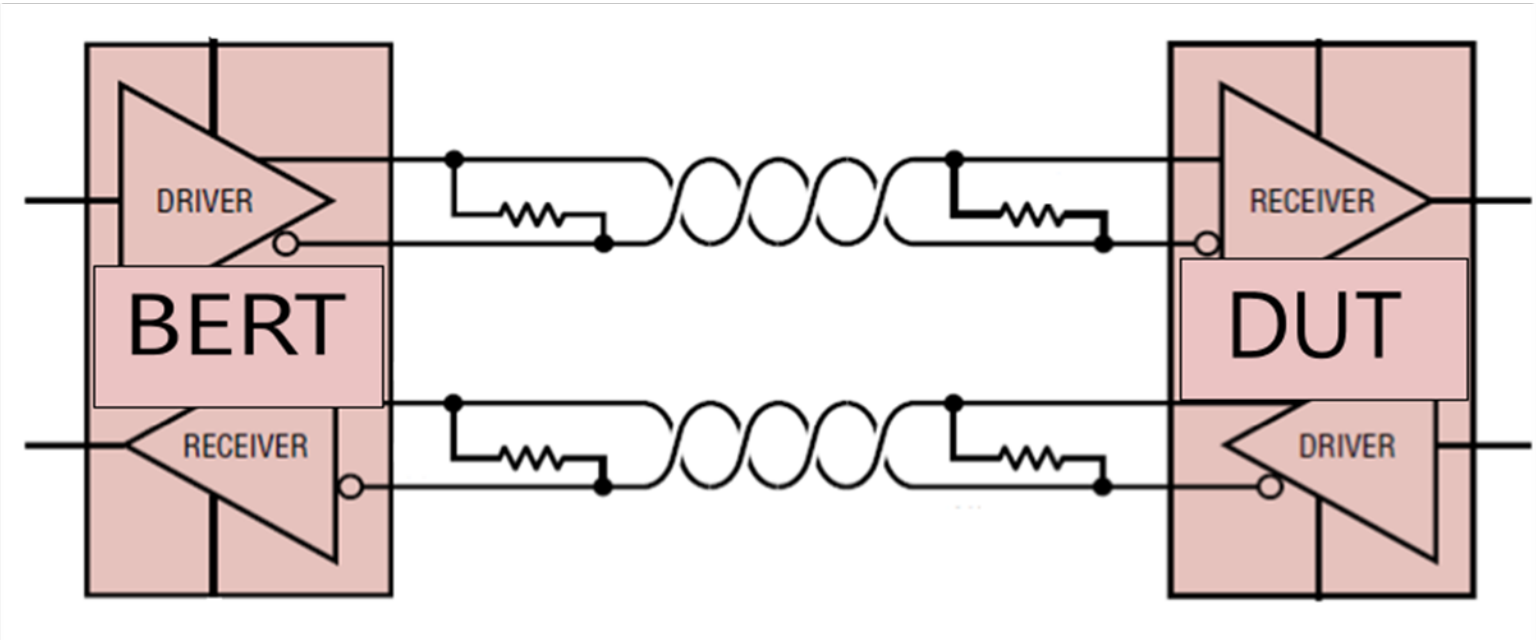
Introduction

driver interconnect receiver



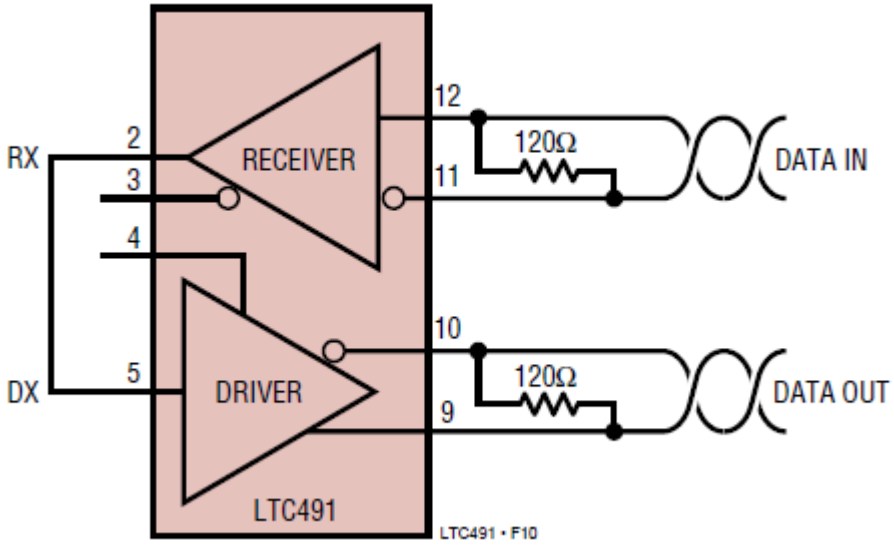


Introduction

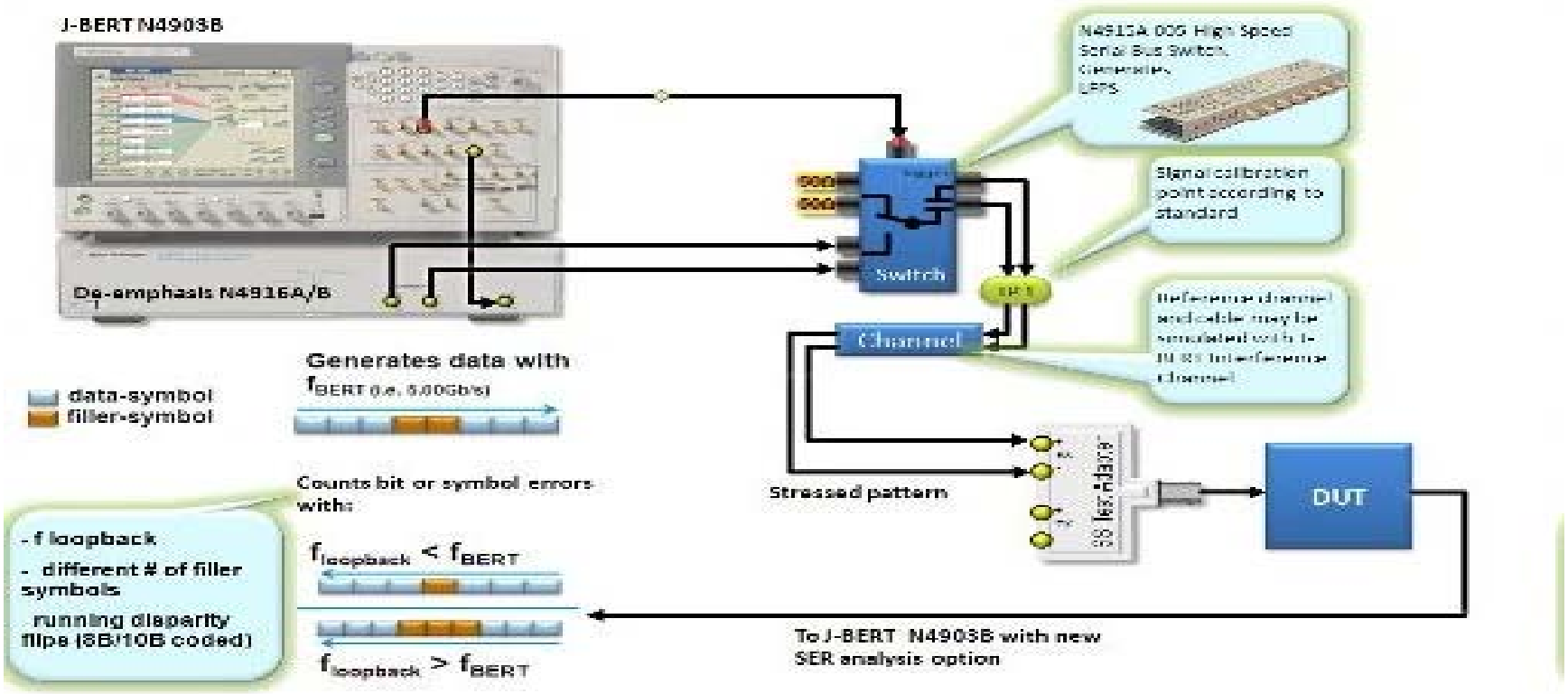


Picture From LVDS Transceiver device specification sheet by Linear Technologies

Introduction



Industry Usage



J-BERT simplifies USB3 Receiver Characterization

Industry Usage

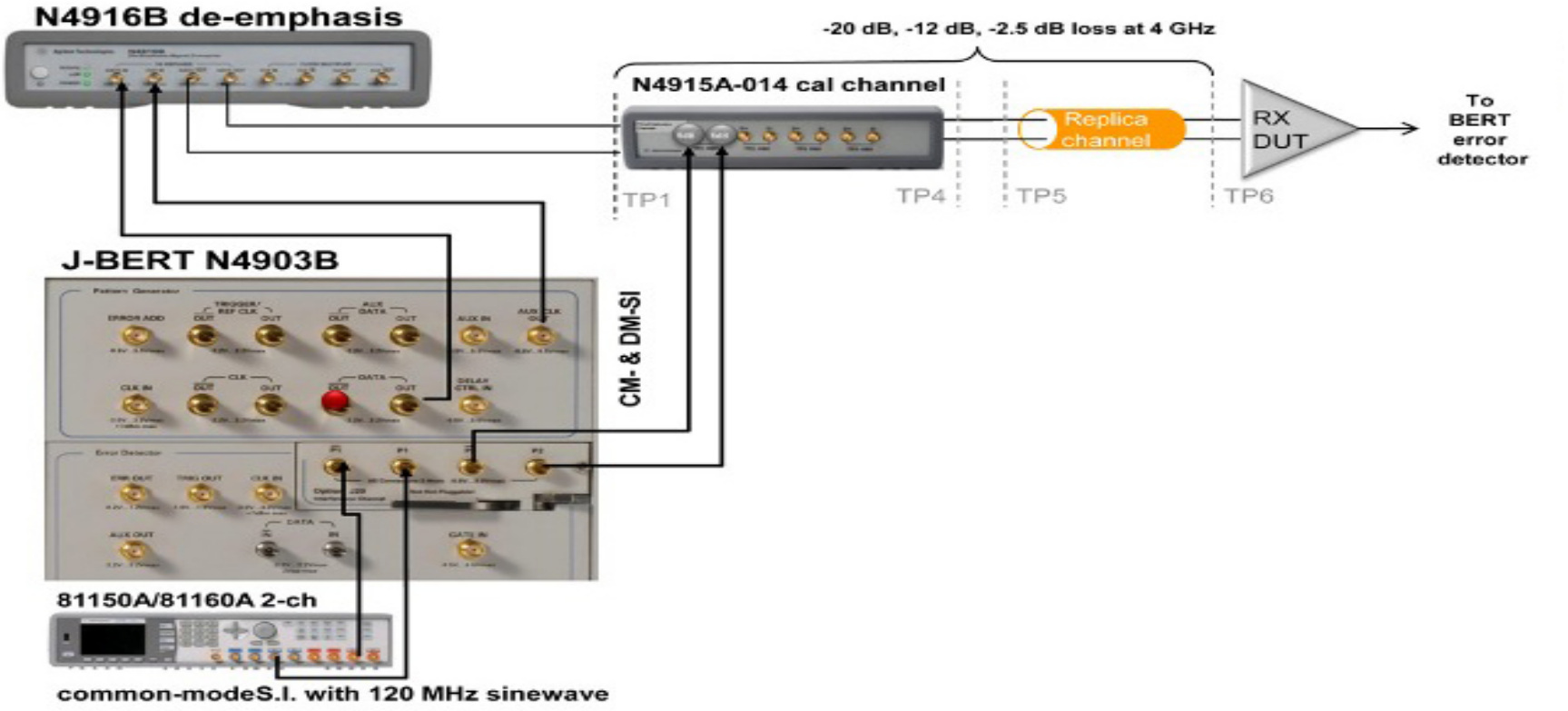


Figure: PCI Express 3.0 Receiver Test Setup with J-BERT N4903B

Industry Usage

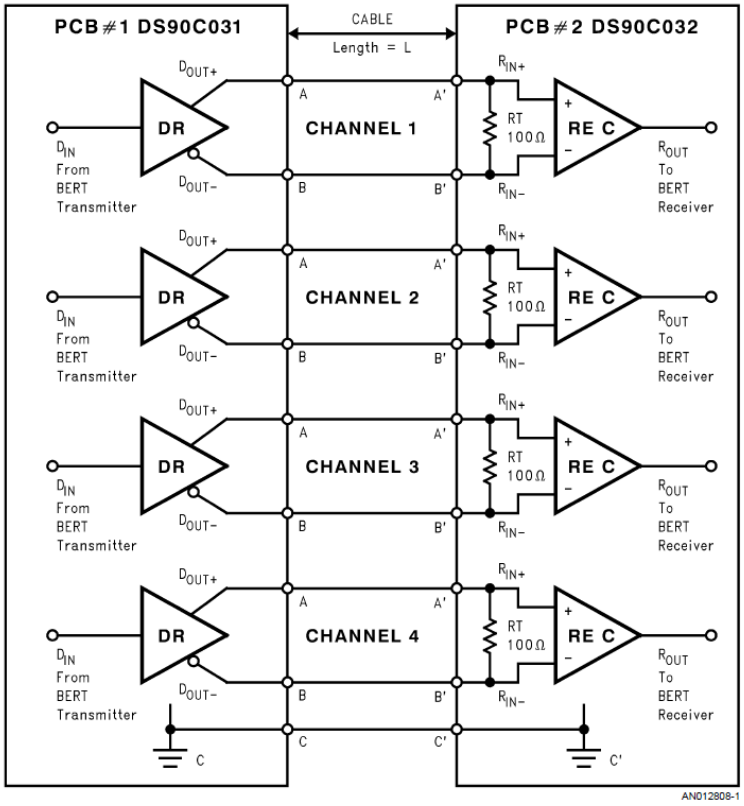


FIGURE 1. LVDS BER Test Circuit

TEST #3 Conditions:

Data Rate = 100 Mbps

Cable Length = 5 meter

PRBS Code = $2^{15} - 1$ NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #3 Results:

Total Seconds: 10,050

Total Bits: 4×10^{12}

Errors = 0

Error Rate = $< 1 \times 10^{-12}$

Introduction

- BER is a ratio between the number of bit errors transmitted and the number of bits received.

$$BER = \frac{N_{Err}}{N_{bits}}$$

- You must determine a confidence level (CL) at which you would like to operate at. you must find out the number of bits you need to transmit based on your CL.

$$N_{bits} = \frac{-\ln(1-CL)}{BER}$$

Introduction

- We then need to determine how much time we the device will needed to run in order to meet our BER and confidence level.

$$Time(seconds) = \frac{-\ln(1-CL)}{\text{bps} * BER}$$

Problem Definition

- Our objective is the development of an economical Bit Error Rate Tester (BERT) that has the ability to determine if the receiver component of the Device Under Test (DUT) is working satisfactorily.

- The signal must be transmitted through the LVDS Signal Specifications.

Current State of the Art

- The closest devices on the market to ours are the AGILENT BERT N4903A/B and the Tektronix BertScope are on the market.

- These are the complete BERT systems that cost 350K
  - Note: Our system is not meant to replace these, but to minimize their use

Test Conditions

- The testing setup for our test environment has been heavily explored and some methods have been determined. The setup is as follows:
- Transmitter with 100 Ohm termination
- Transmission Line with 100 Ohm differential impedance (SMA cables)
- Receiver with 100 Ohm termination

Tasks and Deliverables

Deliverables:

A working prototype which:

- Outputs a Bit Error Rate
- Outputs a status (Pass/Fail/Intermediate)
- Refreshes the BER and status displayed on the user interface at least every 15 seconds.
- Allows the user to start, pause, and restart the BERT

Design Implementation Choices

- The two options for our BERT implementation:
  - An FPGA based BERT
  - A microprocessor based BERT
- Two options for noise generation
  - AWGN
  - Johnston-Nyquist

Decision Matrix Microprocessor VS FPGA (BERT)

Decision	FPGA	Microprocessor
Usage 10	8	4
Ease of Generation 10	6	3
Speed 20	20	5
LVDS 25	19	3
Learning Curve 25	20	15
Cost 10	3	10
Total:	76	40

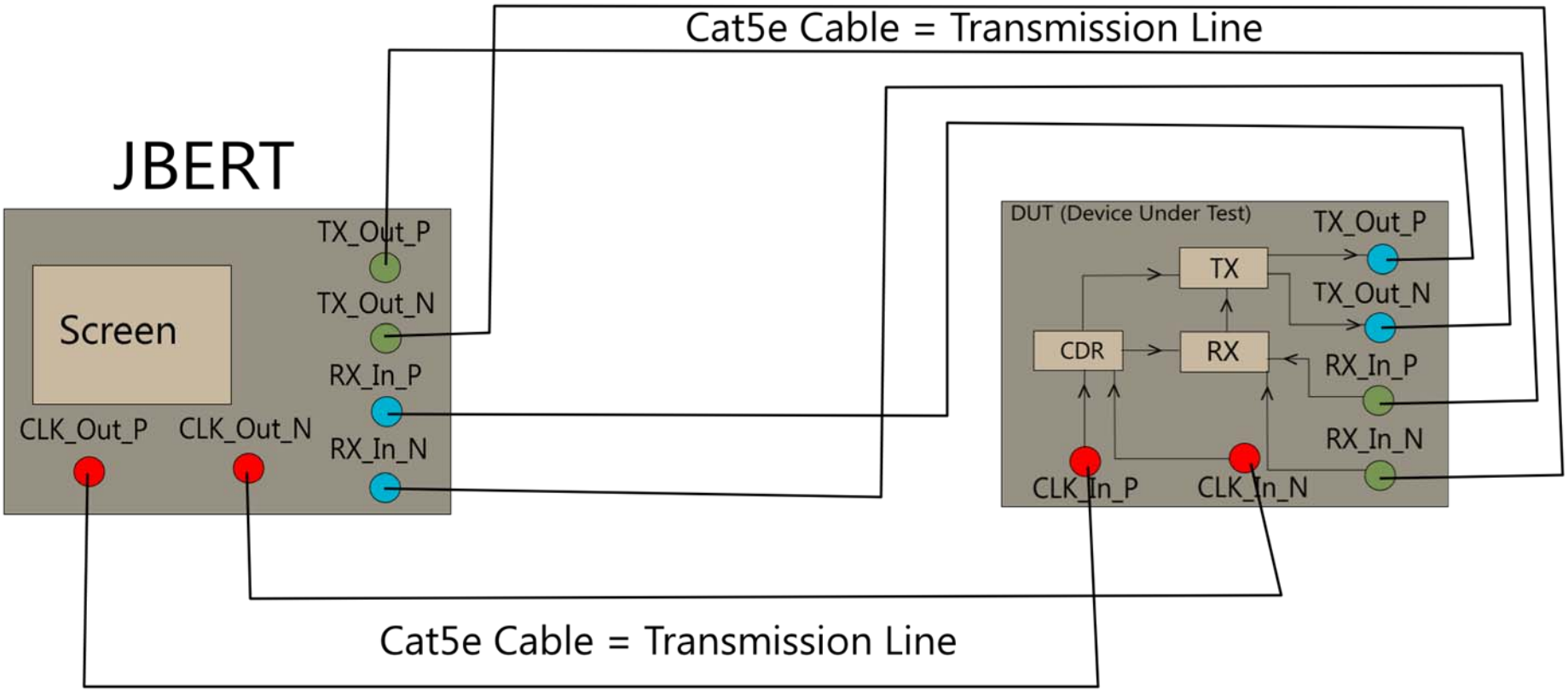
Decision Matrix AWGN VS Johnson-Nyquist Noise

Decision	AWGN	Johnson-Nyquist Noise
Usage 10	10	2
Ease of Generation 10	3	3
Model Accuracy 10	9	3
Total:	22	8

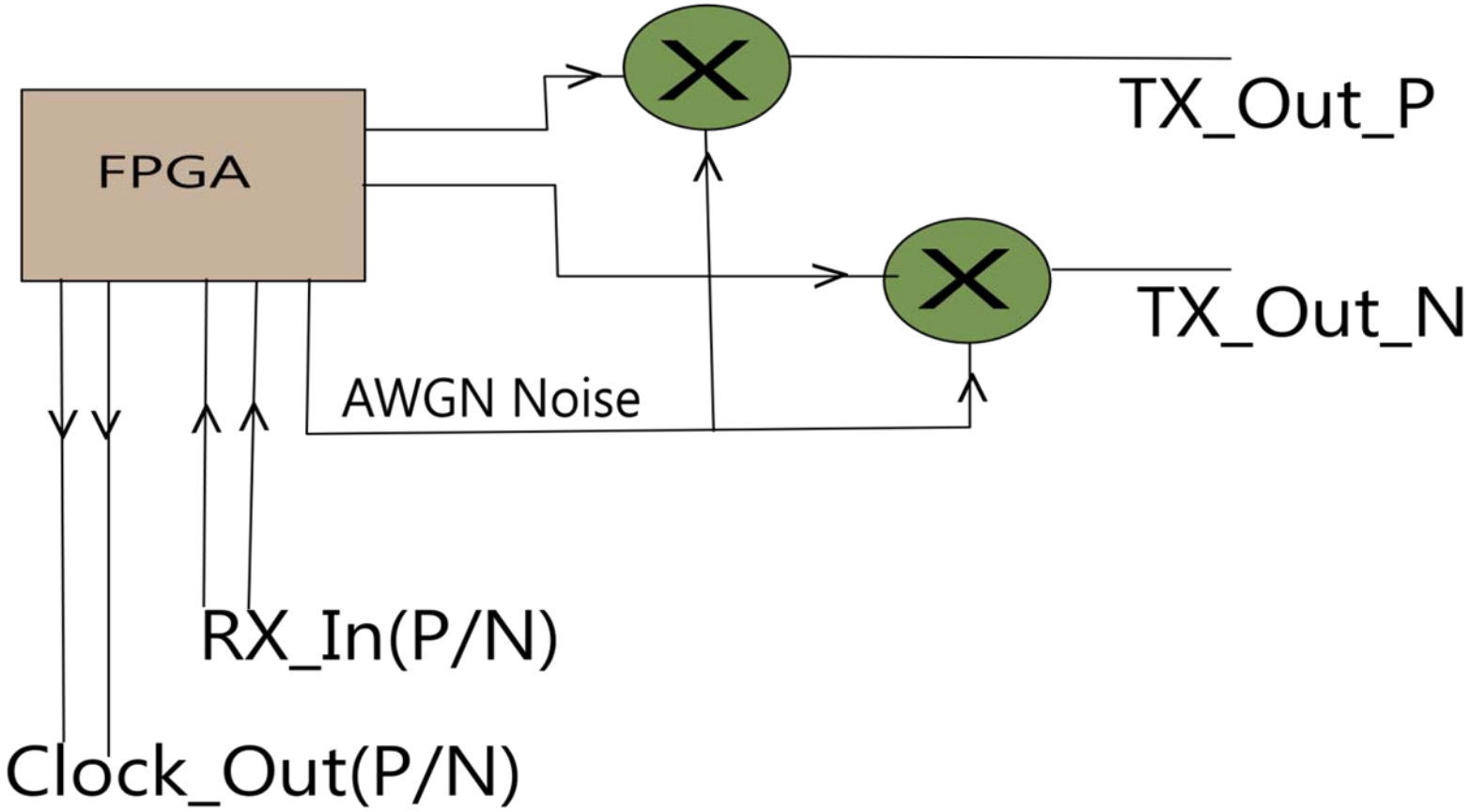
Engineering Approaches

- We propose an FPGA based Bit Error Rate tester which is composed of two main parts; the BERT; and the Additive White Gaussian Noise (AWGN) Generator.

Engineering Approaches

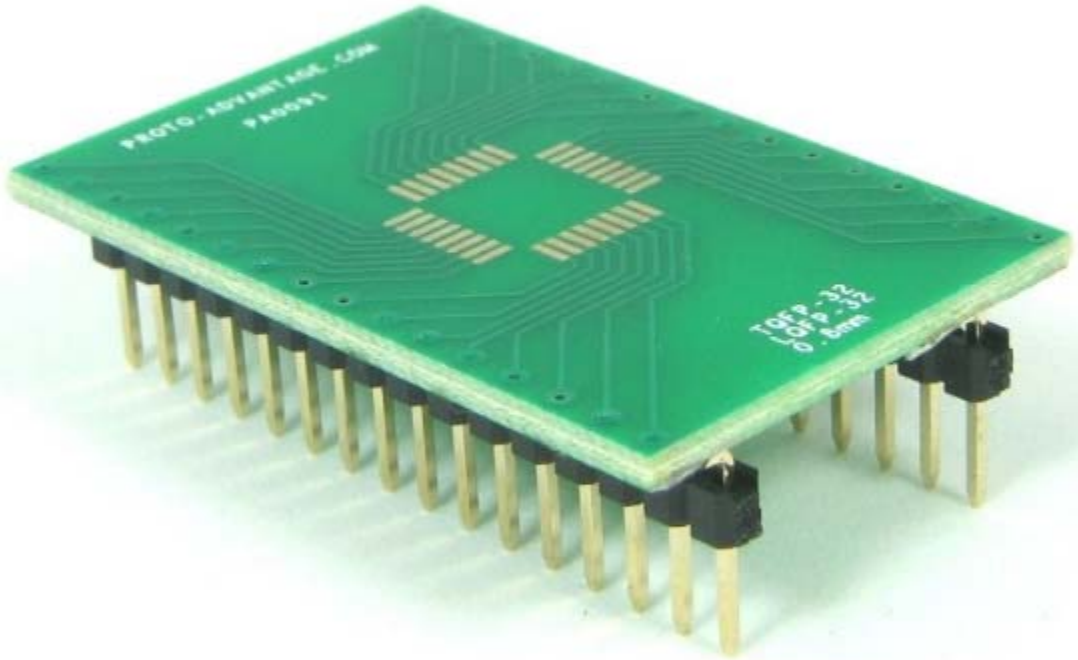


Engineering Approaches



Completed Tasks

- Ordered and received the main FPGA Board that will be used as the BERT

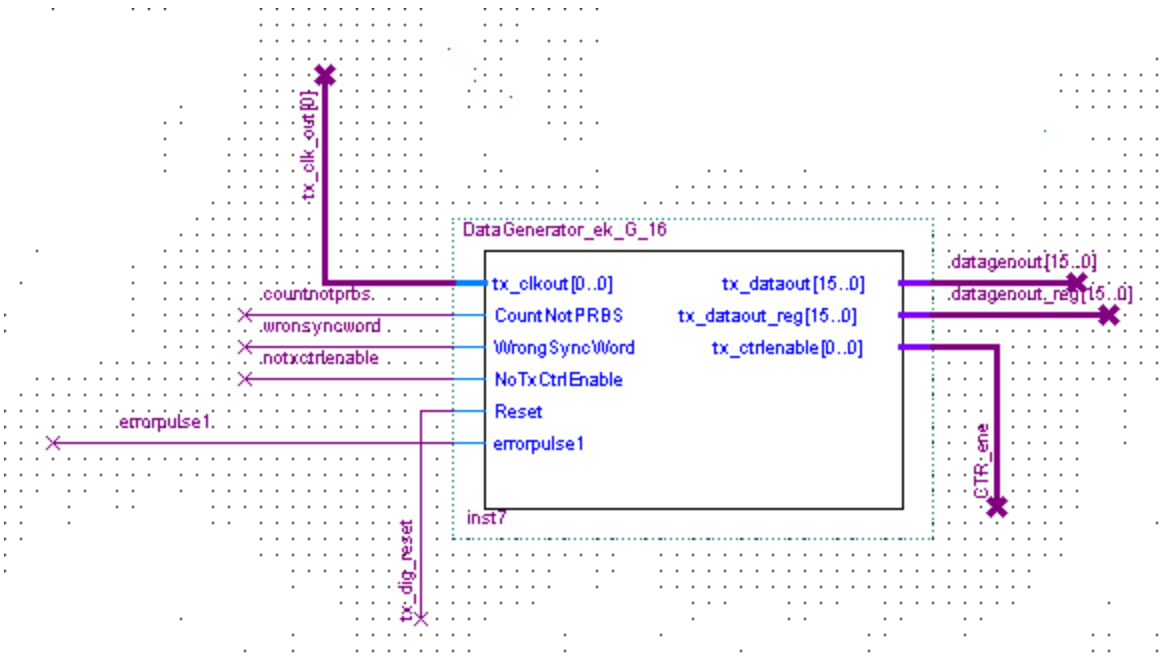

TQFP-32
0.8mm

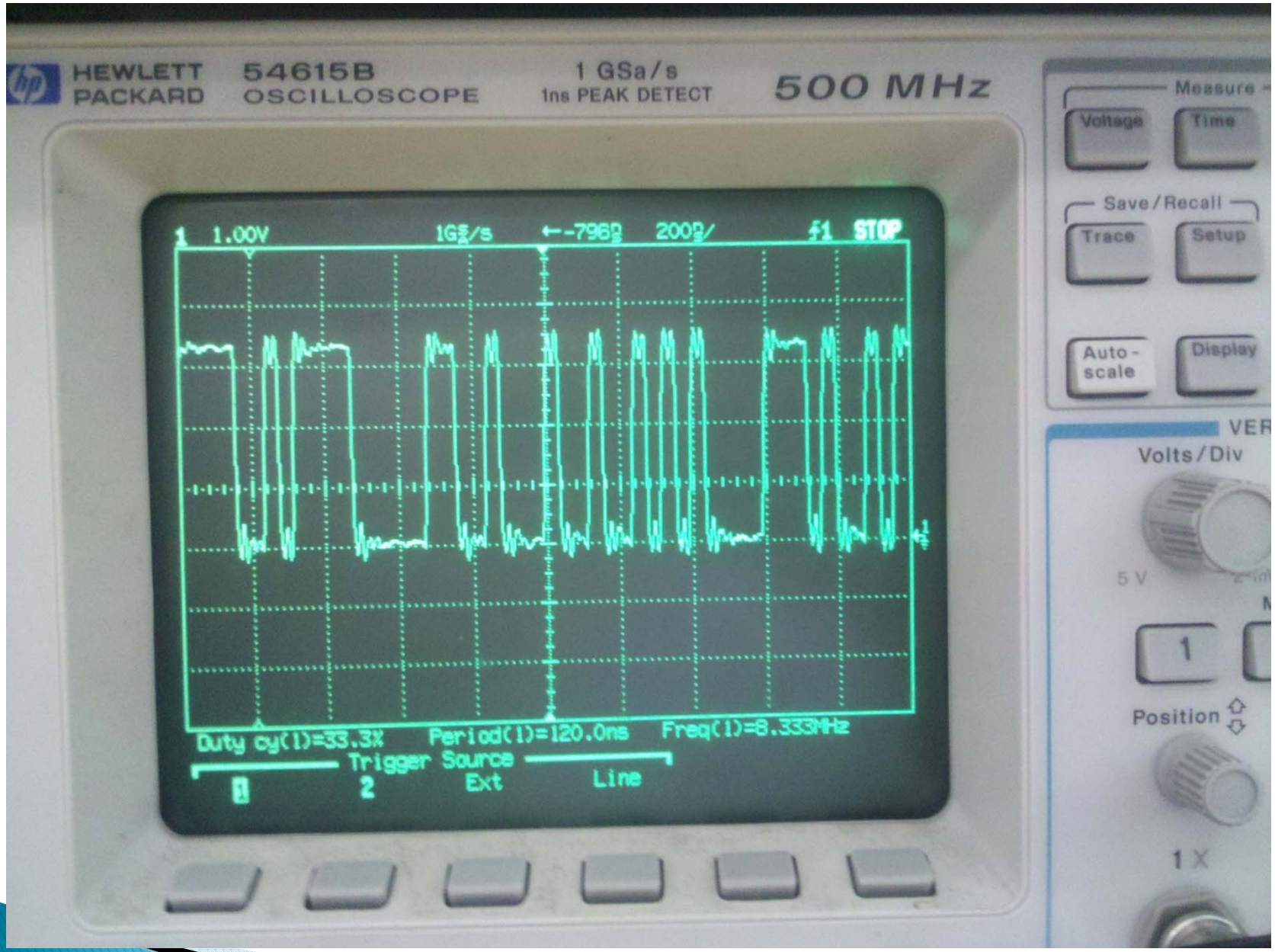
Completed Tasks contd

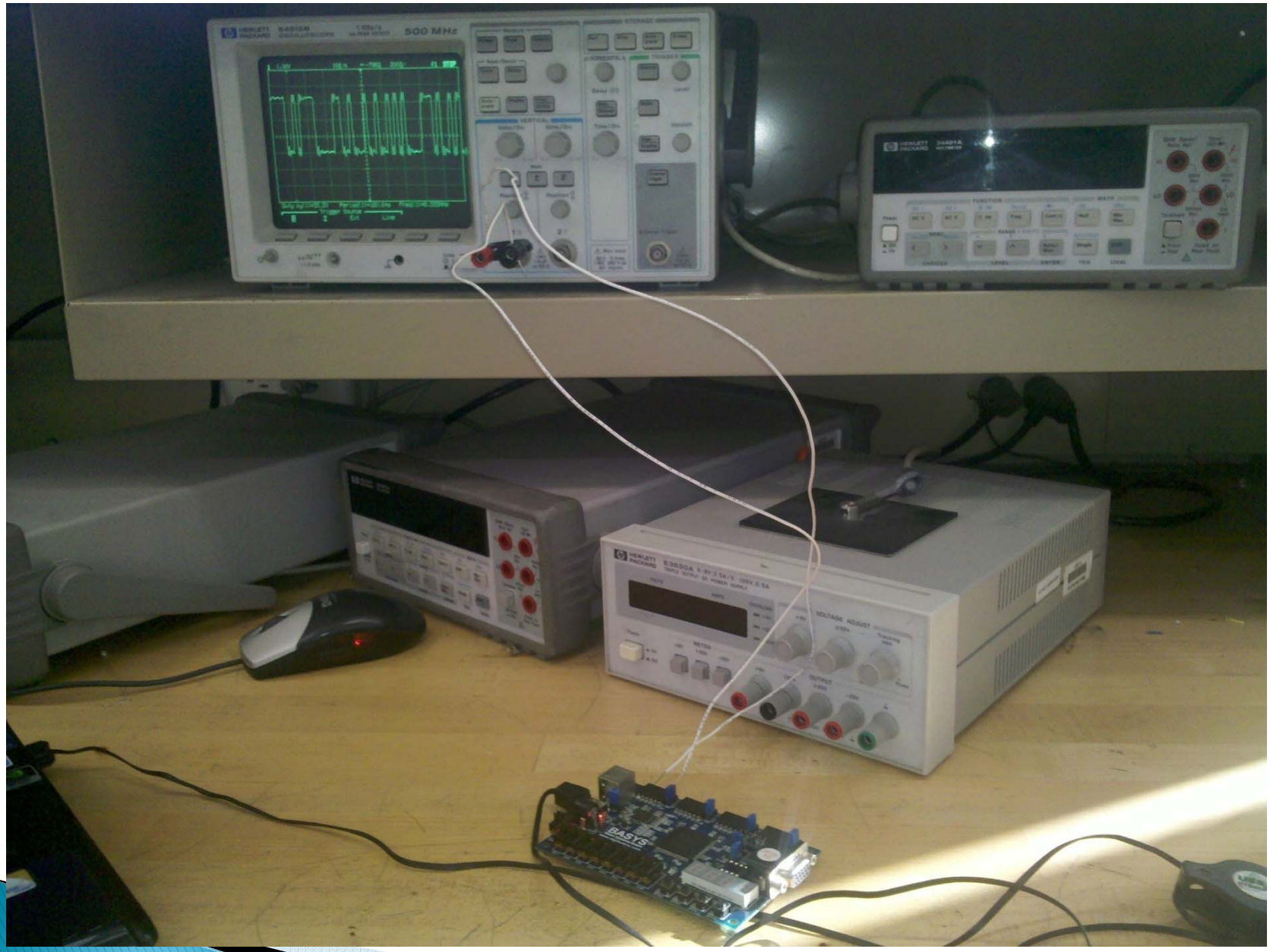
- Consulted with Dr Dimian
  - Confirmed that our noise addition technique is, OK as long as our frequencies are within an appropriate range

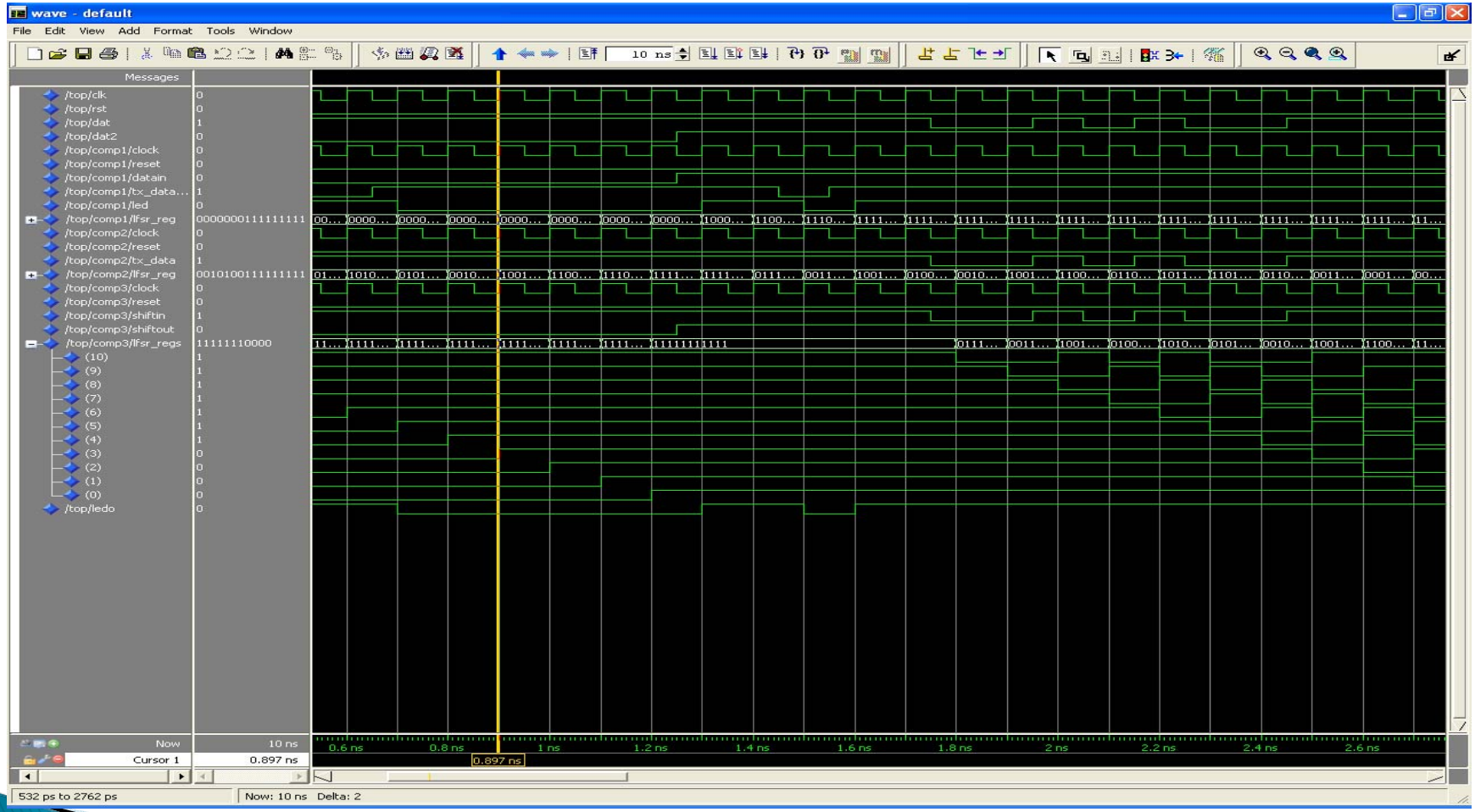
Completed Tasks Contd

- Create PRBS generator and Checker VHDL code



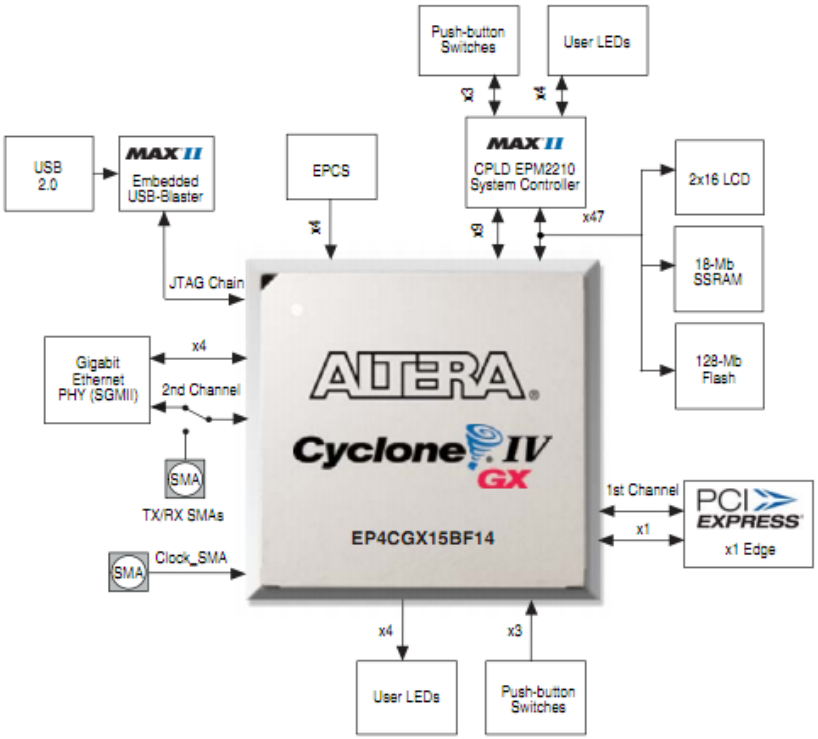

HEWLETT PACKARD
54615B OSCILLOSCOPE
1 GSa/s
1ns PEAK DETECT
500 MHz
Measure
Voltage
Time
Save/Recall
Trace
Setup
Auto-scale
Display
Volts/Div
5 V
Position
1X
1 1.00V
1GSa/s
←-796ps
200ps/
STOP
Duty cy(1)=33.3%
Period(1)=120.0ns
Freq(1)=8.333MHz
Trigger Source
1
2
Ext
Line


500 MHz
BASYS


wave - default
File Edit View Add Format Tools Window
Messages
/top/clk
/top/rst
/top/dat
/top/dat2
/top/comp1/clock
/top/comp1/reset
/top/comp1/datain
/top/comp1/tx_data...
/top/comp1/led
/top/comp1/lfsr_reg
/top/comp2/clock
/top/comp2/reset
/top/comp2/tx_data
/top/comp2/lfsr_reg
/top/comp3/clock
/top/comp3/reset
/top/comp3/shiftin
/top/comp3/shiftout
/top/comp3/lfsr_regs
(10)
(9)
(8)
(7)
(6)
(5)
(4)
(3)
(2)
(1)
(0)
/top/ledo
0000000111111111
0010100111111111
11111110000
Now
10 ns
Cursor 1
0.897 ns
0.6 ns
0.8 ns
1 ns
1.2 ns
1.4 ns
1.6 ns
1.8 ns
2 ns
2.2 ns
2.4 ns
2.6 ns
532 ps to 2762 ps
Now: 10 ns Delta: 2

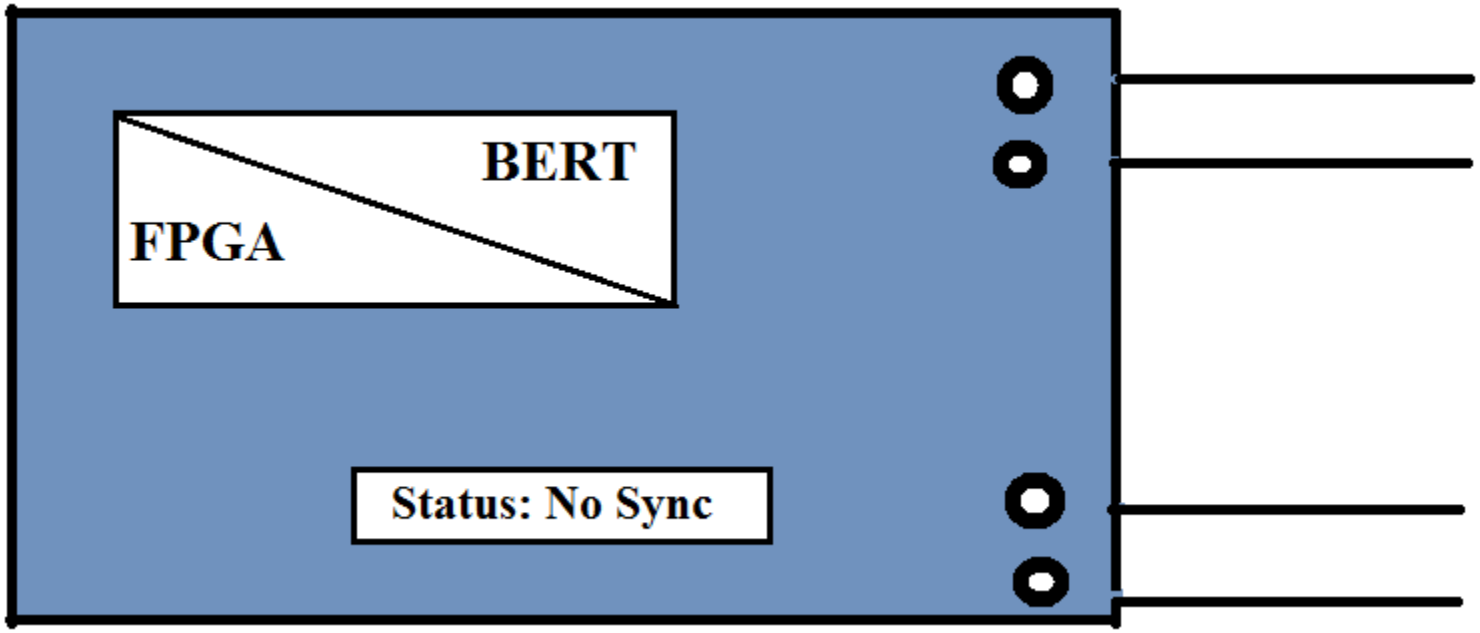
Current Issues

- Minute but detailed soldering must be done to our board in order to use the SMA component

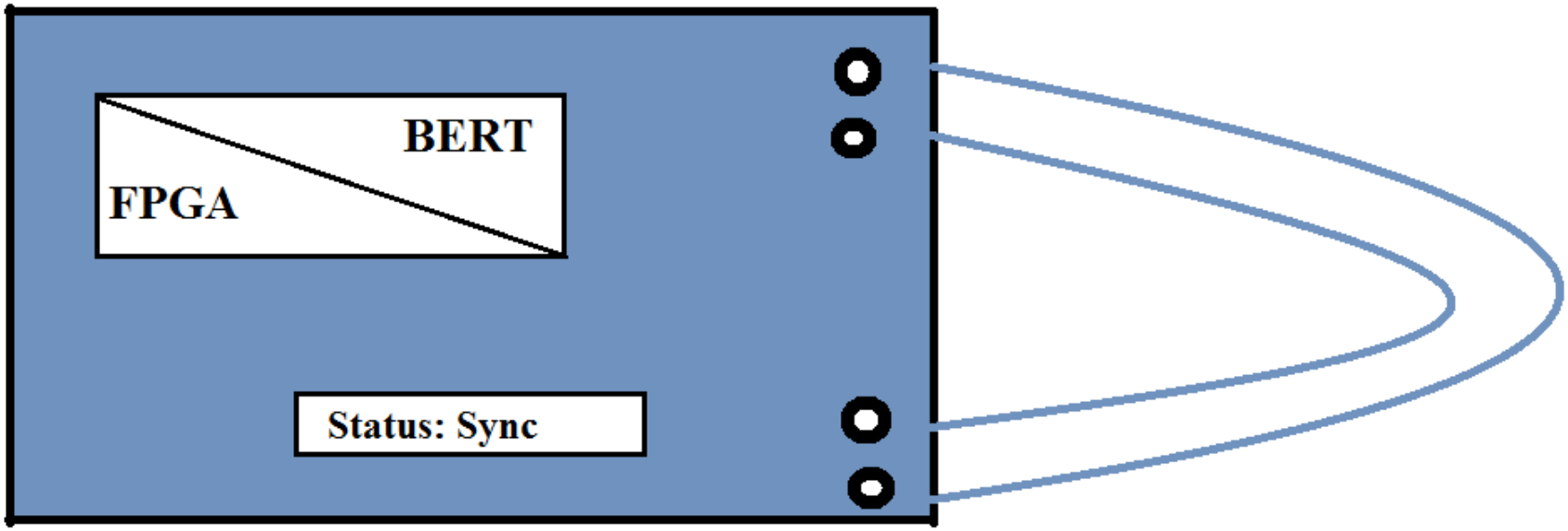


- Spoke with Altera (FPGA company) about rework
- Altera site in MD is sales only
- Forwarded to the FAE, dropped off board for rework
- Will not hold up progress for noise and receiver building

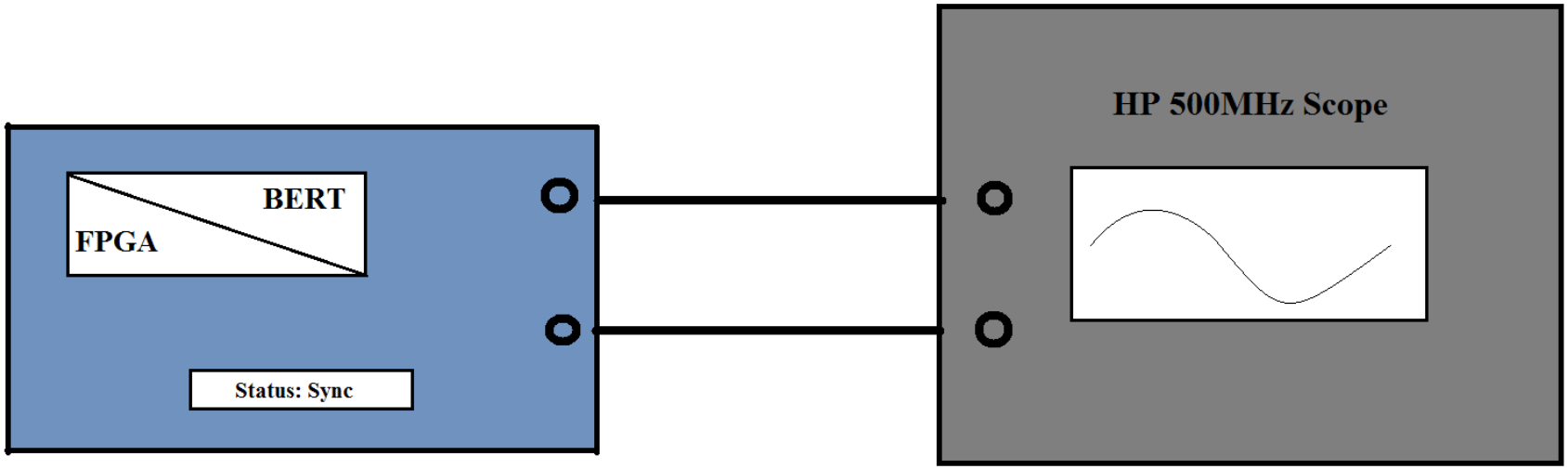
Proof of Concept 1



POC 1 contd



POC 2 contd



Tasks and Timeline

No	Task	Estimated Date	Actual Date
1	Look into current state of art	10/27/2010	10/27/2010
2	Select most appropriate solution	11/03/2010	11/03/2010
3	Consult with faculty on initial solution	11/03/2010	11/03/2010
4	1st Draft of proposal writing	11/10/2010	11/10/2010
5	Submission of 1st draft of proposal	11/17/2010	11/17/2010
6	Revision of proposal	11/17/2010	11/17/2010
7	Submission of proposal	12/01/2010	12/01/2010

Tasks andTimeline

No	Task	Estimated Date	Actual Date
8	Seek applicable hardware	12/05/2010	12/05/2010
9	Commence development of design	1/15/2011	1/15/2011
10	Order remaining components	3/04/2011	3/08/2011
11	Improve PRBS code	3/05/2011	In progress
12	Create AWGN code	3/07/2011	In progress
13	Build System	3/08/2011	In progress
14	Continuous improvement and testing	4/10/2011	In progress
15	ECE day presentation	4/15/2011	In progress

Total Cost

- Signal Integrity FPGA $400
- XCVR/CDR $75
- 8 SMA cables $95
- Others $45

- Total $615

References

- [1] Agilent Technologies, *How do I measure Bit Error Rate (BER) to a given confidence level,* Palo Alto, California
- [2] IEEE, *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) IEEE Std 1596.3-1996*
- [3] Linear Technologies, *Differential Driver and Receiver Pair LTC491 Device Manual*
- [4] Yongquan Fan, Zeljko Zilic, and Man Wah Chiang, *A Versatile High Speed Bit Error Rate Testing Scheme*