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# Lane Departure Warning System Progress Report III

*Saving lives, one alert at a time*

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# Overview

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# Problem Formulation

- Run-Off-Road (ROR) accidents are a leading cause of deaths on US roads and highways (1,550 fatalities, 71,000 injuries a year)<sub>(1)</sub>
- Design a lane departure warning system that provides a quick and effective alert to the driver to take a corrective action when car drifts unintentionally
- Main design components:
  - Input: Monitoring environment
  - Control Unit / Data Unit: Interpret the data from monitoring
  - Output: Alert system for the driver in the event of a lane drift

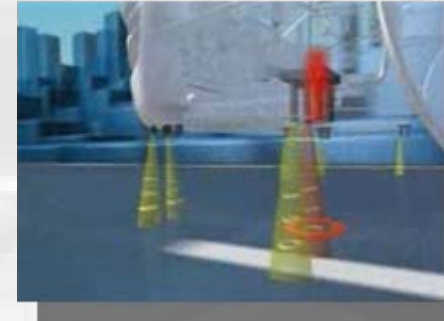


(1) - National Highway Traffic Safety Administration

# Solution Generation - Input

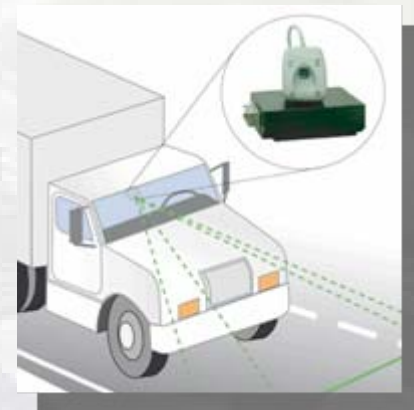
## Infra-red technology

- Constant bombardment of road with IR rays
- To leverage wavelength difference in reflected beam based on color of material hit (road or lane mark)
- Multiple sensors help determine extent of drift



## Camera technology

- Vision based system that uses camera sensors as the lane trackers
- Uses image recognition software and proprietary algorithms to determine when a vehicle drifts



# Top Design Selection - Input

## Input Component - Decision Matrix

Selection Criteria	Weight	INPUTS			
		IR sensors		Camera	
		Rating	Weighted Score	Rating	Weighted Score
Detection range	20	3	0.6	4	0.8
Weather effect	35	4	1.4	2	0.7
Cost	25	4	1	2	0.5
Power	5	4	0.2	3	0.15
Size and weight	5	4	0.2	3	0.15
Design Implementation	10	4	0.4	3	0.3
<b>Total Score</b>			<b>3.8</b>		<b>2.6</b>
<b>Rank</b>			<b>1</b>		<b>2</b>

# Solution Generation - Control Unit

## NetFPGA

- Uses 4 RJ-45 network ports for interface with wire-speed processing on all ports using FPGA logic



## Basys system board

- Allows various interfaces - USB port, 4 6-pin Pmod connectors, VGA, PS/2



## Spartan 3E Starter Board

- Added functionality of SMA connector for high-speed clock input



## Blackfin processor

- Allows access to Blackfin and FPGA pins for off-board connections and probing



# Top Design Selection – Control Unit

## Control Unit - Decision Matrix

		FPGA BOARDS							
Selection Criteria	Weight	NetFPGA		Basys System Board		Spartan 3E Starter Board		BlackFin	
		Rating	Weighted Score	Rating	Weighted Score	Rating	Weighted Score	Rating	Weighted Score
Processing Speed	10	3	0.3	3	0.3	3	0.3	4	0.4
I/O Connections	20	4	0.8	4	0.8	4	0.8	4	0.8
Cost	25	3	0.75	4	1	2	0.5	1	0.25
Power	15	2	0.3	3	0.45	2	0.3	1	0.15
Size	20	2	0.4	4	0.8	3	0.6	2	0.4
Programming Ease	10	3	0.3	3	0.3	2	0.2	3	0.3
<b>Total Score</b>			<b>2.85</b>		<b>3.65</b>		<b>2.7</b>		<b>2.3</b>
<b>Rank</b>			<b>2</b>		<b>1</b>		<b>3</b>		<b>5</b>

# Solution Generation - Output

## Light Emitting Diodes (LEDs)

- LED arrows to provide a visual driving alert



## Seat Vibrators

- Two sets of vibrators built into driver's seat (one set on each side—left and right)



## Buzzers

- Buzzer built in to provide audio alerts





# Top Design Selection – Output

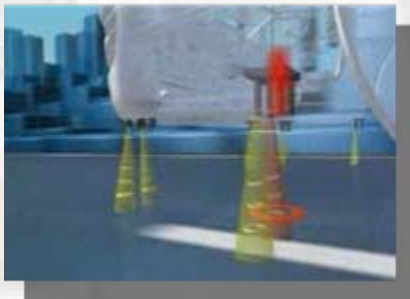
## Output Component - Decision Matrix

Selection Criteria		OUTPUTS					
		Buzzer		LEDs		Vibrator	
		Rating	Weighted Score	Rating	Weighted Score	Rating	Weighted Score
Response time	20	3	0.6	4	0.8	4	0.8
Disturbance to driver	20	2	0.4	4	0.8	4	0.8
Human Interaction	40	2	0.8	3	1.2	4	1.6
Cost	5	3	0.15	4	0.2	3	0.15
Power	15	4	0.6	4	0.6	4	0.6
<b>Total Score</b>			<b>2.55</b>		<b>3.6</b>		<b>3.95</b>
<b>Rank</b>			<b>3</b>		<b>2</b>		<b>1</b>

# Final Solution

## Input - Infra-red

- Constant bombardment of road with IR rays
- Multiple sensors help determine extent of drift



## Control Unit - Basys board

- Allows various interfaces – USB port, 4 6-pin Pmod connectors, VGA, PS/2



## Output - Seat vibrators and LEDs

- Seat vibrators built into seat
- LED arrows to provide a visual driving alert



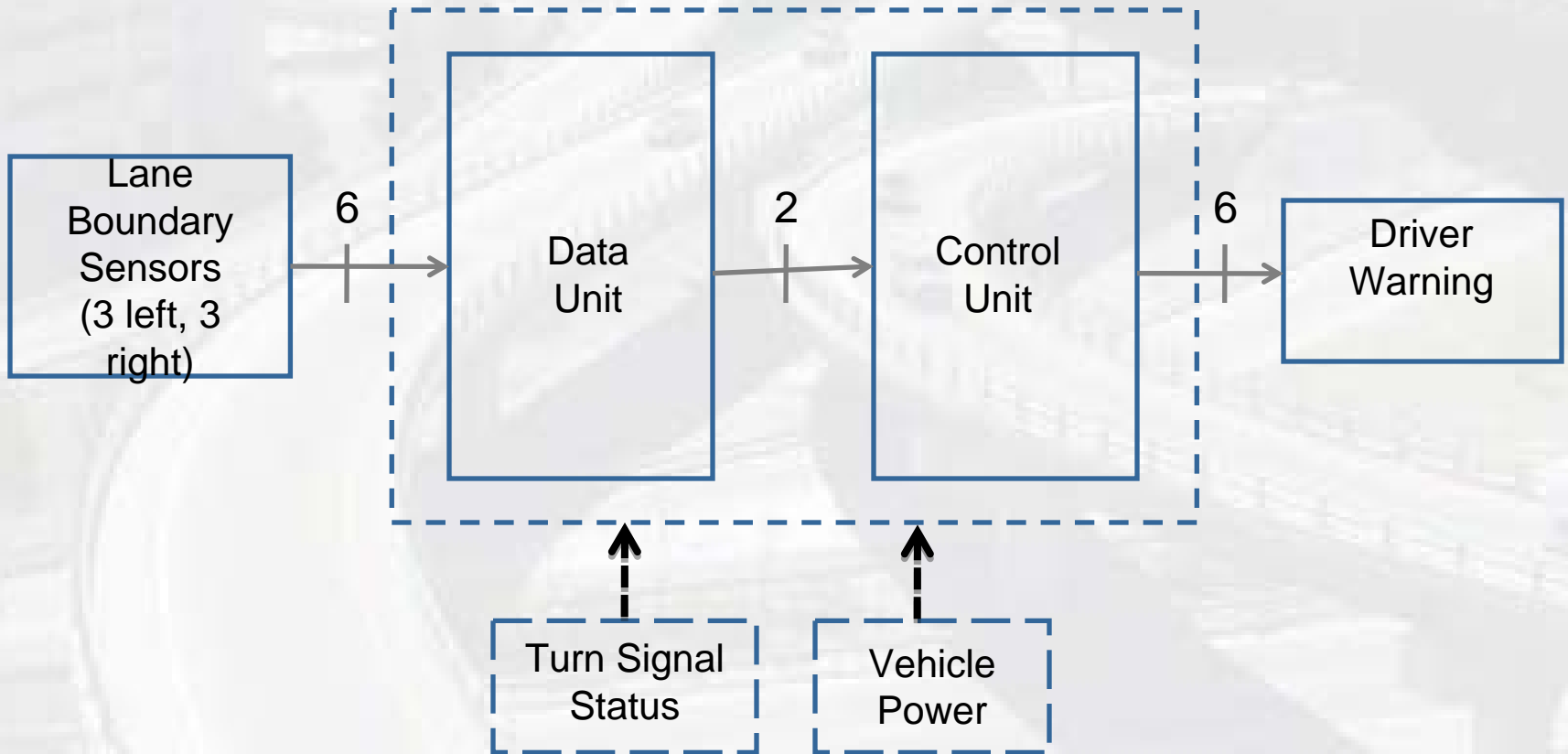
# Demonstration Prototype

- Miniature highway track with model RC car
- Life size driving seat that would mimic the user's driving experience
- Car will be remotely controlled to test functionality in different scenarios



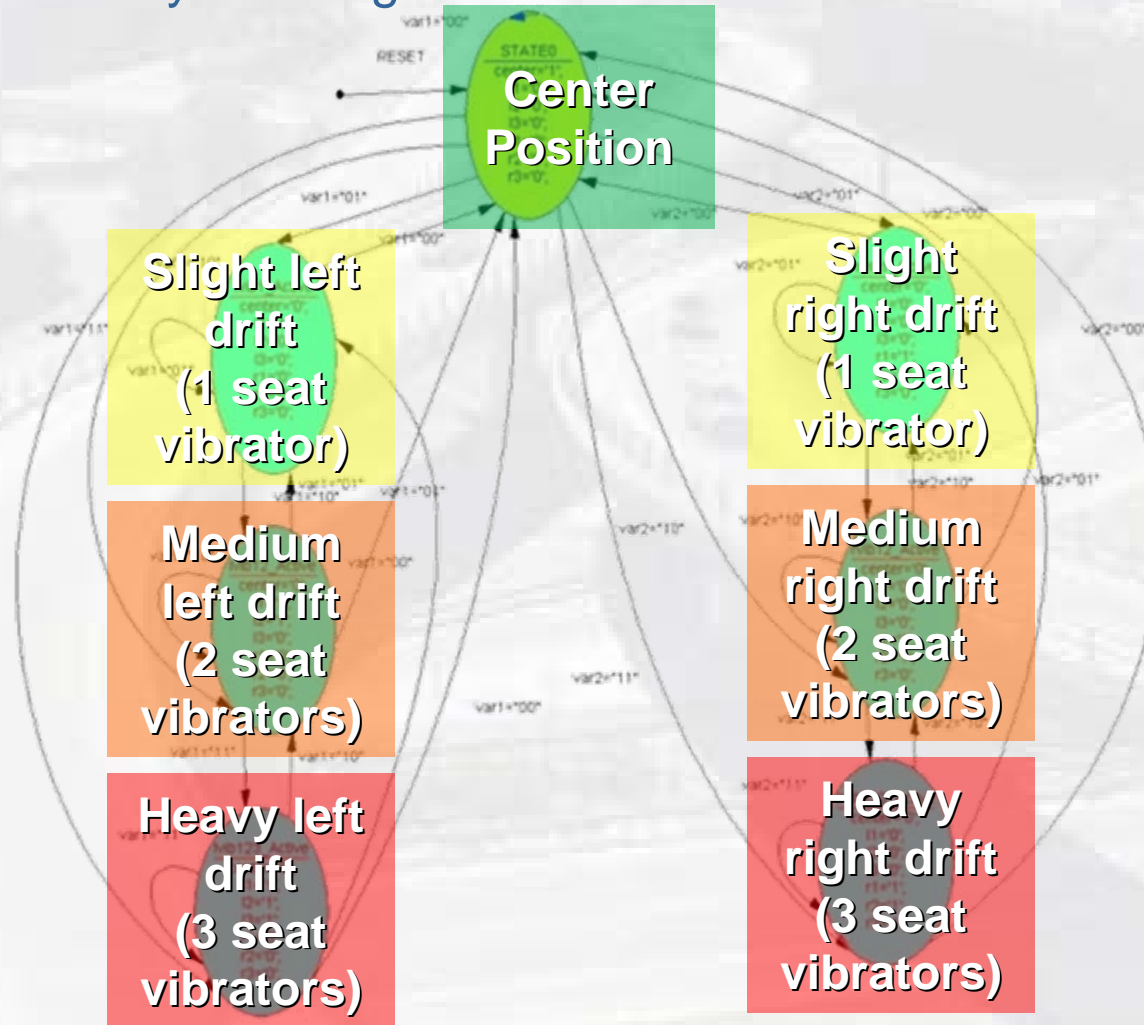
# Progress

## Development of System Algorithm and Simulation



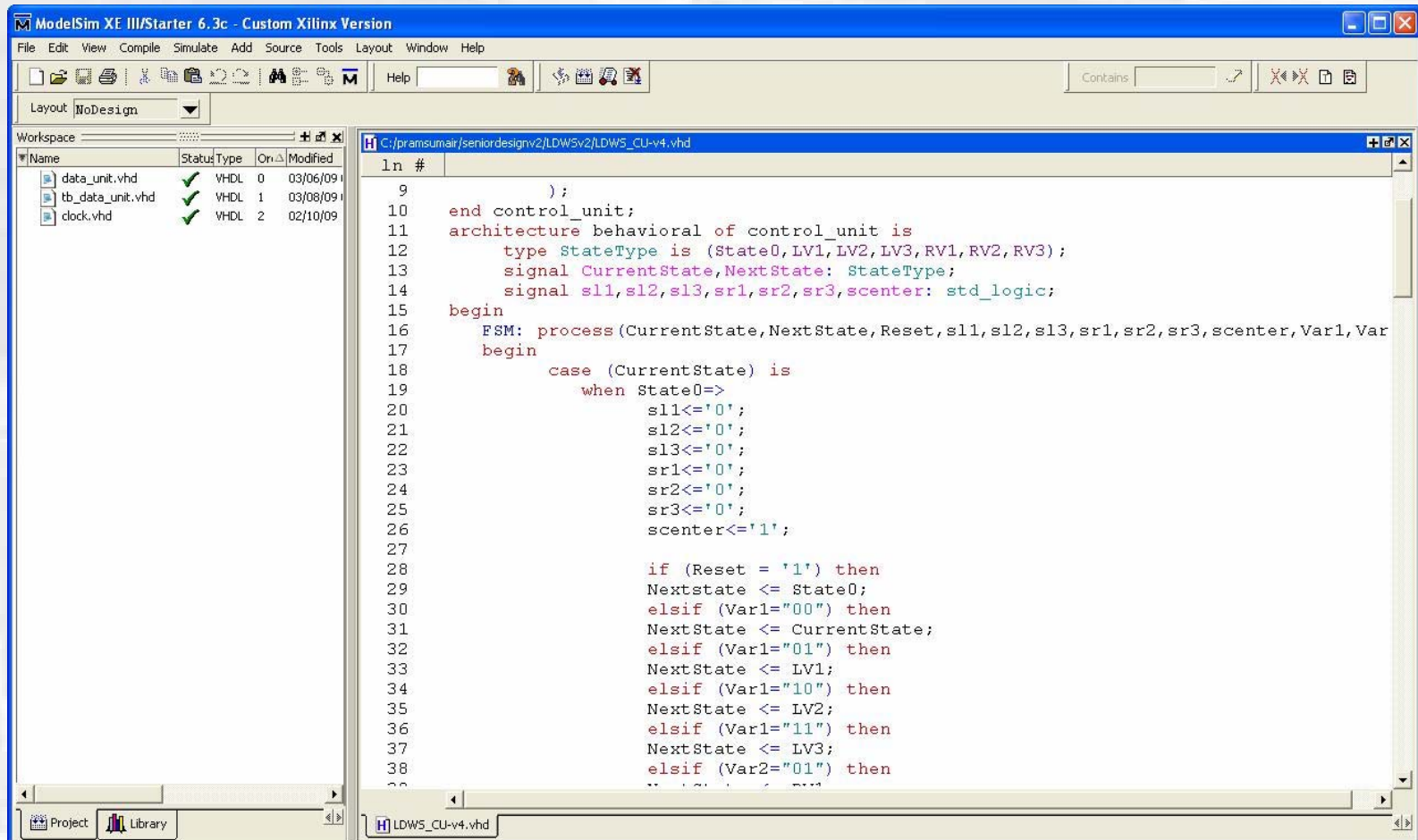
# Progress

## Development of System Algorithm and Simulation



# Progress

## Development of VHDL code

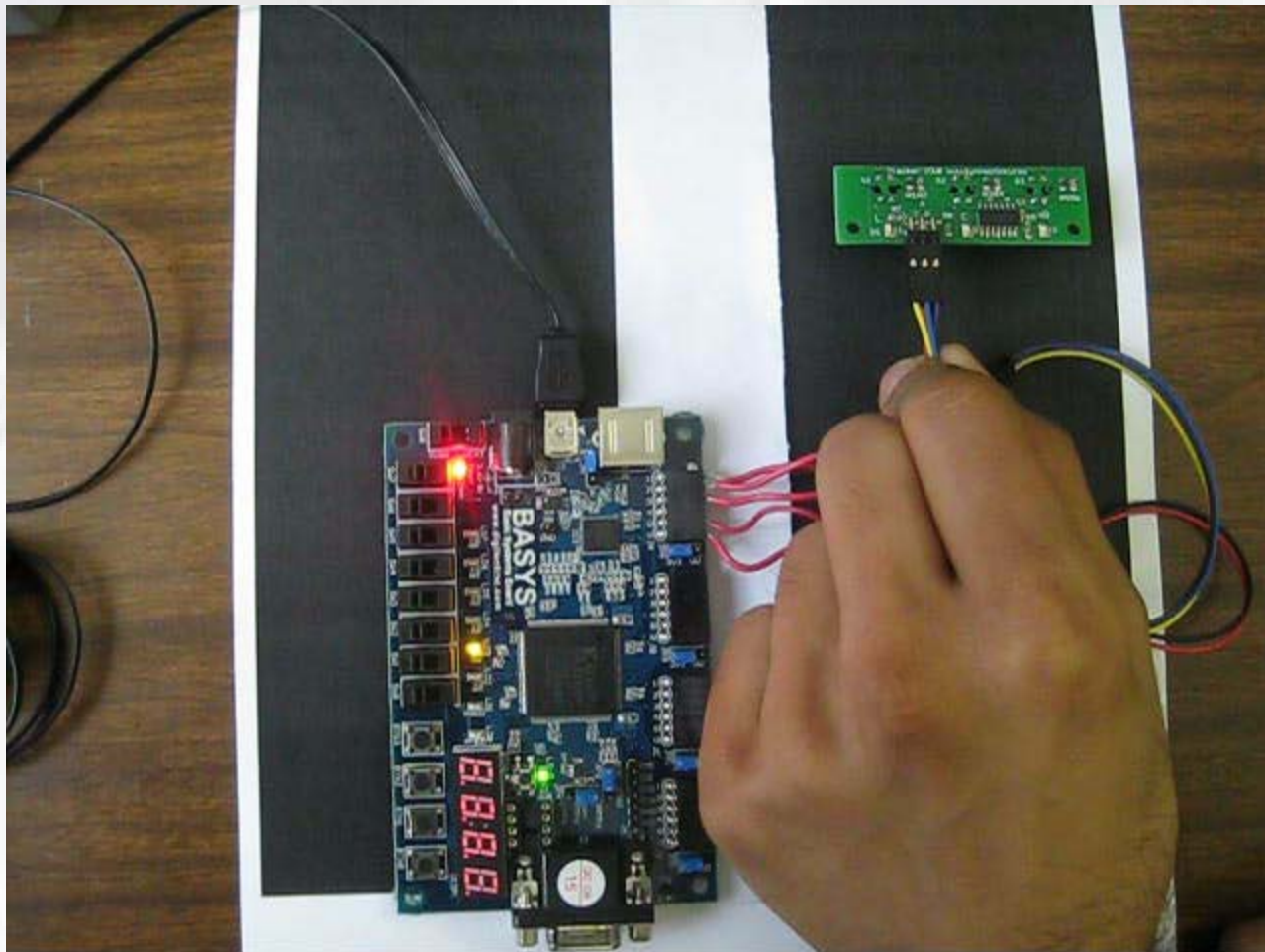


The screenshot displays the ModelSim XE III/Starter 6.3c - Custom Xilinx Version interface. The workspace on the left shows a project named 'LDWS\_CU-v4.vhd' with three VHDL files: 'data\_unit.vhd', 'tb\_data\_unit.vhd', and 'clock.vhd'. The main editor window shows the VHDL code for 'LDWS\_CU-v4.vhd'.

```
1 9
2  );
3  end control_unit;
4  architecture behavioral of control_unit is
5      type StateType is (State0, LV1, LV2, LV3, RV1, RV2, RV3);
6      signal CurrentState, NextState: StateType;
7      signal s11, s12, s13, sr1, sr2, sr3, scenter: std_logic;
8  begin
9      FSM: process (CurrentState, NextState, Reset, s11, s12, s13, sr1, sr2, sr3, scenter, Var1, Var
10         begin
11             case (CurrentState) is
12                 when State0=>
13                     s11<='0';
14                     s12<='0';
15                     s13<='0';
16                     sr1<='0';
17                     sr2<='0';
18                     sr3<='0';
19                     scenter<='1';
20
21                 if (Reset = '1') then
22                     Nextstate <= State0;
23                 elsif (Var1="00") then
24                     NextState <= CurrentState;
25                 elsif (Var1="01") then
26                     NextState <= LV1;
27                 elsif (Var1="10") then
28                     NextState <= LV2;
29                 elsif (Var1="11") then
30                     NextState <= LV3;
31                 elsif (Var2="01") then
32                     NextState <= RV1;
33             end case;
34         end process;
35     end architecture;
```

# Progress

## Hardware Implementation – Base System



# Issues

## Issues

Prototype car was not available

Hardware errors with FPGA board

## Solutions

- Used alternative RC car with similar functionality

- Debugged program and hardware until the errors were pinpointed and rectified



# Risk Monitoring / Management

## Development of System Algorithm and Simulation

### Risks

Logic errors

Coding issues

### Monitoring / Management

- Team critiques of individual algorithms
- Consult with faculty and knowledgeable upperclassmen
- Debug the program extensively
- Consult with faculty and knowledgeable upperclassmen

# Risk Monitoring / Management

## Hardware Implementation / Prototype Demonstration

### Risks

Demonstration props does not allow for proper testing of system functionality

Hardware errors with the FPGA board

### Monitoring / Management

- Consult with project and faculty advisors to come up with different demonstration methods
- Test all physical connections
- Extensively debug the program until the errors are pinpointed and rectified

# Milestones

- Ordered main component parts
- Developed initial LDWS system algorithm
- Implemented base system on FPGA board
- Tested initial driving scenarios



# Future Work

Week 1	Week 2	Week 3	Week 4	Week 5	Week 6	Week 7	Week 8	Week 9
8-Feb	15-Feb	22-Feb	1-Mar	8-Mar	15-Mar	22-Mar	29-Mar	5-Apr
1) Order Parts	1) Develop LDWS system algorithm	1) Use VHDL to develop the input module	1) Construct demonstration set	1) Test model on demonstration set	1) Develop user tests: Power User Test and Normal User Test	1) Create user documentation based on previous plan	1) Beta testing with select power users	1) Beta testing with normal users to ensure that user documentation is comprehensive and easy to follow
2) Use relevant block set to create simulation with Simulink®	2) Consult with faculty advisor (Dr. Gloster) to critique the algorithm	2) Use VDHL to develop the control unit module	2) Critique and test VHDL software	2) Update VHDL code in input module if needed	2) Develop and critique plan for user documentation		2) Update user documentation accordingly	

# Conclusion

- Use our implementation and evaluation plan to guide us to project completion
- Use all available resources to complete project
- Most valuable lesson: Adapting quickly to changing project dynamics



# Questions

