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Common-Emitter Amplifier

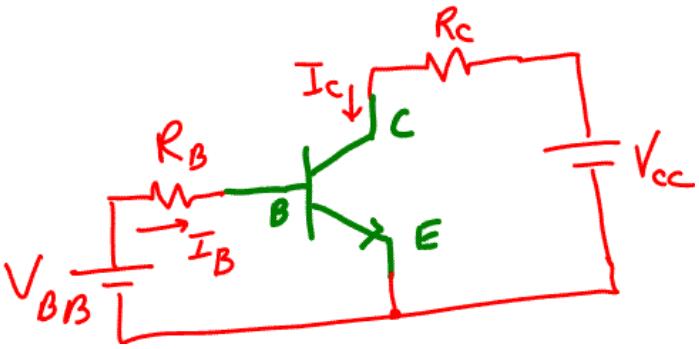
A. Before We Start

As the title of this lab says, this lab is about designing a Common-Emitter Amplifier, and this in this stage of the lab course is premature, in my opinion, of course. How can one design a BJT amplifier only after one simple characteristic experiment? Maybe students are all brilliant or this subject is already covered in a class, extensively. Even with that assumption, experiment with a BJT amplifier should come before asking for designing such circuit. Even before that, a much simpler circuit investigation would be more beneficial to understand the Common-Emitter Amplifier.

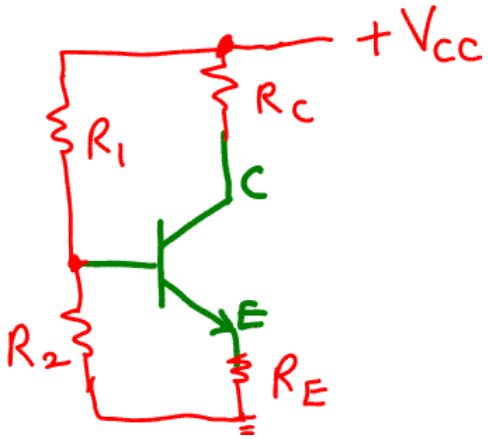
B. Common-Emitter Amplifier Experiment

B.1 Theory

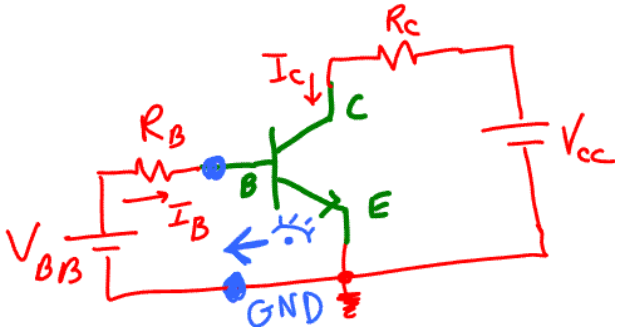
Let's start our discussion on Common Emitter Amplifier (CE Amp), rather from the first BJT Lab, in which we discussed about Base voltage and Collector voltage in the operating region. To revive your memory, here I bring the CE circuit configuration. This DC voltage application into BJT is usually called "DC Biasing"



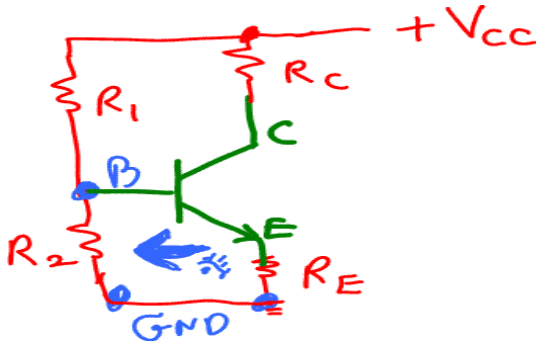
In CE circuit, however, more popular biasing method is to supply single DC voltage (instead of two: V_{BB} and V_{CC}), also with a resistor at the Emitter. From this circuit, let's calculate the voltage corresponding to V_{BB} and the resistance corresponding to R_B. From the upper circuit. Between B and GND, the voltage is V_{BB} and equivalent resistance is R_B.



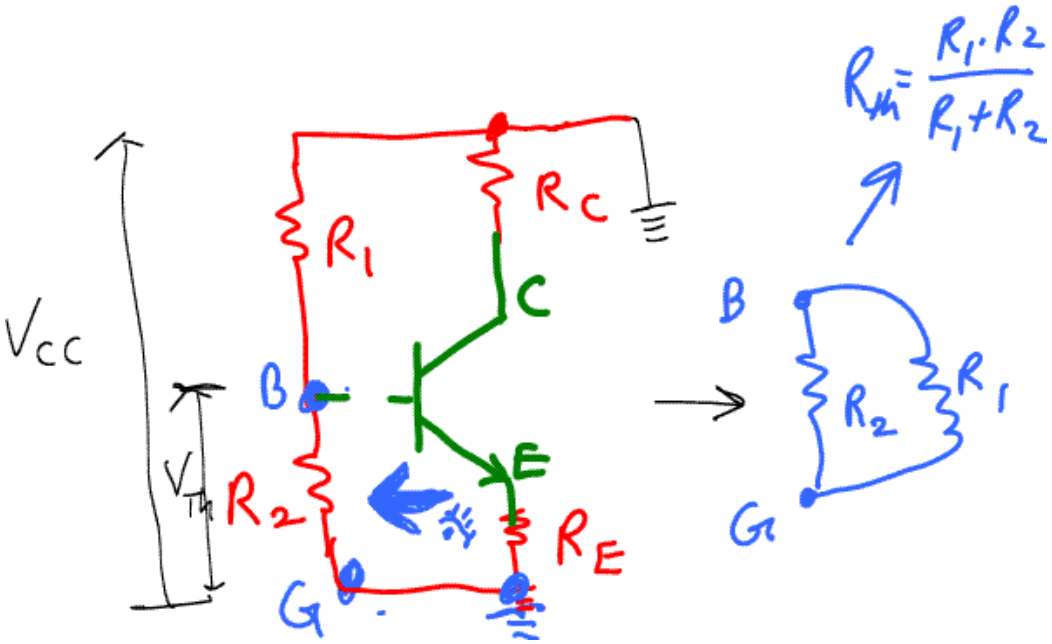
Similarly, on the single voltage biased circuit, we also try to find the equivalent voltage and resistance seen at the terminals B and GND.



Here we apply Thevenin theorem. The thevenin voltage can be acquired by finding the terminal voltage (at B and GND) after opening the terminal. Opening the terminals means we cut the wire between the Base and the junction of R1 and R2.

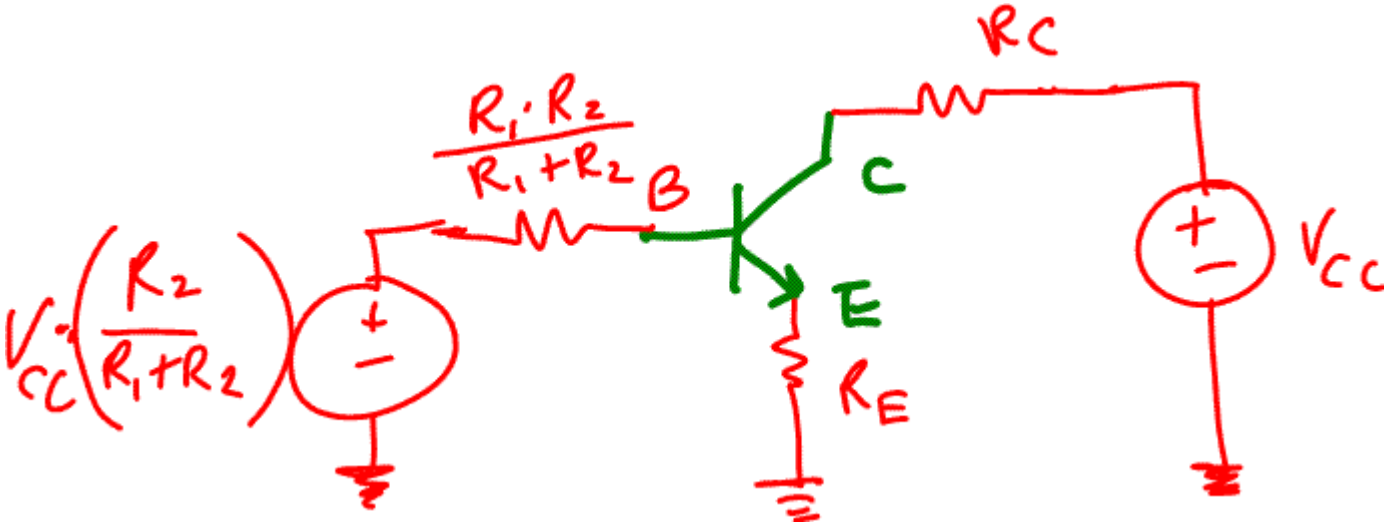


When you open the circuit (See below), the terminal voltage is nothing but the voltage across R2, and R1 and R2 are in series with voltage V_{CC} across the series resistors. So we can apply "voltage divider" to find the terminal voltage: $V_{th} = V_{CC} \cdot \dfrac{R_2}{R_1 + R_2}$



How about Thevenin resistor? Since we have only independent voltage source VCC, we apply the "Input resistance method" which gets the equivalent circuit at the terminals after deactivating the voltage source. Deactivation of a voltage source means shorting the voltage source, we have the two parallel resistors R1 and R2 at the terminals of B and GND. Therefore, Thevenin resistance is $R_{th} = \dfrac{R_1 \cdot R_2}{R_1 + R_2}$

Finally we have the following circuit which exactly corresponds to the initial biasing circuit we studied in the BJT 1 Lab.



OK. Now it's time to consider a CE Amp circuit. By the way, when we say amplifier, we usually mean by amplifying AC signal. This means that the biased voltages are DC values and they are not to be disturbed. At the same time, AC wants to be riding over the DC and gets some boost. Also, the DC bias voltage should not interrupt the input AC signals and the amplified output AC signal. In other words, we can picture this way. A castle surrounded by circling high wall, with entrance and exit gates, is governed by a DC system. Whatever entered through the

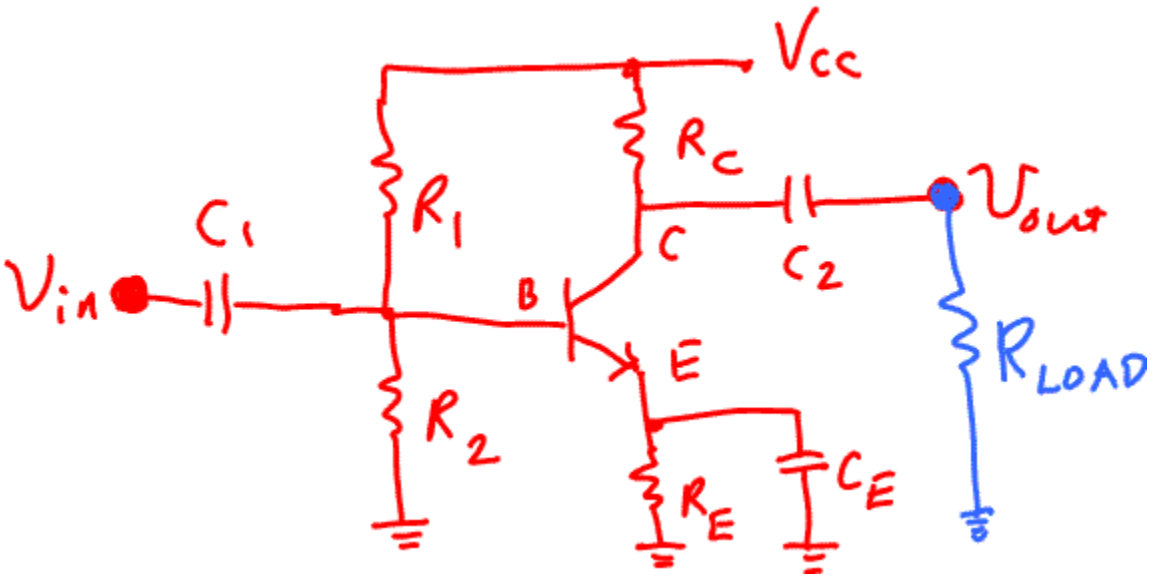
entrance gate is exiting the exit gate with amplification. What a great castle it must be! However, the DC system inside the castle cannot be leaked through the gates. It's a tightly controlled system. Therefore the gates' other function is to block any leakage from the castle to outside world. The castle here is the base voltage divider biased circuit. And the gates are realized by coupling capacitors. The size of the capacitor corresponds to the size of the gate. Smaller gates pass only smaller object, while larger gate passes through larger object.

Actually there is one more device inside the castle to nullify any effect of those foreign objects entering the castle, while keeping the DC system stable and intact. This in circuit formation is a bypass capacitor at the Emitter.

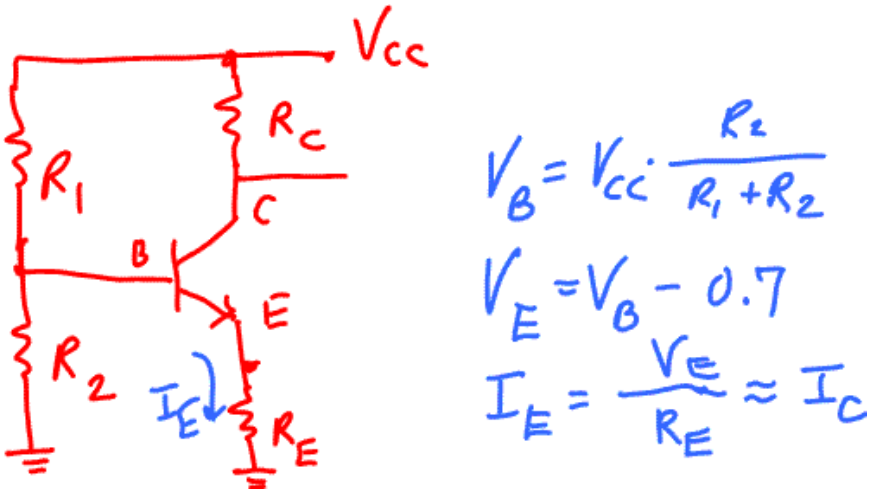
The circuit below is one of the popular AC Amp circuits. C_1 and C_2 are coupling capacitors, and C_E is the bypass capacitor. As you can see, all other elements are exactly the same as the circuit we first discussed. The size, and its impact on frequency response of the whole circuit, of C_1, C_2, and C_E will be discussed shortly.

DC Analysis

DC analysis of the circuit is very important in that (i) it makes sure DC biasing is all right and (ii) it finds I_E which (indirectly) is used for voltage gain of the circuit.



In DC analysis, we assume that there are only DC sources. In the circuit above, when we assume that V_{in} is a DC source, that DC source cannot cross coupling capacitor C_1. Why? Capacitor stores DC energy. In other words capacitor works as a open circuit for DC source. That means the DC-only circuit would look like this:



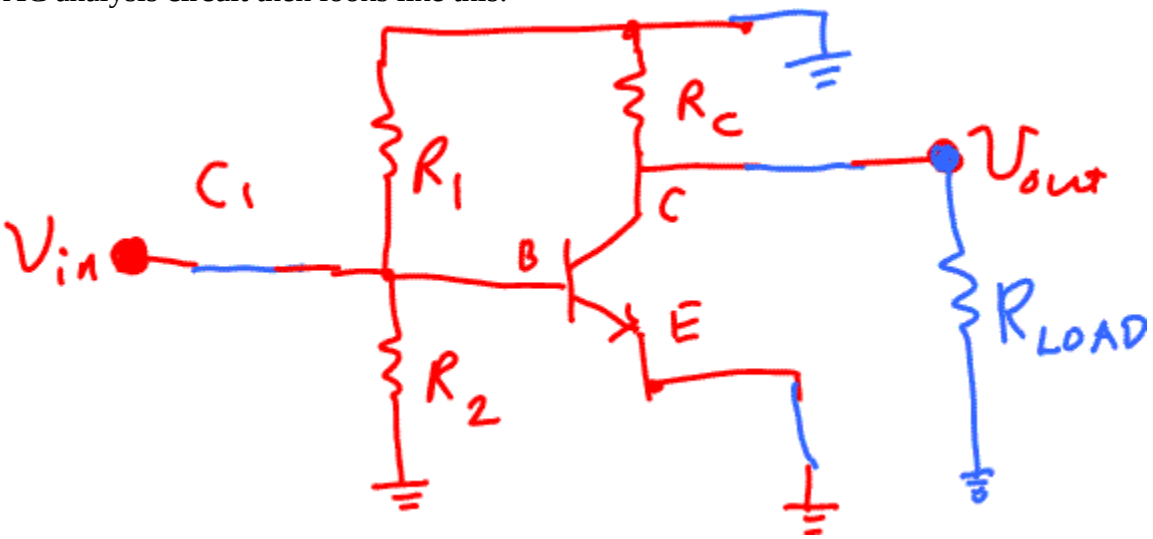
By the voltage divider rule, the Base voltage is $V_B = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$

Then the voltage at the Emitter is 0.7 V lower than VB (typical silicon diode voltage drop), then the Emitter current I_E is determined by $I_E = \frac{V_E}{R_E}$. If we assume that Base current is negligible, then $I_C = I_E = \frac{V_E}{R_E}$

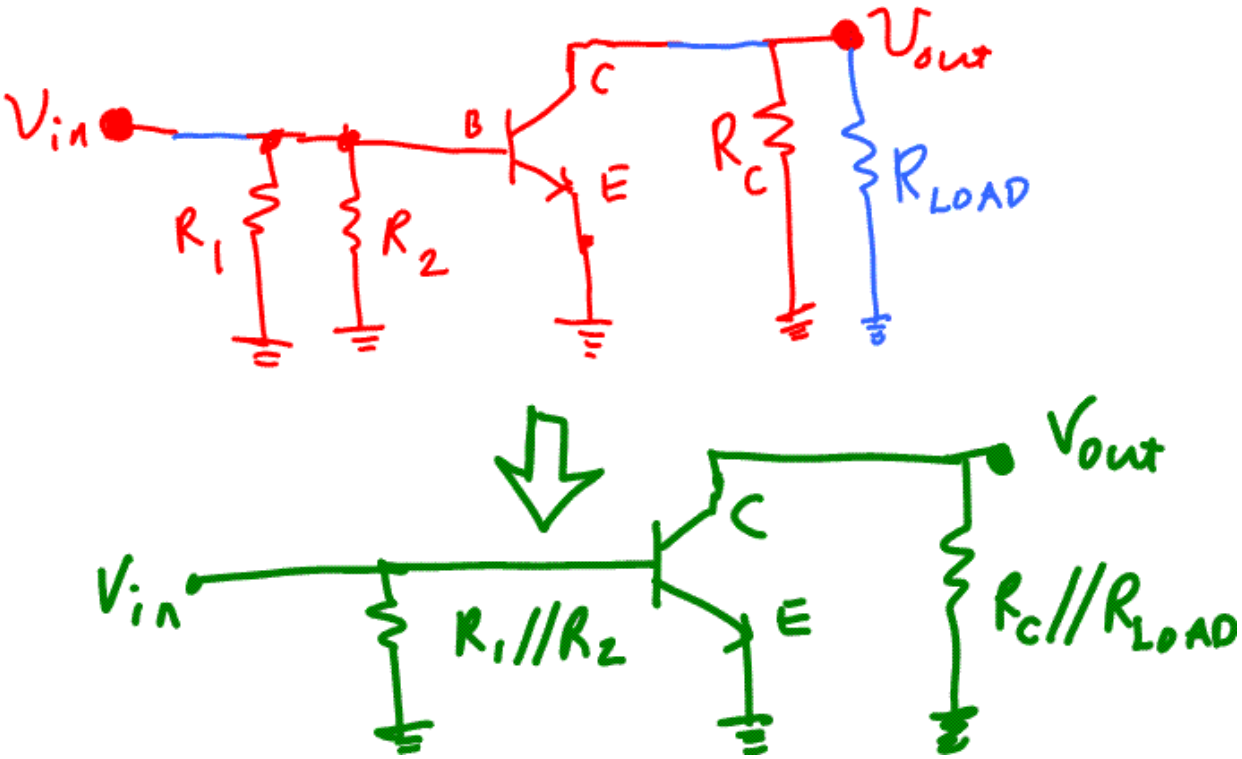
This I_C is very important element in determining the AC voltage gain. Remember this. In AC voltage gain (amplification), the value of IC is an important factor to be included. This we will discuss in the AC Analysis of the circuit.

AC Analysis

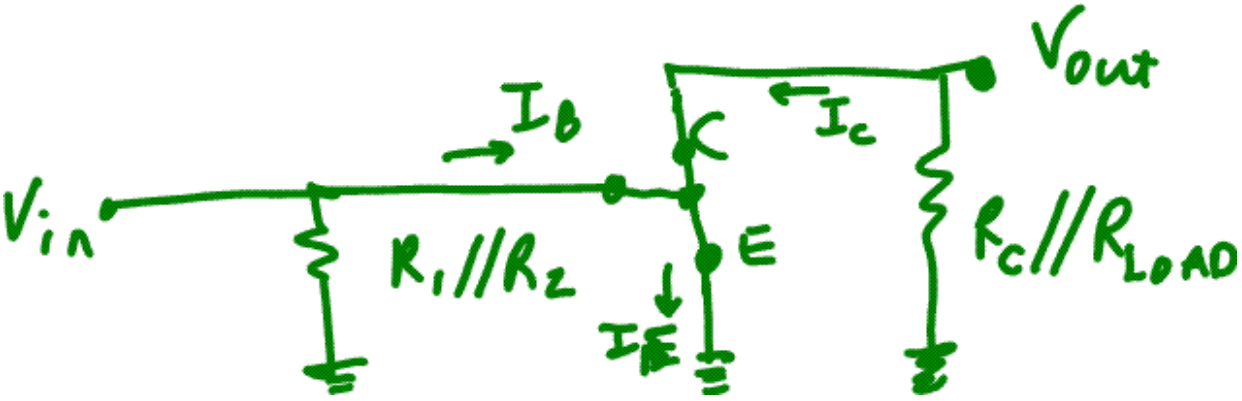
In AC analysis, we assume there is no DC sources. All DC sources are deactivated. That means the DC source V_{CC} will be grounded. Moreover, the capacitors are shorted. Why? The impedance of capacitor is reverse proportional to the capacitance and the frequency of AC signal. If we assume that the AC signal we provide is high frequency signal, then, we can safely say the impedance of capacitor is almost zero. And zero impedance means short circuit. The AC analysis circuit then looks like this:



Since all three CE Amp resistors (R1, R2, and RC) are all connected to the GND, we can redraw the circuit as follows:

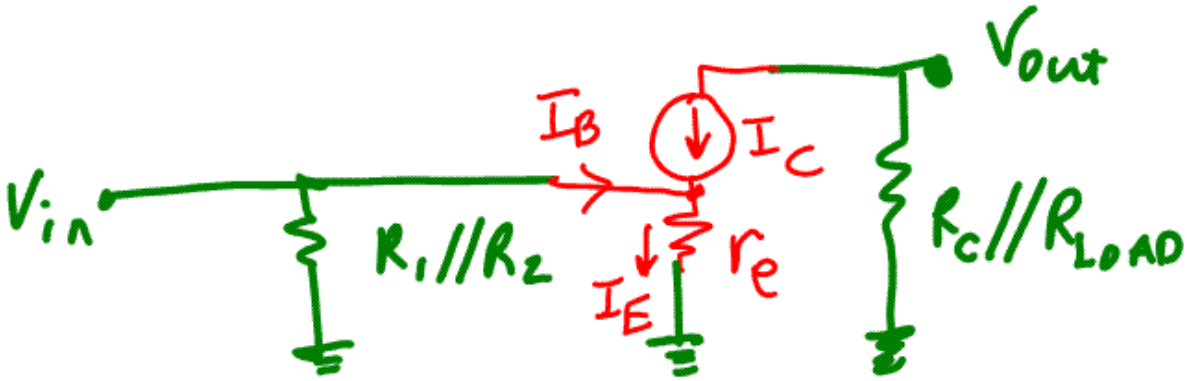


As we know the voltage gain is the ratio output voltage V_{out} and the input voltage V_{in}. How do we get the ratio? If we blindly apply that the Emitter current is close to Collector current, at the same time Base current is zero, then, we would end up at the following "equivalent" circuit:



As you see the above approach has problem: the input voltage is tied to the ground. If you disconnect input circuit from Base (since Base current is zero), then there is no way to connect input and output.

Rescue: Have you heard about Ebers-Moll model of BJT? In the model, the small-signal impedance looking into the Emitter is found by the equation: $r_e = \frac{V_T}{I_c[mA]}$, where V_T=25.3[mV] at room temperature. (Here we learn that BJT performance is dependent upon temperature.) Now we can apply this Emitter resistance re (with simpler form of $25/I_C$[mA]) into the circuit. Then our final good equivalent circuit looks like:



$$V_{out} = -I_C [R_C // R_{LOAD}]$$

$$V_{in} = r_e I_E \doteq r_e I_C$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-I_C [R_C // R_{LOAD}]}{r_e I_C} = -\frac{R_C // R_{LOAD}}{r_e}$$

Whew! After a long road to the final circuit, we have the following conclusion:

(1) The popular CE Amp circuit's voltage gain is dependent upon
- (a) R_C
- (b) Load resistor , and
- (c) the Emitter resistance.

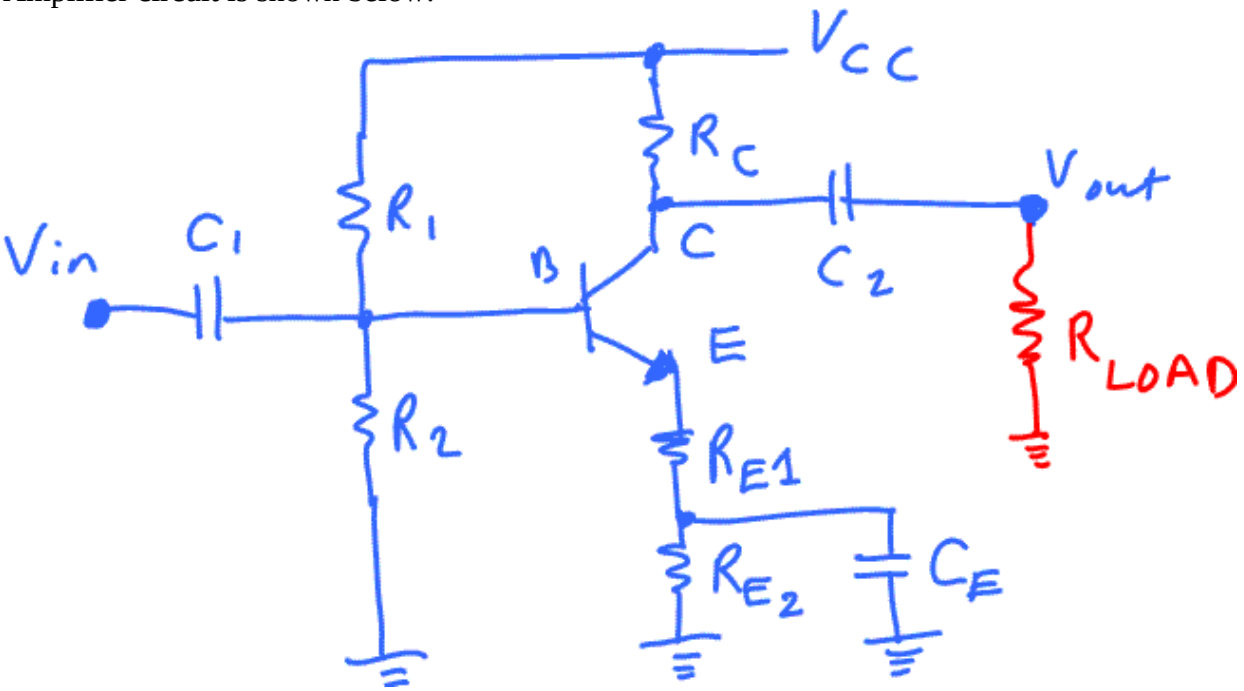
(2) Since Emitter resistance is dependent on temperature, the voltage gain of the circuit can be unstable.

(3) Since the load resistor is also in the equation, load affects the voltage gain of the circuit. Remember this when you design your Common Emitter Amplifier.

Here I intentionally summarize the way we design for a common emitter amplifier because the above amplifier is not the best one I suggest. Design steps and consideration are discussed in the next Common Emitter Amplifier, so-called, swamped Common Emitter Amplifier. Here the idea is to add some bypassed emitter resistance for stable biasing with no change in gain at signal frequencies.

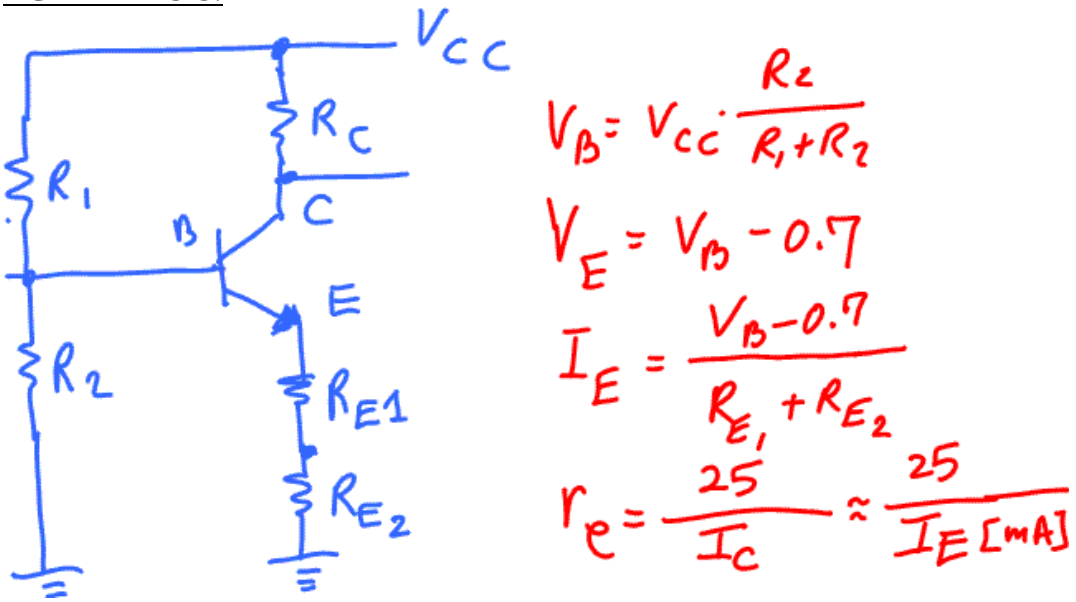
Swamped Common Emitter Amplifier

The only change here in the most popular Common Emitter Amplifier is that we increase the AC resistance of the Emitter circuit to reduce variations in voltage gain. The Common Emitter Amplifier circuit is shown below:

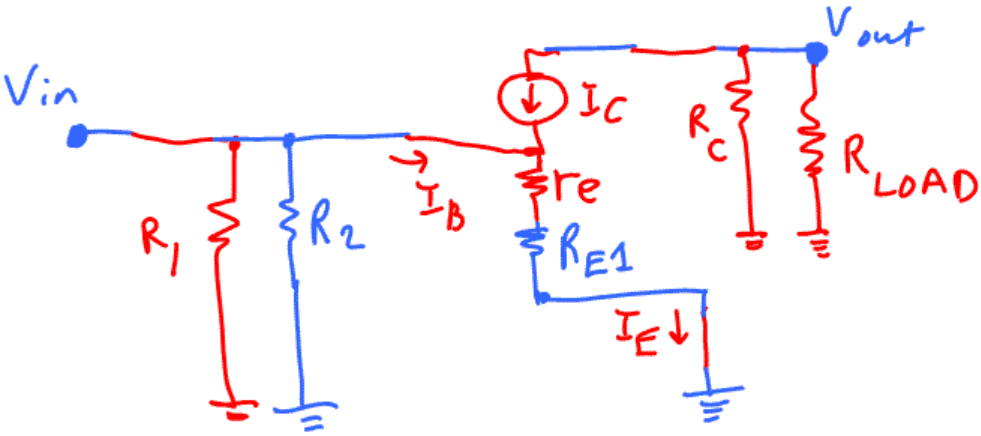


As you see above, part of the Emitter resistance is bypassed by the capacitor C_E.

DC ANALYSIS:



AC ANALYSIS:



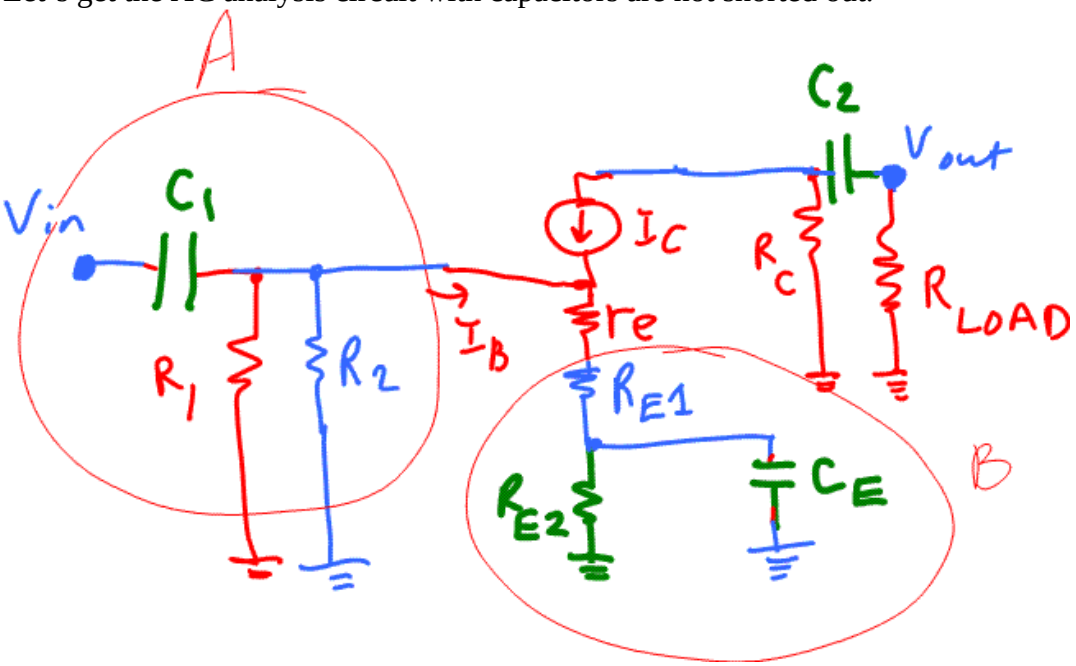
$$V_{out} = -I_C \cdot [R_C // R_{LOAD}] \qquad V_{in} = I_E [R_{E1} + r_e]$$

$$\rightarrow A_v = \frac{V_{out}}{V_{in}} = -\frac{R_C // R_{LOAD}}{r_e + R_{E1}}$$

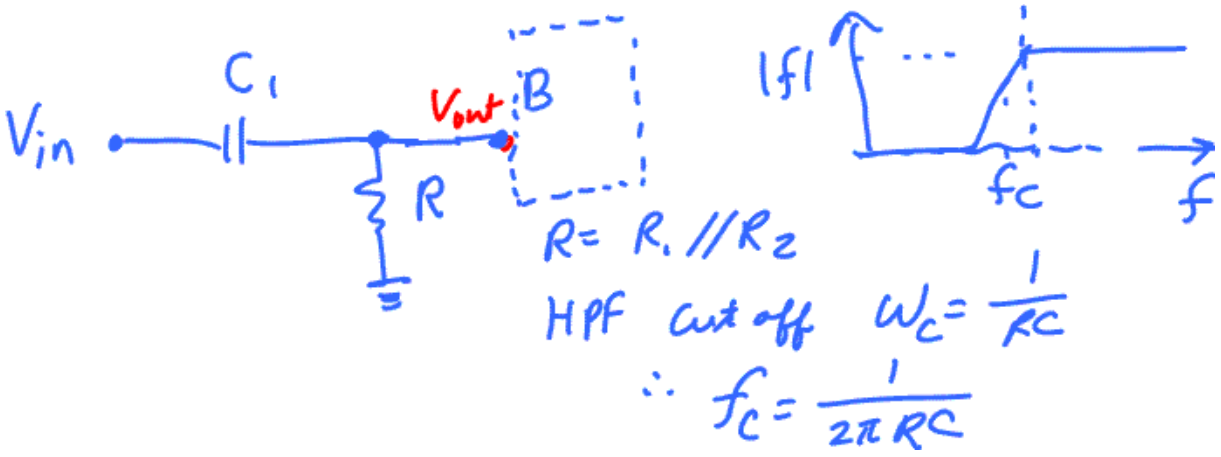
$$(I_C \approx I_E)$$

FREQUENCY ANALYSIS:

Well, we've run far and, thankfully, this is the last subject of the discussion. Before we said, in AC analysis, we short out capacitors when the AC signal frequency is high. This means that when AC signal frequency is low, the capacitor cannot be removed from the consideration. Then how "high" is high enough? This will answer the bandwidth of our Common Emitter Amplifier. Let's get the AC analysis circuit with capacitors are not shorted out.

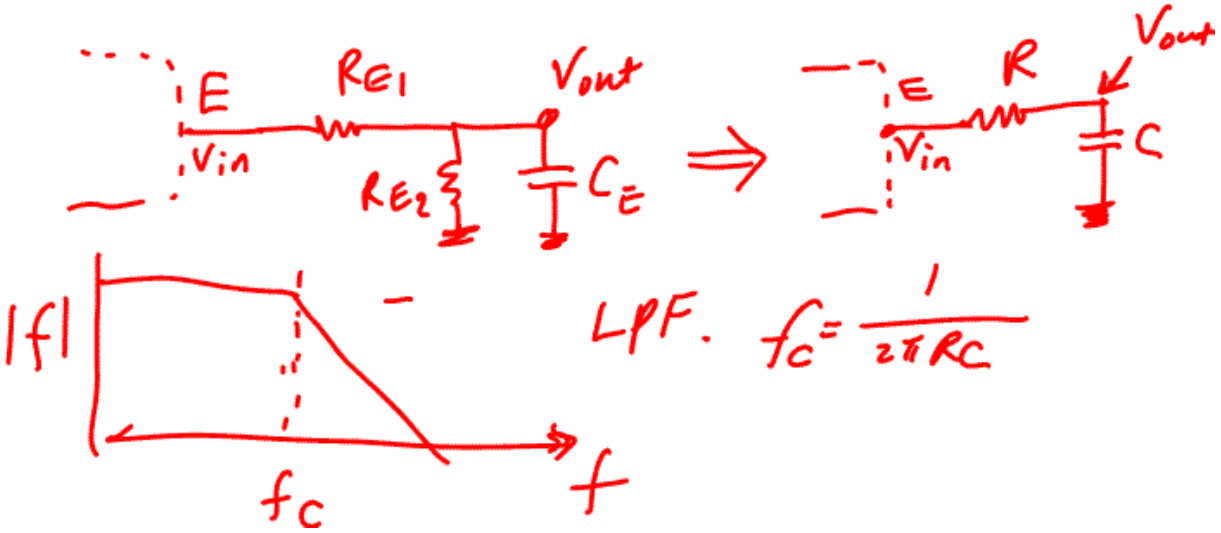


Let's look at the left circled circuit part, A. If we reduce the circuit A then, we can see the circuit from V_{in} to the Base of the BJT (which is the input coupling circuit) forms a simple typical passive high pass filter circuit. It's cutoff frequency is determined by the capacitor and resistor.



From here we can guess (and use it in the design) what the lowest frequency it can pass without any reduction in the promised gain.

On the other hand, the circuit part at the bottom for bypassing, B, we can see this part is a simple typical passive low pass filter, with its cutoff frequency controlled by, again, capacitor and resistor.

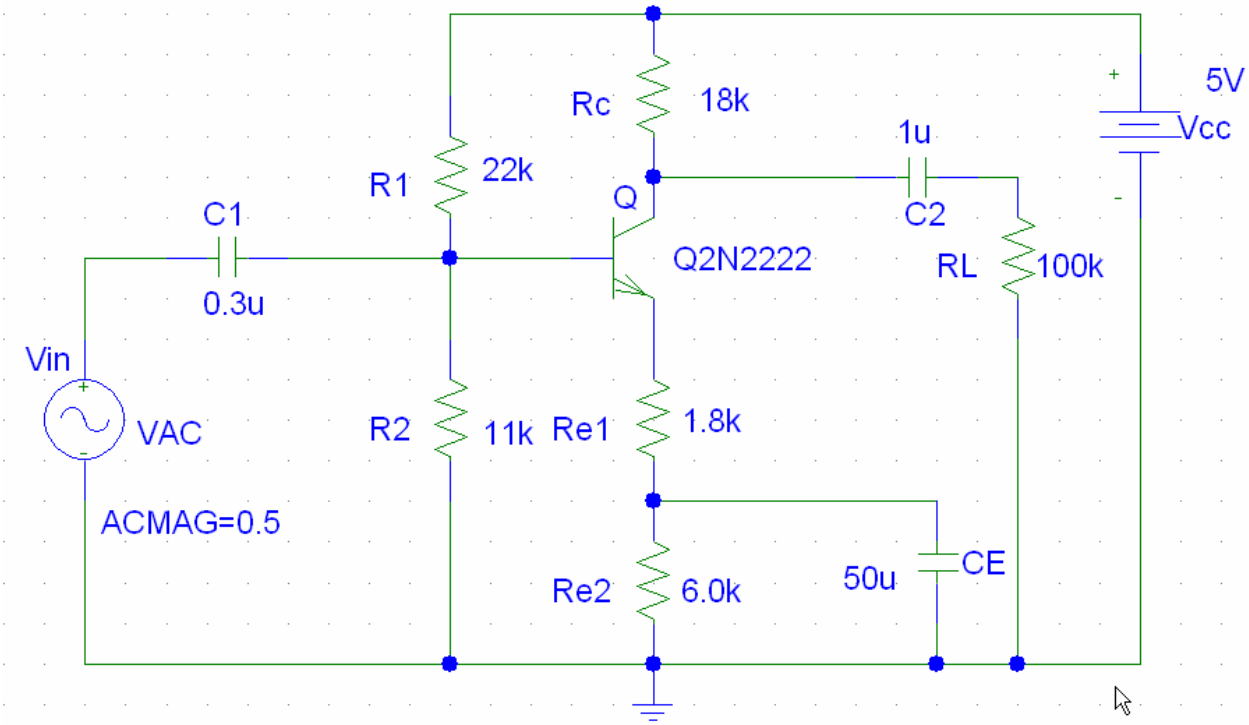


What about the output side capacitor? That part is again another high pass filter circuit. If you change the load, that means you change the frequency response of the circuit.

B.2 Simulation

Since we spent enough time in Theory on Common Emitter Amplifier, we are now eager to design a circuit. But wait for a second. Let's do some simulation first. The circuit presented here may somewhat disappoint you mainly because this circuit does not satisfy the assignment, homework, or project of your class. Since I cannot satisfy everybody, and I do not intend to do so by the way, take the circuit presented here as a starter, but very important starter.

Circuit Formation in PSPice



Note that:

(a) Input signal is VAC (instead of usual VSIN) in the circuit since we need frequency response of the output voltage. AC Sweep is done only with VAC with only amplitude specified. Different frequency will be applied by the simulator.

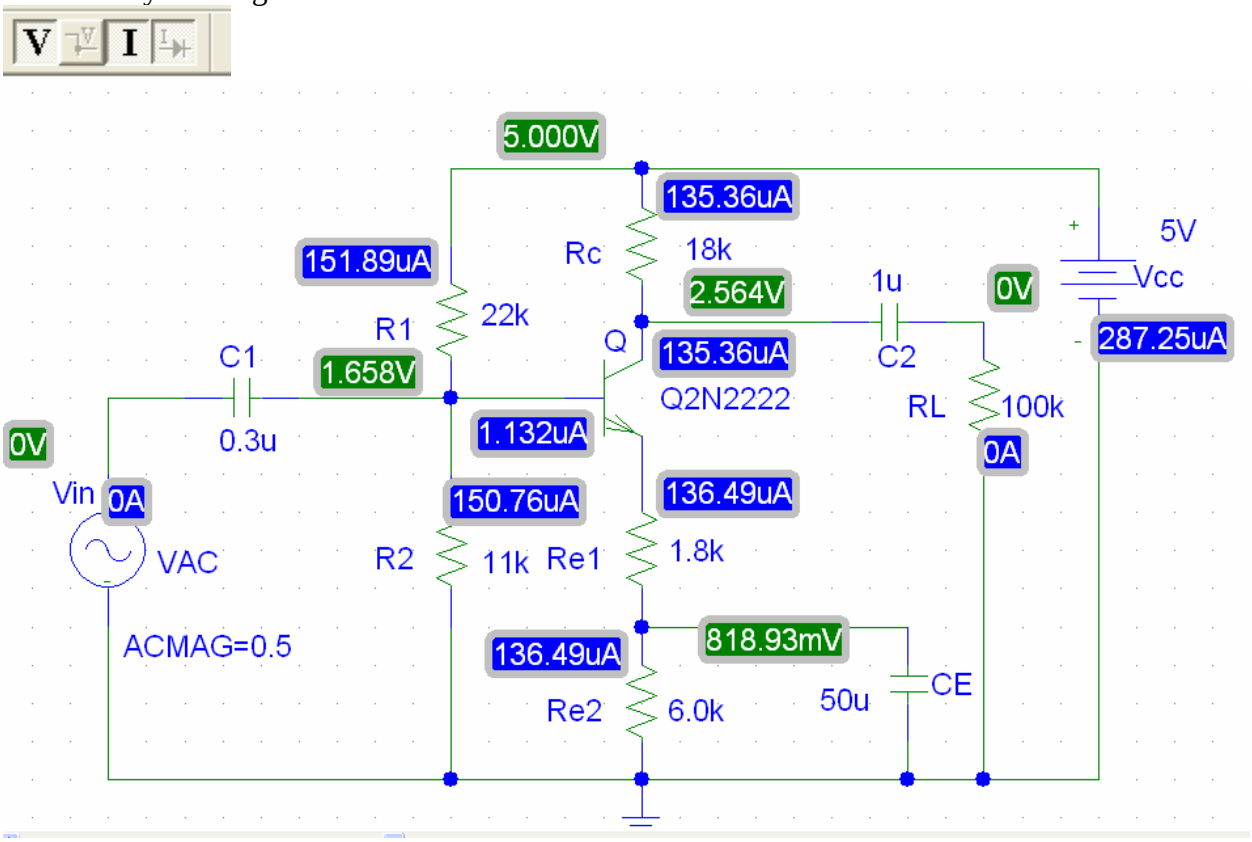
(b) To ease the limitation of power supply by IOBoard, V_{CC} is supplied by 5V source.

(c) The load resistance in the circuit is chosen 100kΩ. This value may be significantly different from your assigned work. You, I mean, you need to do some work too. Right?

(d) Why those values of resistors? Try to answer by DC analysis. Find expected voltage gain from the DC analysis.

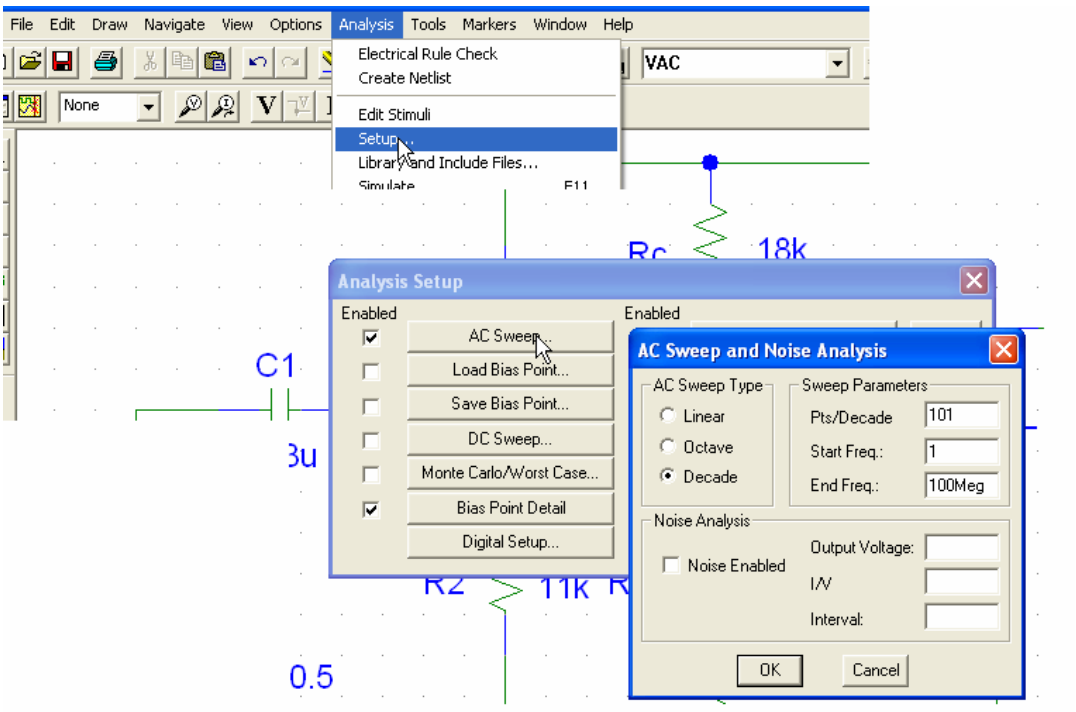
(e) Why those values of capacitors? Perform AC analysis and find expected low and high cutoff frequencies.

Getting Voltage and Current (all DC of course) gives you the pseudo-DC analysis of the circuit. From here you can get a lot of information.

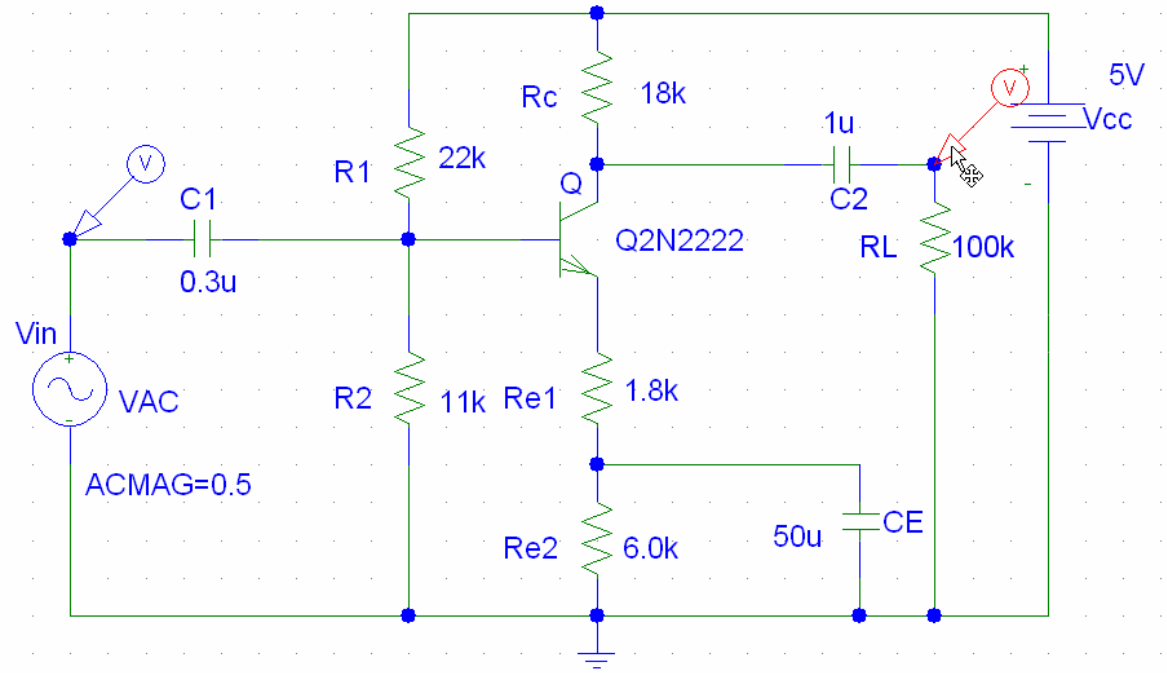


AC Sweep

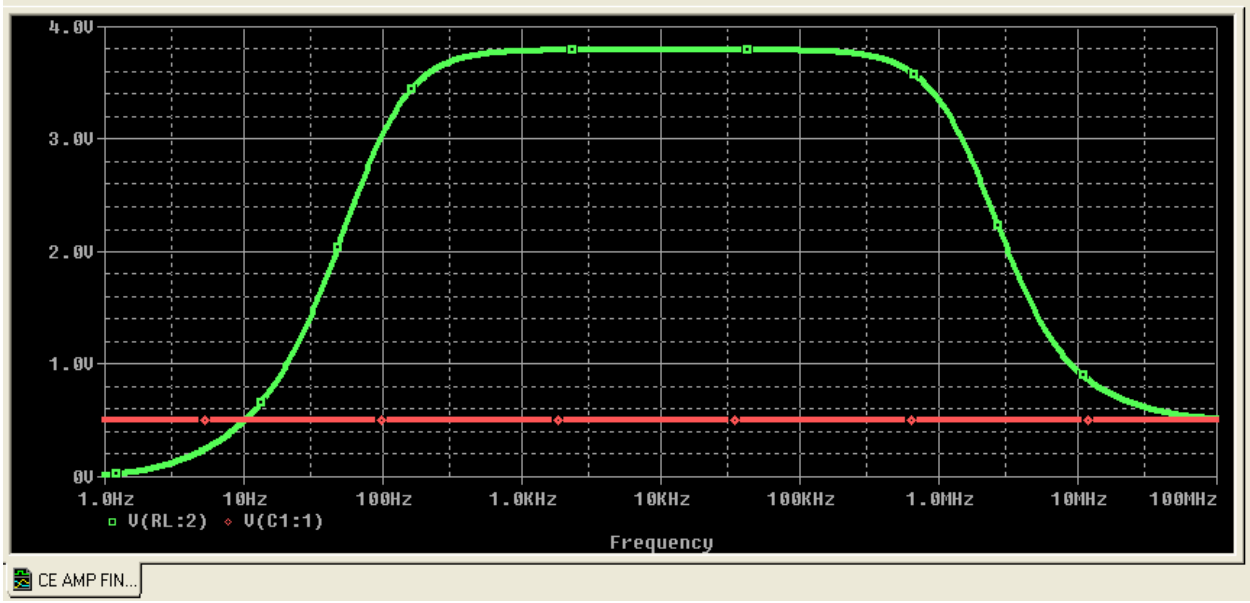
To do AC Sweep, your AC source must be VAC. You decide only ACMAG (AC magnitude), and I picked 0.5 in the circuit above. In the AC Sweep we have to assign our frequency band of interest. Here I set from 0 to 100MHz.



Then we place two voltage probes for frequency analysis:



Simulated Results (Frequency Response)



The green tracing is the voltage at the load and red, the input voltage, at each of the frequency at the range of 0 - 100MHz. What is the low cutoff frequency? What is the high cutoff frequency? What is the mid-band voltage gain?
How can you change the cutoff frequencies by changing capacitor values?
How do you change the gain by changing resistor values?
Do you see the influence of load, so called "load effect"?