EECE 499/693: Computers and Safety Critical Systems

3 How Computer Systems Fail

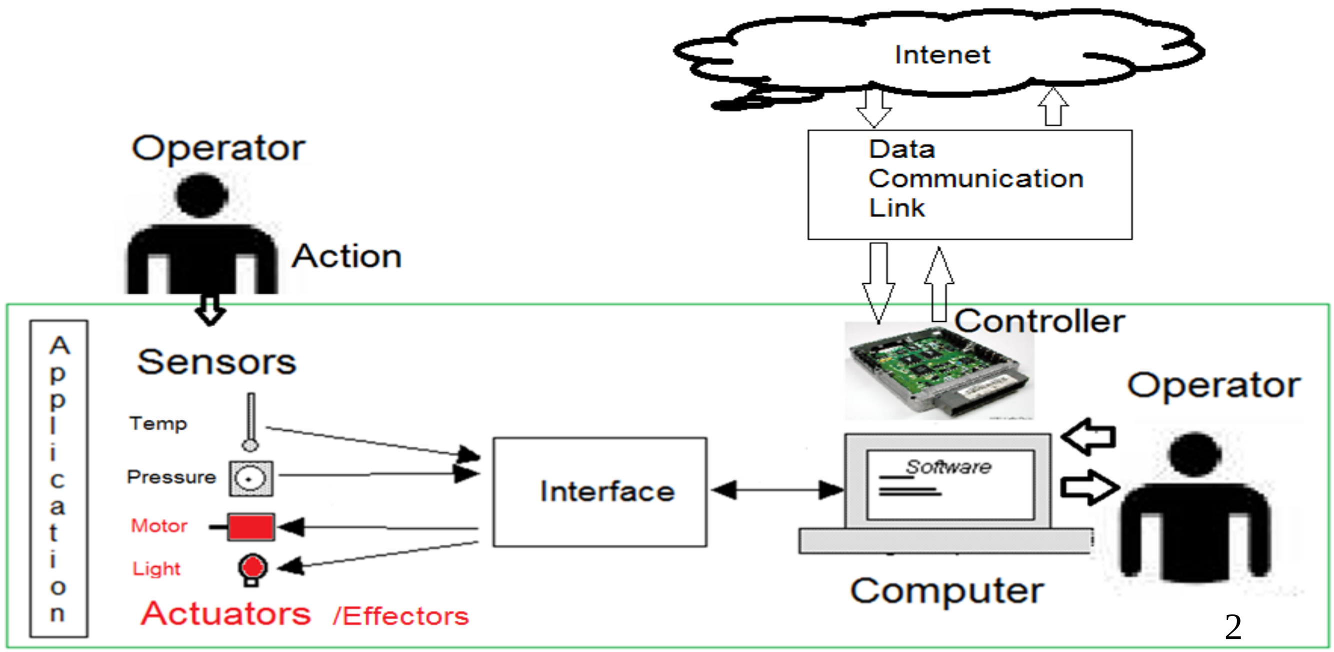
Instructor: Dr. Charles Kim

Electrical and Computer Engineering
Howard University

www.mwftr.com/CS2.html

Background

- Basic computer system (without safety features) with H/W, S/W, and Operator actions
- Need to understand how computer systems fails in order for design modification to deal with potential failures which may cause mishaps.
- Main subject: **Computer Failure Causes**



Computer System Failures – Failure Causes

- Recall "Failure" – failing to perform a duty or expected action.
- Computer System Failure Causes
  - ("Random") Hardware faults
    - Inherent defects in manufactured hardware items
  - Software faults
    - Inherent defects residing in the software programming as errors, anomalies, and discrepancies.
  - Systematic faults
    - Personnel error
    - Environmental conditions
    - Design Faults
      - Design inadequacies
      - Procedural deficiencies

Component Failure Modes and Effects

- Dealing with system failures on a component-by-component basis as opposed to dealing with the effects of specific failure causes
- Why?
  - Computer in a system can “see” the real-time actions of its components
  - Computer in a system cannot “see” readily the causes
- Our approach in the chapter:
  - Discussion of computer systems on a component-by-component basis
  - Each component is examined in terms of its potential failure mode (“the way a component fails”)
  - Looking at a various ways that component failure modes can be determined

Component Failure Mode and Effect Analysis – Sneak Preview

- NSTX Failure Modes & Effects Analysis / NSTX-FMEA-61-4 / 8/17/00 /

WBS Element: 3.2 Cooling Water System
Component: Pumps & Automatic Valves

Function: The Low Pressure Pump provides cooling water flow, the High Pressure Pump (and redundant back-up unit) boosts the pressure for the OH coil. The Automatic Supply and Return Valves control the overall supply of cooling water to the NTC.

Failure Mode	Effect	Detection	Recovery
Low Pressure Pump failure	Loss of coolant flow to NTC	Flow switch measurements, de-energize PAUX relay to power supply system permissives	Shutdown and repair or replace
High Pressure Pump failure	Loss of OH pressure, reduction of OH coolant flow	Flow switch measurements, de-energize PAUX relay to power supply system permissives	Switch to back-up unit
Automatic Supply Valve failure to open	Delivery of coolant to NTC precluded, PLC logic prevents starting of pumps	PLC logic	Troubleshoot and repair or shutdown and replace
Automatic Supply Valve failure to close	Loss of ability to isolate NTC water circuits from pump room, PLC logic prevents closing of Automatic Return Valve	PLC logic	Close manually, troubleshoot and repair or shutdown and replace
Automatic Return Valve failure to open	Delivery of coolant to NTC precluded, PLC logic prevents opening of Automatic Supply Valve	PLC logic	Troubleshoot and repair or shutdown and replace
Automatic Return Valve failure to close	Loss of ability to isolate NTC water circuits from pump room	PLC logic	Close manually, troubleshoot and repair or shutdown and replace

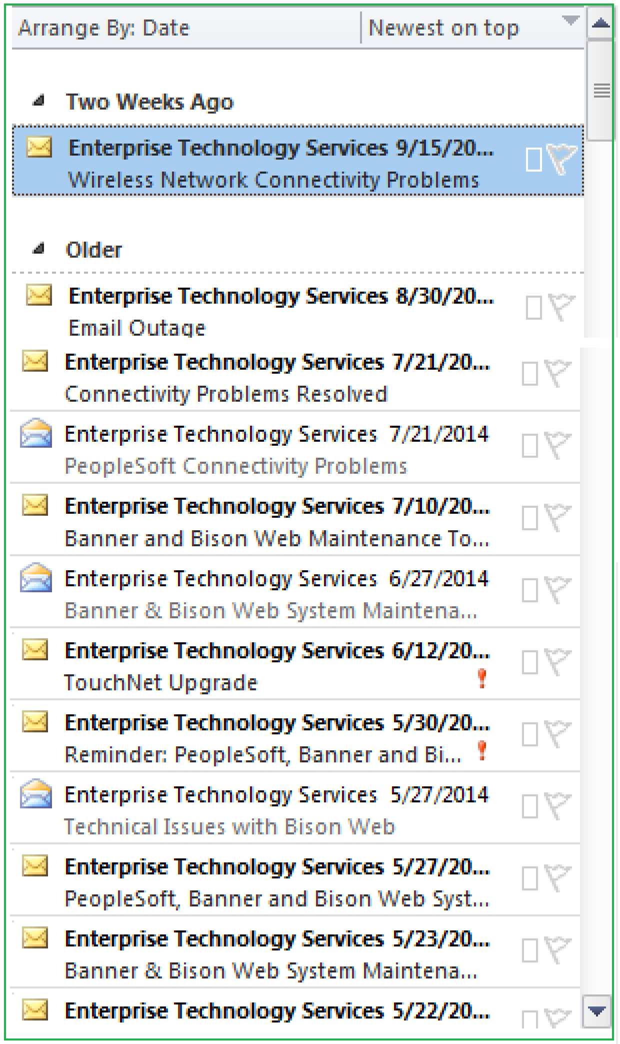
Component Failure Mode Determination

- Sources and means of determining component failure modes- Vendor Data, Facility Records, Published Databases, Technical Literatures, Analysis, Hypothetical Worst-Case Failure Modes

- 1 Vendor Data
  - Based on actual field history
  - Not usually available to the system designer – companies are reluctant to share and publicize.

- 2 Facility Records
  - Maintenance and operating records on past use and failures
  - Incomplete and partial failure modes only

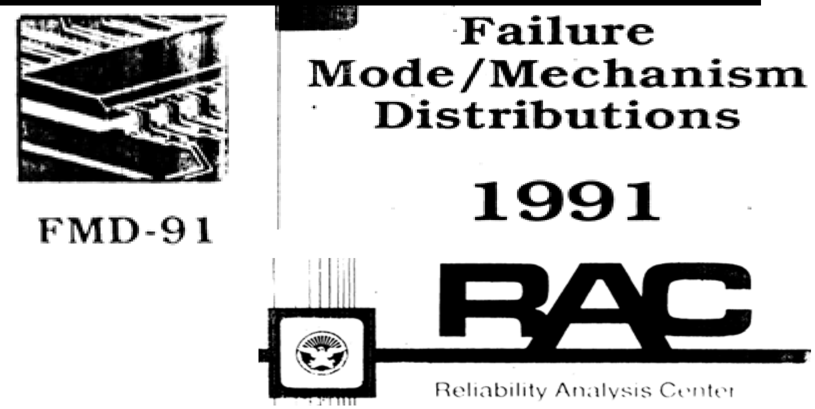
Examples of facility record

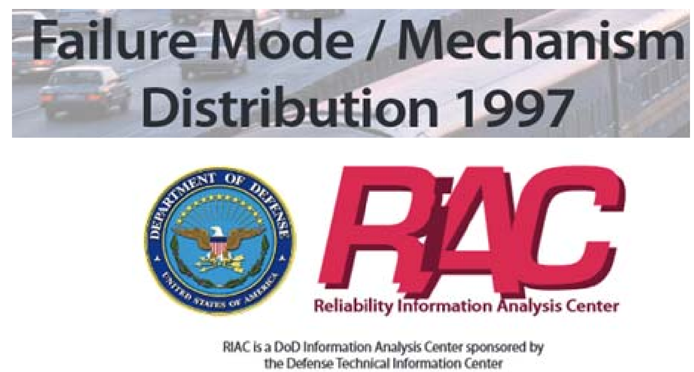


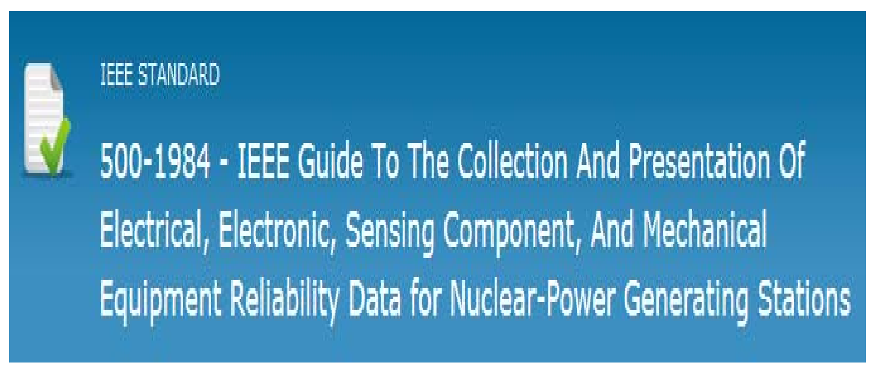
Staff Name and Date	Problem and description (including any error messages)	Time taken to fix problem	Attempted solution and suggestions for next step	Person who fixed it	Contact information
Ian / 31/7/03	Mouse stopped working. No error messages	30 mins	Checked mouse device settings in control panel / system. No properties found. Turned off PC and Swapped over mouse. Mouse started working again.	Jo	Central Services IT co-ordinator

Component Failure Mode Determination – conti.

- 3 Published Databases
  - Cover failure modes for many hardware components in computer systems
  - FMD-91 Failure Mode/Mechanism Distributions, Reliability Analysis Center, Rome, NY (1991)
  - IEEE Std-500-1984 IEEE Guide to the Collection and Presentation of Electrical, Electronic, Sensing Component, and Mechanical Equipment Reliability Data for Nuclear-Power Generating Stations (1984) --- Currently Withdrawn







FMD-91 at a glance

13. ABSTRACT (Maximum 200 words)

The intent of this document is to present failure mode distributions to be used in support of reliability analysis such as FMEAs and FMECAs when used in conjunction with accepted reliability prediction techniques such as MIL-HDBK-217 along with RACs Nonelectronic Parts Reliability Data (NPRD). The intent of these distributions is that they form a basis for a standard set of distributions to be used in the reliability engineering industry. The scope of this publication covers all electronic, mechanical and electromechanical parts or assemblies on which RAC has collected failure data.

Failure mode, effects and criticality analysis (FMECA) is an extension of failure mode and effects analysis (FMEA).

Part failure rate (λ_p) - The part failure rate (λ_p) from the appropriate reliability prediction or failure rate data source such as MIL-HDBK-217 or NPRD-91 shall be listed.

Failure Effect Probability (β). The β values are the conditional probability that the failure effect will result in the identified criticality classification, given that the failure mode occurs.

Device Type	Failure Mode	Failure Mode Probability (α)
Alarm	False Indication	.48
	Failure to Operate on Demand	.29
	Spurious Operation	.18
	Degraded Alarm	.05
Antenna	No Transmission	.54
	Signal Leakage	.21
	Spurious Transmission	.25

Military Handbook (MIL-HDBK-217)

MILITARY HANDBOOK

RELIABILITY PREDICTION OF
ELECTRONIC EQUIPMENT

NOT MEASUREMENT SENSITIVE

MIL-HDBK-217F

2 DECEMBER 1991

SUPERSEDING
MIL-HDBK-217E, Notice 1
2 January 1990

RADC-TR-90-72
Final Technical Report
May 1990

- Reliability Prediction of Electronic Equipment
- Failure Rate Prediction Models for
  - Microcircuits (Sec. 5)
  - Discrete Semiconductors (Sec 6) – Diode, transistors, etc
  - Resistors (Sec. 9)
  - Capacitors (Sec. 10)
  - Inductive Devices (Sec. 11)
  - Rotating Devices – Motors (Sec. 12)
  - Relays (Sec. 13)
  - Switches (Sec. 14)
  - Connectors (Sec. 15)
  - And more !!!

Part Failure Rate Models --- Preview

We'll be back soon.

MIL-HDBK-217F

$$\lambda_p = (C_1\pi_T + C_2\pi_E)\pi_Q\pi_L \quad \text{Failures}/10^6 \text{ Hours}$$

$$\lambda_p = (C_1\pi_T + C_2\pi_E + \lambda_{cyc})\pi_Q\pi_L \quad \text{Failures}/10^6 \text{ Hours}$$

$$\lambda_p = \lambda_{BD}\pi_{MFG}\pi_T\pi_{CD} + \lambda_{BP}\pi_E\pi_Q\pi_{PT} + \lambda_{EOS} \quad \text{Failures}/10^6 \text{ Hours}$$

- λ_p : Failure Rate
  - C_1 : Die Complexity Failure Rate
  - C_2 : Package Failure Rate
  - π_T : Temperature Factor
  - π_E : Environmental Factor
  - π_Q : Quality Factor
  - π_L : Learning Factor (Years in Production)

Microprocessor

Die Complexity Failure Rate - C_1

No. Bits	Bipolar C_1	MOS C_1
Up to 8	.060	.14
Up to 16	.12	.28
Up to 32	.24	.56

Package Type	π_{PT} Hermetic	π_{PT} Nonhermetic
DIP	1.0	1.3
Pin Grid Array	2.2	2.9
Chip Carrier	4.7	6.1

Failure Rate Determination Example – Sneak Preview

We'll be back soon.

MIL-HDBK-217F

- Example 1: CMOS Digital Gate Array
- Device: CMOS Digital Timing Chip (4046) for airborne inhabited cargo application
  - 1000 transistors
  - Case Temp 48 C and 75mW power dissipation
  - Normal manufacturing
  - Electrical testing, seal testing, and external visual inspection
  - B-level burn-in followed by electrical testing
  - Complied to MIL-STD-883 screening method
  - 24-pin DIP with a glass seal
  - Has been manufactured for several years
- Solution
  - Section 5.1
  - C1 = 0.020

$$\lambda_p = (C_1\pi_T + C_2\pi_E)\pi_Q\pi_L \quad \text{Failures}/10^6 \text{ Hours}$$

P 5-3

MOS Digital and Linear Gate/Logic Array

Digital		Linear
No. Gates	C_1	No. Transistors
1 to 100	.010	1 to 100
101 to 1,000	.020	101 to 300
1,001 to 3,000	.040	301 to 1,000
3,001 to 10,000	.080	1,001 to 10,000
10,001 to 30,000	.16	
30,001 to 60,000	.29	

Q1:

I'm having trouble counting the number of transistor in the gate designs that I have made.

NAND, NOR, NOT: transistors = 2 * # of inputs

AND, OR, transistors = 2 * # of inputs + 2

www.ece.gatech.edu/academic/courses/ece2030/faq/gates/main.html

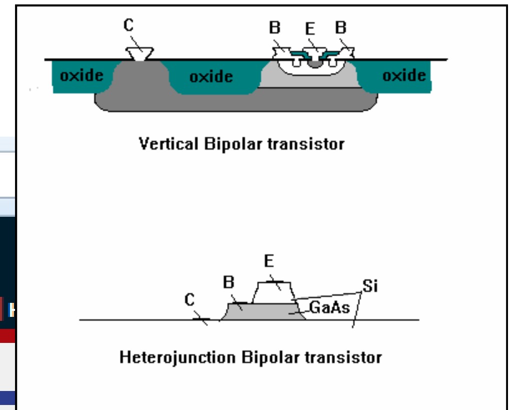
Failure Rate Determination – Background Knowledge Required

MIL-HDBK-217F

- Semiconductor background

SECTION IV - GLOSSARY

Listed below are: (1) a compilatio
apparatus and compositions usef
included in the glossary below, a
assigned definitions which may be
related art.



www.uspto.gov/web/patents/classification/uspc438/defs438.htm

United States Patent and Trademark Office

Home | Site Index | Search | FAQ | Glossary | Guides | Contacts | eBusiness | eBiz alerts | News | H

Patents > Guidance, Tools, and Manuals >> Classification >>> Class Definition

Class Numbers & Titles | Class Numbers Only | USPC Index | International | HELP

CLASS 438, SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

Click here for a printable version of this file

SECTION I - CLASS DEFINITION

A. This class provides for manufacturing a semiconductor containing a solid-state device by a combina

NPRD-91

NONELECTRONIC PARTS RELIABILITY DATA 1991

Reliability Analysis Center

A DoD Information Analysis Center

13. ABSTRACT (Maximum 200 words)

This document provides failure rate data for a wide variety of component types including mechanical, electomechanical, and discrete electronic parts and assemblies. It also provides summary failures rates for numerous part categories by quality level and environment.

Data represents a compilation of field experience in military, commercial, and industrial applications, and concentrates on items not covered by MIL-HDBK-217, "Reliability Prediction of Electronic Equipment." Data tables include part descriptions, quality levels, application environments, point estimates of failure rate, data sources, number of failures, total operating hours, and detailed part characteristics.

Part Description	Qual Lev	App Env	Data Source		Fail Per E6 Hours	Total Failed	Operating Hours (E6)	Detail Page
Accelerometer					49.2154			
	Com	AI			89.0991			
			NPRD-082		534.1592	86	0.1610	3-1
			NPRD-096		14.8620	7	0.4710	3-1
	Mil				42.5082			
		AI			168.5923			
			16953-000		111.1108	65	0.5850	3-1
			25199-000		280.5080	2094	7.4650	3-1
			NPRD-106		153.7490	367	2.3870	3-1
		DOR	13253-000		0.4342	143	329.3300	3-1
		GM			49.2490			
			25199-000		277.8615	182	0.6550	3-1
			NPRD-067		12.1951	2	0.1640	3-1
			NPRD-084		35.6761	301	8.4370	3-1
			NPRD-095	<	27.0270	0	0.0370	3-1
		SF	10219-034	<	8.9286	0	0.1120	3-1
	Unk				46.6686			
		A	14182-001		236.6061	-	--------	3-1
		G	14182-001		52.5229	-	--------	3-1
		SF	14182-001		8.1790	-	--------	3-1

IEEE std 500-1984: example

- ANSI/IEEE Std 500-1984 P&V
  - IEEE Standard Reliability Data for Pumps and Drivers, Valve Actuators, and Valves

IEEE STANDARD

500-1984 - IEEE Guide To The Collection And Presentation Of Electrical, Electronic, Sensing Component, And Mechanical Equipment Reliability Data for Nuclear-Power Generating Stations

(Composite of 11.2.a, 11.2.b and 11.2.X)

CHAPTER: 11 Driven Equipment **SECTION:** 11.2 Valves **SUBSECTION:**

ITEM OR EQUIPMENT DESCRIPTION

FAILURE MODE	FAILURE RATE								(*) OUT OF SERVICE (†) REPAIR TIME OR (§) RESTORE (HOURS)			
	FAILURES/10^6 HOURS				FAILURES/10^6 CYCLES							
	LOW	REC	HIGH	REF	LOW	REC	HIGH	REF	LOW	REC	HIGH	REF
ALL MODES	0.03	1.39	3.23E3			732			0 * 0.40 †	117.0 0.98	8.14E3 476	

ANSI/IEEE Std 500-1984 P&V

(REC) recommended values

Published Data – on Webpage

Lecture 4: Computer Systems

Assignment #3: Read Chapter 1 The Origins of Accidents of Scott Sagan's book, ***The Limitation of Safety*** (Pri
the subject with one's own critic view. The first paragraph should comprehensively summarize the entire report.
presentation file by Oct 20 via email. Selected good works will be invited to present in the class of Oct 21.

Lecture 5: How Computer Systems Fail

MIL-HDBK-217F IEEE Std 500-1984 P&V FMD-91 NPRD-91 ATmega Datasheet

USPTO Class 438 - Semiconductor Device Manufacturing: Process

- All in PDF format
- **Print the Section 5 of MIL-HDBK-217F and bring to the class.**

Component Failure Mode Determination – conti.

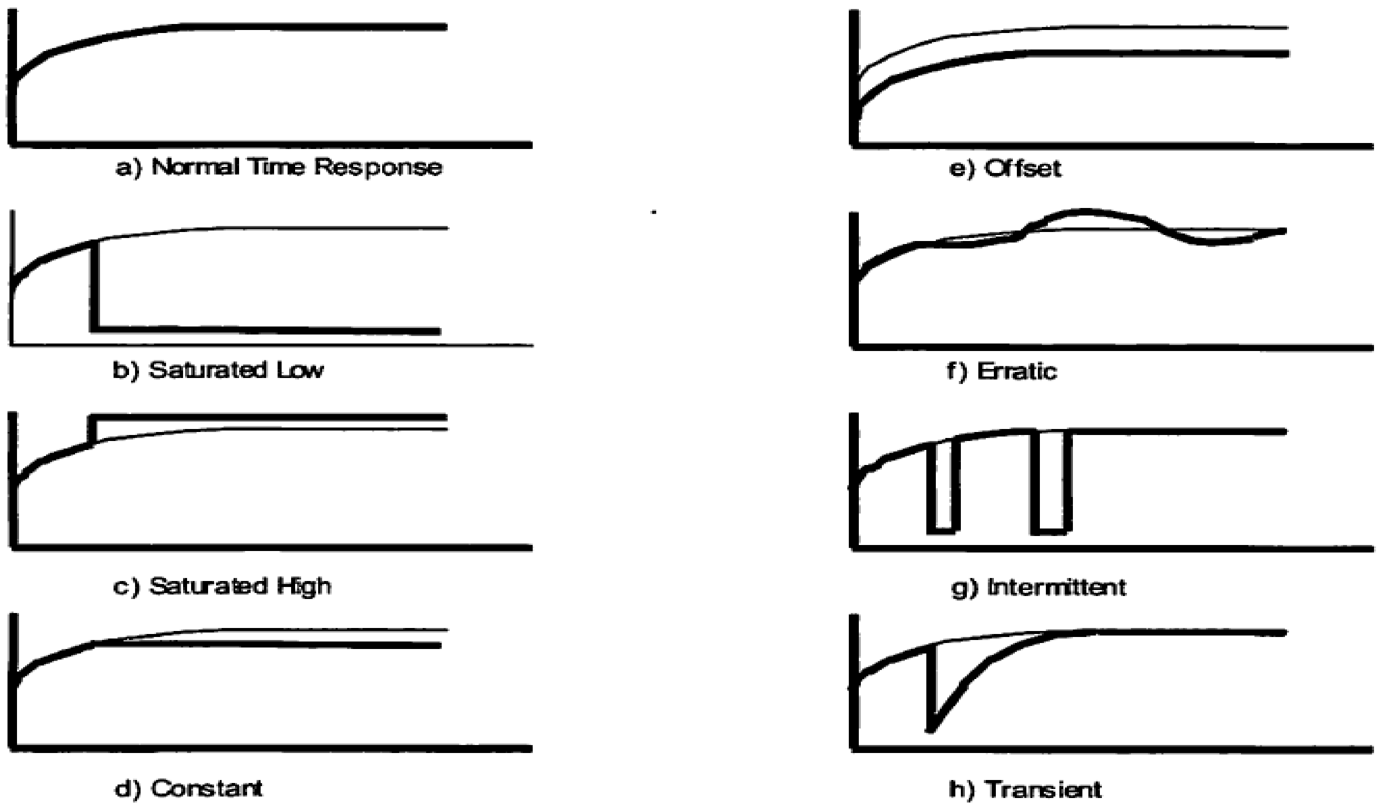
- 4 Technical Literatures
  - Conference and journal articles on software engineering and software reliability
  - How faults are introduced into software – programmer mistakes and oversights
- 5 Analysis
  - Engineering analysis for failure modes of some parts whose failure mode data are not available on its constituent parts
- 6 Hypothetical Worst-Case Failure Modes
  - Why ?
    - Failure modes obtained from different sources and Analysis are not enough – cover only a fraction of possible failure modes
  - How to solve this deficiency?
    - Consider a worst case scenario in failure modes
      - Environmental conditions
      - Maintenance/repair failures and mishandling etc
  - **This will be covered later in detail**

Component Failure Modes

- First
  - Sensor Failure Modes
  - Actuator Failure Modes
  - Power and Interconnect Failure Modes
  - Operator Failures
- Next
  - Computer Failure Modes

Sensor Failure Modes

- Sensor
  - Converts a physical stimulus into a corresponding electrical signal
  - Sensor failure: the output is an incorrect signal for a given stimulus
- Sensor Hardware Failure Modes
  - Explained in terms of **time responses**



Sensor Failure Modes

- Sensor Hardware Failure Modes - **Explanation**

Sensor Signal Type	Failure Mode	Explanation
Analog or Digital	Minimum output	Sensor output maintains lowest possible signal level.
	Maximum output	Sensor output maintains highest possible signal level.
	Constant output	Sensor output does not change when input changes
	Offset	Actual sensor output is offset by a constant amount from correct value
	Erratic	Actual sensor output varies erratically about true sensor response.
Discrete Level	Intermittent	Switches intermittently between high and low level.
	Spurious switch	Switches with no input.
	Switch at wrong level	Switches when input stimulus is at an incorrect value.
	Fail to switch	Fails to switch with input change.
Discrete Switch	Short circuit	Switch contact appears closed.
	Open circuit	Switch contacts appears open.
	Intermittent open/short	Switch contact alternates intermittently between open and closed position.
	Switch at wrong level	Switches when input stimulus is at an incorrect value.
	Fail to switch	Fails to switch with input change.

Sensor Failure Modes - Example

- Sensor Hardware Failure Modes
  - **Transducer and Transmitter**

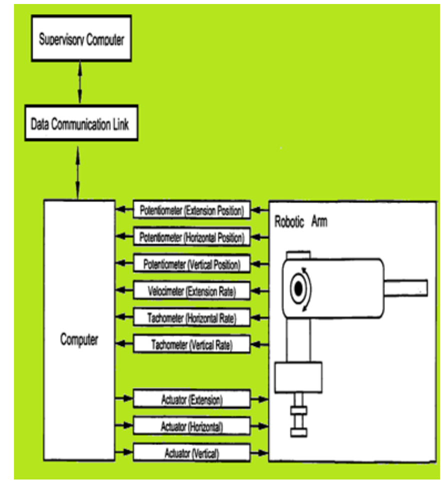
Sensor Hardware Failure Modes

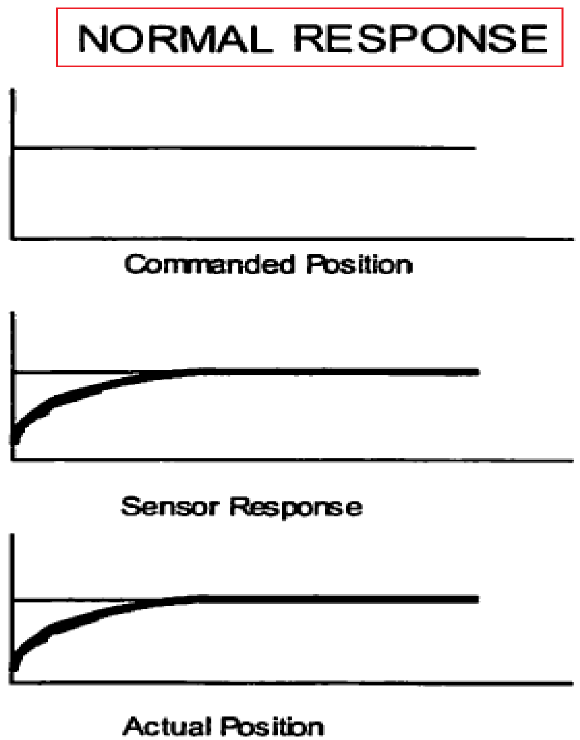
Sensor	Failure Modes
Current (AC) meter	Shorted. Open circuit. Degraded operation. (1)
Level transducer	Minimum output. Maximum output. Constant. Erratic. (2)
Photodetector	Open. Shorted. Degraded operation. (1)
Position gyroscope	Drift. Out of specification. Opened. Shorted. Binding/sticking. Spurious/false operation. Unstable operation. (1)
Thermocouple	Constant output. (2)

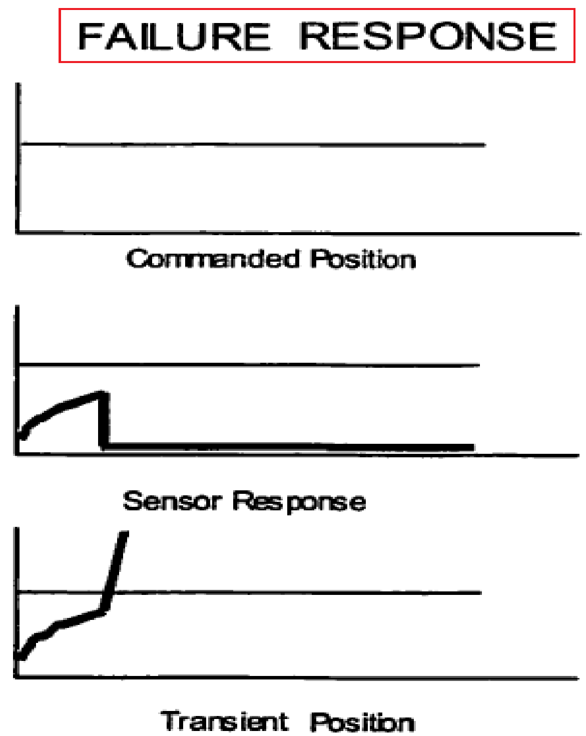
Sources: (1) FMD-91. (Op. cit.) (2) IEEE Std 500-1984. (Op. cit.)

Sensor Failure Effects

- No direct impact of sensor failure to sensor itself
- Dangerous if the sensor (failure) output is connected with operator actions
- Directly connected to mishaps when sensor outputs are processed by the computer to generate signals for effectors.







Side Bar

Computer Control System Design

Class Activities

in 5 Steps

- Lessons/Suggestion
  - Start with clear understanding of your system. Don’t do on others. Use your own system with your own scopes, functions, and methods
  - All inputs and outputs, corresponding components (sensors & actuators) are to be included in the system design, requirement, hardware connection, etc.
  - Understand and know the way your system operates (i.e., output generation with all conditions of inputs) under normal condition – this becomes the basis of your flowchart
  - Flowchart is to connect input conditions to outputs to make your system work. Use a diamond shape for conditions and decisions to make (IF….ELSE…)

Side Bar

Assignment #3

Reminder

- Assignment #3
- Check the webpage

Lecture 4: Computer Systems

Assignment #3: Read Chapter 1 The Origins of Accidents of Scott Sagan's book, ***The Limitation of Safety*** (Princeton University Press, 1993), and discuss the subject with one's own critic view. The first paragraph should comprehensively summarize the entire report. Submit (1) a paper report by Oct 16 and (2) a presentation file by Oct 20 via email. Selected good works will be invited to present in the class of Oct 21.

Lecture 5: How Computer Systems Fail

Sensor Failure Effects - Example

Effector/Actuator Failure Modes and Effects

- Effector/Actuator
  - Conversion of electrical signal into a physical stimulus
  - **Failure:** incorrect physical stimulus for a given electrical signal
- Effector/Actuator Hardware Failure Mode Data
  - Same source for sensor hardware failure modes
  - RAC and IEEE data sources
  - Actuator physical outputs: min, max, constant, offset, erratic values, intermittent, and transient failures
- Effects of Actuator Hardware Failure
  - Possibly, considerable mechanical and electric power output can be generated, which may **lead to property damage and personnel injury** during system operation, system non-operating maintenance and inspection periods.
  - Usually a **direct cause of mishaps**

Effector/Actuator Failure Modes (partial list)

Effector Failure Modes

Type of Effector	Failure Modes
Blower	Bearing failure. Mechanical failure. Electrical failure. Blade *erosion. Out of balance. Motor failure.* (1)
Electric motor	Binding/sticking. Fails to start. Fails to run after start. (1)
Electric power switch	Opened. Mechanical failure. Shorted. High contact resistance. (1)
Pump	Leaking. No operation. Seal/gasket failure. Intermittent. (1)
Relay - power	Fail to close. Fail to open. Shorted. (1)
Relay - protective	Spurious operation. Fails to open. Fails to close. (2)
Valve - hydraulic	Leaking. Stuck closed. Stuck open. Intermittent operation. Improper flow. (1)
Valve - pneumatic	Broken. Leaking. Opened. Closed. Spurious opening. Spurious closing. (1) Spurious opening. Spurious closing. Failure to open on demand. Failure to close on demand. Premature or delayed actuation (Actuation that occurs out *of timing sequence). Partially opening. Partially closing.* (2)
Valve - solenoid	Spurious opening. Spurious closing. Failure to open on demand. Failure to close on demand. Premature or delayed actuation (Actuation that occurs out of timing sequence). Partially opening. Partially closing. (2)

Sources: (1) FMD-91. (Op. cit.) (2) IEEE Std 500-1984. (Op. cit.)

Actuator Failure - Example

HU Professor's Invention May Save Lives

BY ANDREW MOTEN
Contributing Writer

Almost two years ago, Charles Kim, Ph.D., professor of engineering, nearly lost his life because of an electrical fault.

Kim says a fault caused his car to stall in early 2005, as he drove in a high traffic area of I-395.

"My car stopped three different times—once while on the Interstate. And the mechanics couldn't find a problem," he said. "Later on, I found out it was a problem with the electrical wire in my car."

Each year, electrical faults, also known as arcing, cause approximately 40,000 house fires in the United States and an unknown number of automobile problems, according to a 2004 report by the Consumer Product Safety Commission. The house fires cause more than $680 million in property damages.

Through the necessity to find the electrical fault, Kim developed a device that could potentially detect faulty electrical wiring before disasters have the chance to occur. This budding breakthrough in technology works on the same principal as a DSL phone/internet line.

"I started on this project around the summer of 2005," Kim said, who has been a professor of computer and electrical engineering at Howard for almost eight years. "I've been working with electric faults and

Derril Smith - Senior Photo Editor

Engineering Professor Charles Kim, awaits patent approval for a device that would detect faulty electric wires.

the two began last year, Kim said.

"If patented, it is my hope that the technology is used to benefit the likes of commercial airline companies, U.S. Military aircraft and ships, as well as everyday civilians," Kim said.

Until Kim's patent is completed, the method for detecting faulty electrical wires is physical observation, a method that leaves room for human error. In some instances, that margin has proved dangerous and oftentimes fatal.

In July 1996, 230 people died when TWA Flight 800 exploded in the airspace just outside of Long Island, N.Y. and crashed into the Atlantic Ocean. In 2003, a series of manhole explosions occurred

THE HI
The Daily Student Voice of How
VOLUME 90, NO. 70
TUESDAY, JANUARY 23, 2007

- The Hilltop Tuesday, January 23, 2007

Distributor Ignition Coil

The rest of the story

TECHNOLOGY

Biz group teams with Howard to commercialize tech

University brains pair up with big business brawn to take technologies from the lab to the marketplace

By Ben Hammer
Staff Reporter

A manufacturing industry group has teamed with Howard University to commercialize technologies that could have applications for local companies involved in defense, biotechnology and other businesses.

The National Center for Manufacturing

Breaks or modifications in power flow are especially costly and dangerous in planes and ships, which contain many miles of tightly wound lines interwoven with other cables. The system could be used in other complex electrical systems such as car engines to locate hard-to-find problem spots that flare up intermittently but not when a mechanic is looking for a fix.

"The problem is you cannot reach, you cannot pinpoint because they are mostly out of reach or under compartments you don't know where they are," Kim says. "So pilots know something is wrong, and they have to ground or abort the mission in mid-air."

NCMS senior program manager David

tions Group of Germantown use to send digital bits of data over electrical lines. Current and similar companies provide Internet service in buildings through plug-in connections and sensors to power companies for monitoring their infrastructure in the field.

Getting Kim's hardware-and-software system into commercial production won't be easy.

Commercializing research technologies developed in government and university labs is notoriously difficult because researchers and businesses don't speak the same language, and private industry sees commercialization efforts as risky.

"It's just been really hard," says April Young, Comerica senior vice president of venture banking. "There have not been a lot of successes because the culture is very different. A company is usually 1 percent idea and 99 percent execution, and that's just a challenge."

Young, a former director of the Virginia Department of Economic Development and executive director of the Fairfax County Economic Development Authority, has been involved for years in efforts to strengthen the area's capabilities to transfer technologies from research labs into businesses.

E-MAIL: BHAMMER@BIZJOURNALS.COM PHONE: 703/258-0831

US008102779B2

(12) **United States Patent**
Kim

(10) **Patent No.:** **US 8,102,779 B2**
(45) **Date of Patent:** **Jan. 24, 2012**

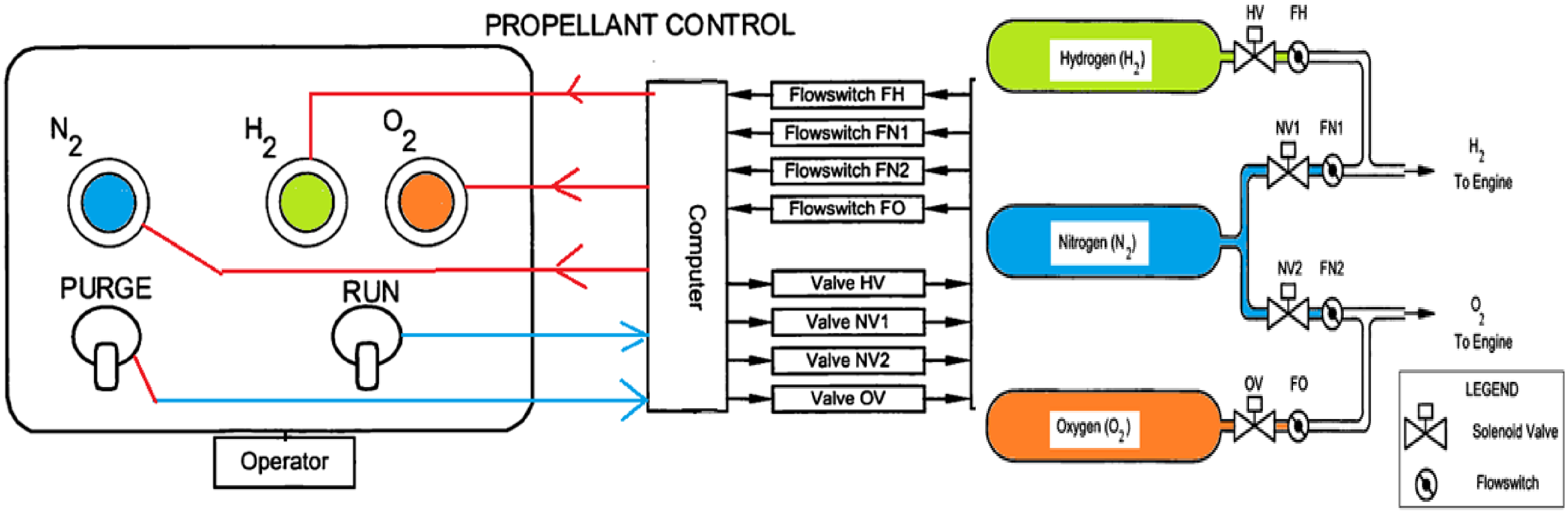
(54) **SYSTEM AND METHOD OF DETECTING AND LOCATING INTERMITTENT ELECTRICAL FAULTS IN ELECTRICAL SYSTEMS**

(75) Inventor: **Charles J. Kim**, Annandale, VA (US)

(73) Assignee: **Howard University**, Washington, DC (US)

6,198,401	B1	3/2001	Newton et al.	
6,313,642	B1	11/2001	Brooks	
6,385,561	B1	5/2002	Soraghan	
6,477,475	B1 *	11/2002	Takaoka et al.	702/59
6,646,447	B2	11/2003	Cern	
6,725,176	B1	4/2004	Long et al.	
6,759,851	B2	7/2004	Hazelton	
6,842,011	B1	1/2005	Page	
6,856,936	B1	2/2005	Chen	
6,868,357	B2	3/2005	Furse	
6,927,579	B2	8/2005	Blades	

Effector/Actuator Failure - Example



- **Scenario 1**: The system in in standby and all valves are initially closed. Then HV undergoes a spurious opening. → Hydrogen mixes with air and the mixture ignites explosively.
- **Scenario 2**: The engine is presently running with HV and OV open. In the PURGE command, the HV fails to close. → Hydrogen flows into the test chamber resulting in explosion.

Power and Interconnect Failure Modes and Effects

- Electrical power is required for all computer systems
  - Utility Grid Source (for ground-based system)
  - On-site Source (for mobile or transportation system)
  - Conversion to DC or lower AC is usually required to furnish power for electronic components and instruments
- Interconnect Hardware
  - All computer system components are connected from the power source through use of electrical wires, hydraulic or pneumatic lines.
  - Interconnect hardware is also required to connect sensors to computers and computers to actuators (effectors)
- Interconnect Hardware Failure Modes
  - See next slide
- Interconnect Hardware Failure Effects
  - The one after the Modes slide

Power and Interconnect Failure Modes (partial list)

Power and Interconnect Component Failure Modes

Component	Failure modes
Electronic/instrumentation power supply	Incorrect voltage. No output.
Hydraulic accumulator	Leaking. No operation. Out of specification. Stuck closed.
Hydraulic pump	Leaking. Improper flow. No flow.
Interconnect, electrical	Open. Shorted. Intermittent.
Interconnect, pneumatic	Leak.
Interconnect, hydraulic	Leak.
Public utility power	No output.
Uninterruptable (backup) power supply	Fail to transfer on demand.

Source: (1) FMD-91. (Op. cit.)

Intermittent Electrical Interconnect Faults

- SwissAir 111
- TWA 800
- Fires and possibly explosion by arc and spark

Swissair Flight 111 | September 2, 1998

After a four-and-a-half-year investigation, *which revealed evidence* of an in-flight fire above the cockpit caused by faulty wiring and fueled by flammable airframe insulation, Canada's Transportation Safety Board published its final recommendations.

TWA Flight 800 | July 17, 1996

focused on the flammability of the 747's fuel tank, including its potential ignition sources, design, and certification standards, and on the maintenance and aging of the aircraft's other systems, particularly wiring and fittings that could spark or overheat. Within two years of the crash, new fuel-management procedures were required for all 747s.

Swissair 111

Arcing from wiring of the in-flight entertainment network did not trip the circuit breakers but ignited flammable covering on insulation blankets and quickly spread across other flammable materials. The crew did not recognize that a fire had

TWA 800

FBI closes probe into TWA crash

Agency says criminal act did not cause blast

By Pat Milton
Associated Press

The CIA released a simulation video Tuesday re-enacting the explosion of TWA Flight 800. From left, this is the depiction of the accident. Frame one shows the Paris-bound flight as it explodes off the coast of Long Island. Frame two shows the fiery descent of the jumbo jet. Frame three shows the aircraft disintegrating as it plummets toward the ocean.

Associated Press photo

Intermittent Electrical Interconnect Faults

- USS Parche (683) – Arc Damage

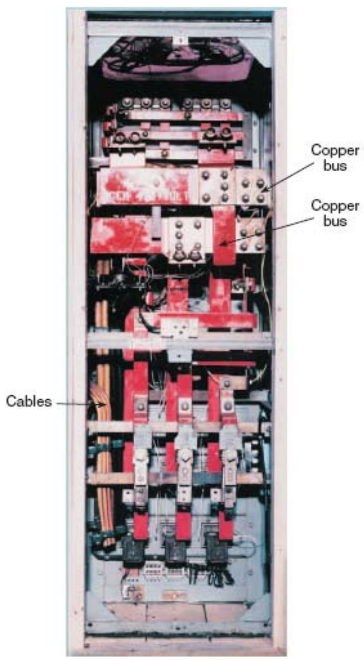


Figure 2. Inside the rear of a typical small switchboard. The red painted bus bars vary from 1 to 2 in. wide.

Figure 1. Arcing damage sustained on USS *Parche* (SSN 683). Note that some of the copper bus, cables, insulators, and switchboard structure are missing.

Evolution of Arc Fault Protection Technology at APL

H. Bruce Land III, Christopher L. Eddins, and John M. Klimek

JOHNS HOPKINS APL TECHNICAL DIGEST, VOLUME 25, NUMBER 2 (2004)

NFF ("No Fault Found")

- **Chronic Problem of Intermittent Faults**: **NFF**
  - Problem reported by crew is not reproduced.
  - Average NFF figure for avionics is approx. 30%.
  - Off-Line Testing Problem with Random, Intermittent Nature of the Electrical Faults

Saturday
Dec 18, 2004 **Aviation Today**

No-fault-found findings are turning up at the extraordinarily high rate of 50 to 60 percent at commercial airlines and military repair depots. Much of this is attributable to the failure of ramp and bench tests to detect age-related problems found in avionics boxes and other aircraft components, not to mention old wiring.

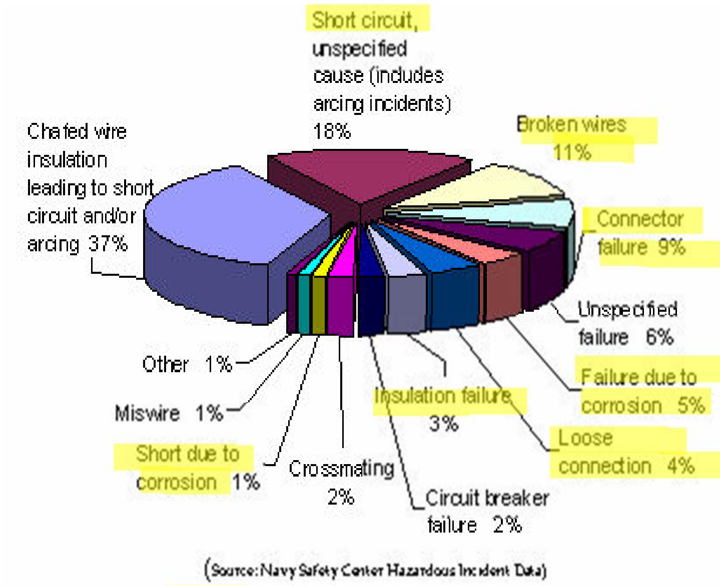


Figure 10. Typical wire system failure modes for aircraft (1980-1999).

- **So, how to detect intermittent faults?**

Invention

(12) **United States Patent**
Kim

(10) **Patent No.:** **US 8,050,002 B2**
(45) **Date of Patent:** **Nov. 1, 2011**

(54) **HOUSING ARRANGEMENT FOR FAULT DETERMINATION APPARATUS AND METHOD FOR INSTALLING THE SAME**

(75) Inventor: **Charles J. Kim**, Annandale, VA (US)

(73) Assignee: **Howard University**, Washington, DC (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 273 days.

6,198,401	B1	3/2001	Newton et al.	
6,313,642	B1	11/2001	Brooks	
6,385,561	B1	5/2002	Soraghan	
6,477,475	B1	11/2002	Takaoka et al.	
6,646,447	B2	11/2003	Cern	
6,725,176	B1 *	4/2004	Long et al.	702/183
6,759,851	B2	7/2004	Hazelton	
6,842,011	B1	1/2005	Page et al.	
6,856,936	B1	2/2005	Chen	
6,868,357	B2	3/2005	Furse	
6,927,579	B2	8/2005	Blades	
6,934,655	B2	8/2005	Jones	
6,965,303	B2	11/2005	Mollenkopf	
6,972,574	B2	12/2005	Allan	
7,319,574	B2	1/2008	Engel	

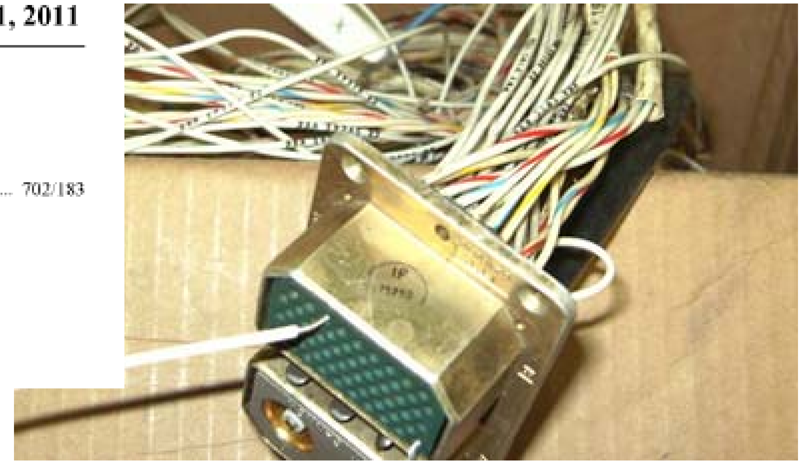


Fig. 2A

Fig. 2B

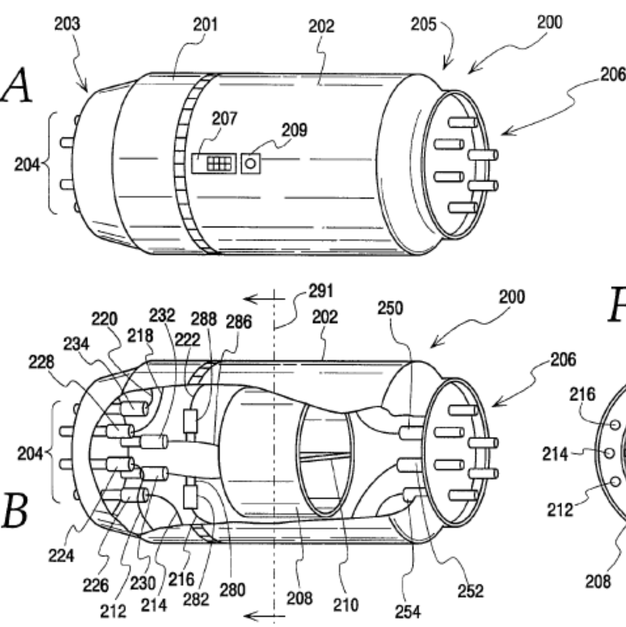
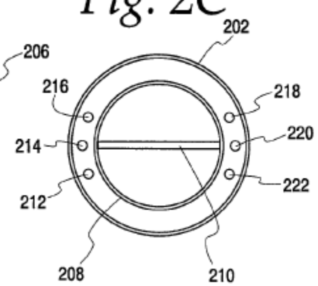
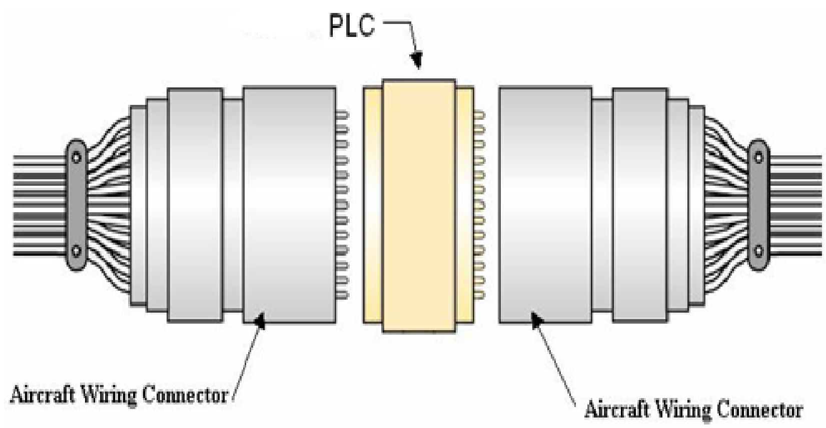


Fig. 2C





Power and Interconnect Failure Modes and Effects

- Interconnect Hardware Failure Effects
  - Generally results in an apparent failure of primary components, or simultaneous dysfunction of computer, sensor, and actuator electronics.
  - Failure in electrical interconnect between sensor and computer make computer “think” a sensor failure.
  - Failure in electrical interconnect between a computer and an actuator make computer “think” a required task is completed, while no actuator action is performed.

Operator Failures

- Operator failure has two forms
  - Operator error
    - Operator mistakes in following correct procedure, triggering a mishap
    - Ways of making errors
      - Omitting of required actions
      - Performing of non-required actions
      - Failing to recognize needed actions
      - Responding poorly (too late, too early, incorrect)
      - Failing to communicate (miss-communication)
  - Procedural inadequacies
    - Design faults in procedures, causing correctly acting operator to fail

Combination of Failures

The Washington Post

Metro Crash: Experts Suspect System Failure, Operator Error in Red Line Accident

By Lyndsey Layton
Washington Post Staff Writer
Tuesday, June 23, 2009

Experts familiar with Metro's operations focused last night on a failure of the signal system and operator error as likely causes of yesterday's fatal Red Line crash.

Metro was designed with a fail-safe computerized signal system that is supposed to prevent trains from colliding. The agency's trains are run by onboard computers that control speed and braking. Another electronic system detects the position of trains to maintain a safe distance between them. If they get too close, the computers automatically apply the brakes, stopping the trains.

These systems were supposed to make yesterday's crash impossible.

In yesterday's crash, it appeared that the operator of the train that crashed did not apply the emergency brakes, also known as the "mushroom." Experts said the train appeared to be traveling fast before impact because the force pushed the first car of the train on top of the train ahead. Witnesses on the train that crashed also reported that the train did not brake before impact.

There was no reason to think that the operator did not spot the train ahead of her yesterday. The weather was clear, and the trains were not in a tunnel.

The Second Part

- Computer Hardware Failure Modes and Effects
- “Tin Whiskers” get attention recently

Computer Hardware Failure Modes and Effects

- Digital Integrated Circuit (IC)- chip
- Physical construction of IC
- Packages
- Pins
  - Signal pins
    - Binary information flow in and out of the chip
  - Support pins
    - Power
    - Ground

Digital IC Failure Mechanisms and Modes

- **Concern**: generation of incorrect output bit pattern on its signals pins given a correct input bit pattern

Digital Integrated Circuit Failure Mechanisms and Modes

Digital Component	No. Pins	Failure Mechanisms	Failure Modes
CPU (microprocessor) Integrated circuit	40 to 296	Die attachment failure. Metallization failure. Contaminated. Cracked/ fractured. Oxide defects.	High leakage current. Output stuck low. Shorted.
Memory – MOS integrated circuit	16 to 40	Mechanical failure.	Data bit loss. Short. Open. Slow transfer of data.
Digital integrated circuits (General)	14 to 40	Contaminated. Oxide defects. Wire bond failure. Metallization failure. Die attachment failure. Package/related failure.	Open. Shorted. Output stuck high. Output stuck low. Supply open.

Source: (1) FMD-91. (Op. cit.)

IC Failure Modes

- **Input Data Alteration** between the pins and the chip
  - Open wire (wire-bond failure)
  - Opened wire contacting another wire
  - Can undergo permanent, intermittent, and transient failures
- **Chip Output Data Alteration** between chip and the pins
  - Open wire (wire-bond failure)
  - Opened wire contacting another wire
  - Can undergo permanent, intermittent, and transient failures
- **Chip Failure** in performing I/O functions
  - Transistors embedded on silicon material
    - Silicon bulk defects
  - Micro-thin aluminum conductors of the circuits
    - Aluminum defect, oxide defects
  - Can undergo permanent, intermittent, and transient failures
  - No way of knowing the location, extent, and specific effects of the failure mechanisms/modes
  - No practical way to translate failure mode/mechanism data into a specific functional failure modes

Electronic Interface Component Failure Modes and Effects

- Commonly employed electronic components

Table 3.6 Computer Interface Components Failure Modes/Mechanisms and Effects

Computer Interface Component	Failure Modes/Mechanisms	Failure Effects
Capacitors (decoupling)	Short. Change in value. Open.	Loss of electronics function (short). Reduction in transient protection (Open.)
Connector/connection	Open. Poor contact/intermittent. Short.	Loss of electronics function or data alteration.
Clock	Stops. Frequency change.	Loss of CPU function (clock stoppage or rate increase). Frame period increase (clock rate decrease.)
DC power supply	Incorrect voltage. No output.	Loss of electronics function.
Electrical filter (EMI)	Shorted, capacitor failure.	Reduction or loss in transient protection.
Printed wiring assembly	Open. Short.	Loss of electronics function or data alteration.

Source: (1) FMD-91. (Op. cit.)

CPU Functional Failure Modes

- Worst-Case Scenario Analysis
- Bigger threat is the propagation of the CPU failures to the outside – Safety concern

Table 3.7 CPU Functional Failure Modes

Failed CPU Component(s) (Figure 2.18)	Failure Effect (Local)
ALU	Arithmetic or logical operation yields incorrect result.
Instruction decoder & pointer	Generates incorrect address causing memory to return incorrect contents.
Accumulator & register(s)	Potential alteration of correct data or address.
Input port	Alters correct input data.
Output port	Alters correct output data.
Memory data interface	Alters data written to memory or data and instructions read from memory.
Memory address interface	Alters correct address before memory addressing.

ADC/DAC Functional Failure Modes and Effects

Table 3.9 Effector Output Module Functional Failure Modes and Effects

Effector Output Module	Failure Mode	Failure Effects
D/A converter (multichannel) (Figure 2.12)	Conversion failure	Incorrect output data including minimum, maximum, constant, offset, or erratic values
	Select failure	Incorrect analog channel selected
Digital/discrete converter (Figure 2.12)	Conversion failure	Incorrect output bit(s)
	Select failure	Incorrect discrete channel selected
Digital/digital converter (Figure 2.12)	Conversion failure	Incorrect digital output

Operator Input Device Failure Modes

Table 3.10 Operator Input Device Failure Modes/Mechanisms

Operator Input Device	Failure Modes/Mechanisms
Keyboard assembly	Mechanical failure. Spring failure. Contact failure. Wiring and connection failure. Locked up. Indicator/display failure. Integrated circuit failure. Cable failure.
Potentiometer	Opened. Intermittent. Drift. Spurious/false operation. High contact resistance. Shorted. Mechanical failure.
Switch (summary)	Opened. Mechanical failure. Shorted. High contact resistance.
Switch (toggle)	Mechanical failure. Opened. Contact failure. Shorted. Spring failure. Intermittent operation. Binding/sticking.
Trackball	Lamp failure. Connector failure. Integrated circuit failure. Diode failure.

Source: (1) FMD-91. (Op. cit.)

Operator Output Device Failure Modes

Table 3.11 Operator Output Device Failure Modes/Mechanisms

Operator Output Device	Failure Modes/Mechanisms
Alarm	False Indication. Failure to operate on demand. Spurious operation. Degraded alarm.
CRT (Cathode ray tube) video display	Power supply failure. Loss of control. Performance degradation. Open filament.
Lamp /light	No illumination. Loss of illumination.
Light emitting diode (LED)	Open. Short.
Klaxon (annunciator module)	Degraded operation. Spurious/false operation. Fails to operate on demand.
Meter	Faulty indication. Open. No indication.
Liquid crystal display	Dim rows. Blank display. Flickering rows. Missing elements.

Communication Module Failures

- Communication Components
  - Optical transceivers
  - Wireless transceivers
  - Routers
  - Modem
  - Radio
- Failure Modes
  - Failing to transmit and/or receive data
  - Transmitting incorrect data
  - Distorting received data

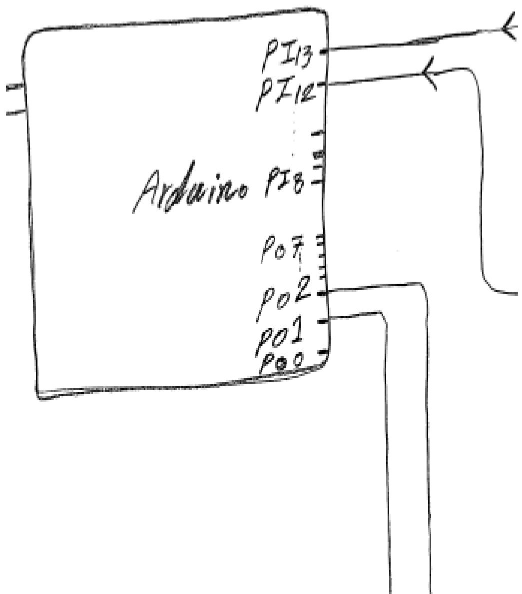
Software Faults and Failures

- Observation
  - Software components, “codes” or “instructions”, do not break or wear out.
  - Many reports of “Software failure” – “Computer program (“collection of instructions”) failure”
- Definition of “Software Failure”
  - “Software does not produce a correct response given a set of inputs and internal states”
  - Software failures are caused by
    - **Software Fault**
    - **Software Requirement Fault**

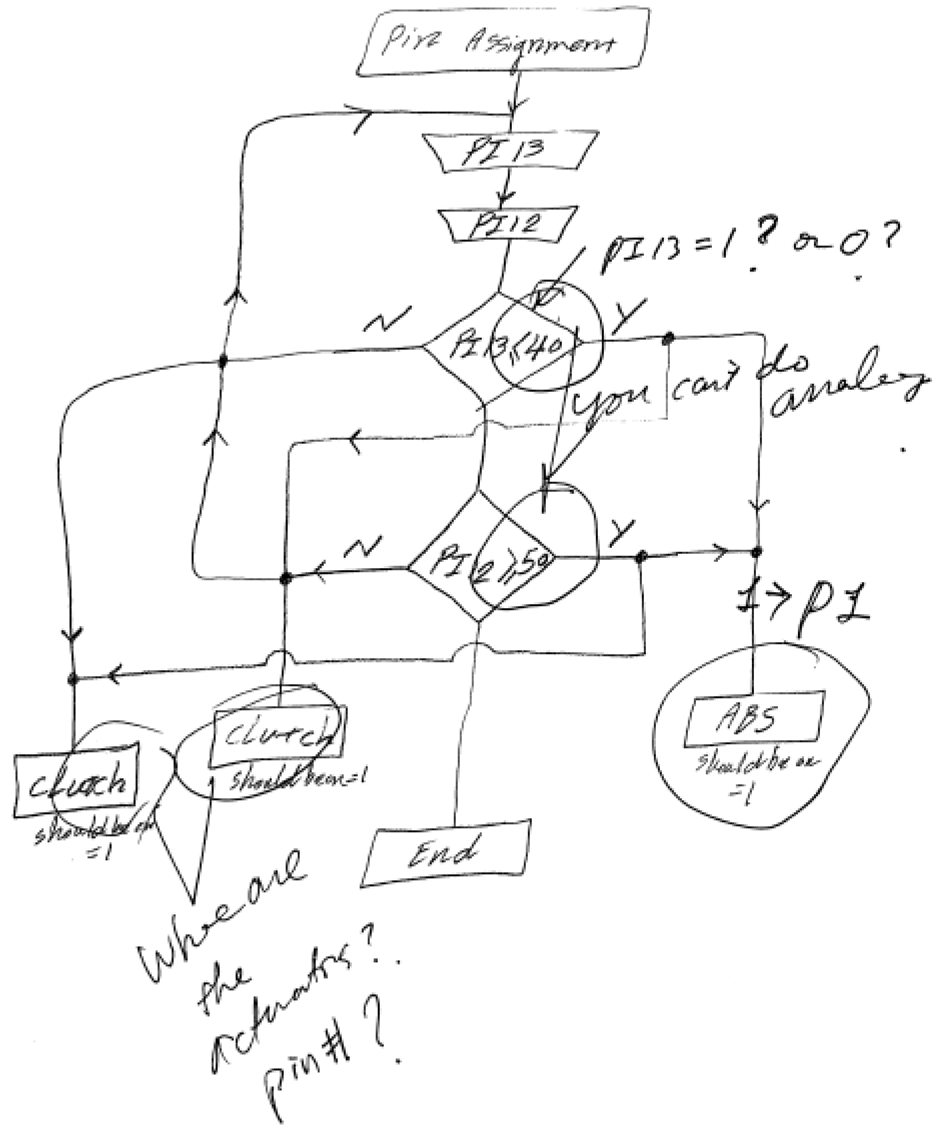
Software fault vs. Software requirement fault

- <u>Remember our class activity for an electronic control system</u>: Step 1 Computer System → Step 2 Software Requirement → Step 3 Hardware Programming →Step 4 Flowchart → Step 5Pseudo-Coding → Program
- Software Fault
  - A <u>defect</u> in the software as a result of <u>programming</u> following the software requirements
  - Debug may correct this type of fault
    - Allocation of non-computer-trained engineers would not solve the problem
- Software Requirement Fault
  - A defect in the software requirement itself
  - <u>*Design*</u> faults and failures
    - Software engineers may not correct this type of fault

SW Fault Example 1 – Requirement or SW fault?

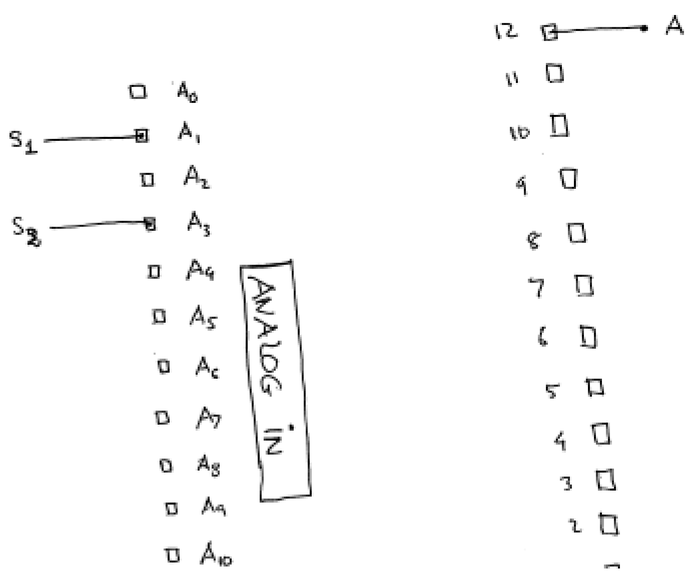


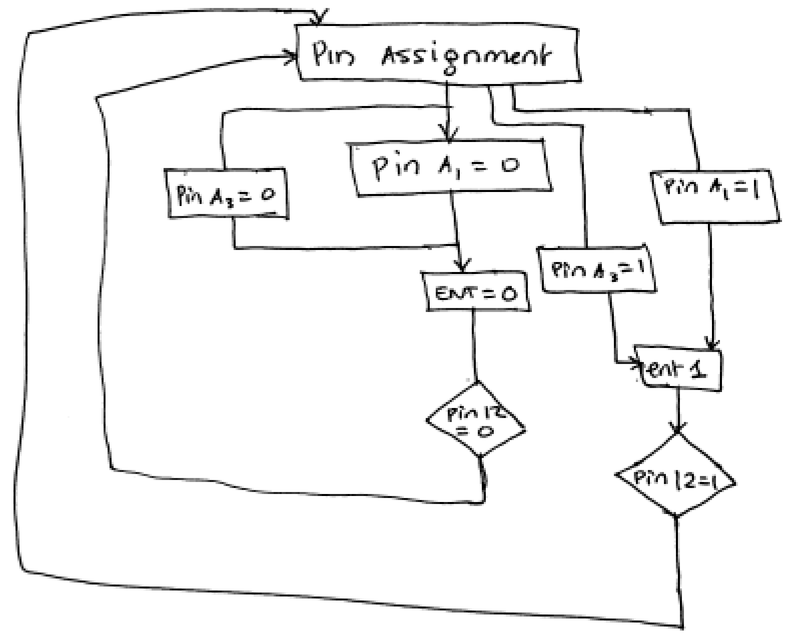
speed sensor	distance sensor	brake system decrease speed	brake system should stop the car
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1



SW Fault Example 2 - Requirement or SW fault?

S_1	S_2	A
0	0	0
0	1	1
1	0	1
1	1	1





What happens if pin A_1 = 1.6 ?

Fault-Free Software

- Fault-Free Software – why we don't see as many computer-caused accidents in microwave oven, DVD player, and TVs as in Automobile
- Computer control systems for most home appliances are "bug free" because they:
  - Employ discrete variables only
  - Involve a finite discrete Input/Output function (namely, truth-table)
  - Have no real-time constraints
  - **Therefore**, can be exhaustively tested (subjected to all possible combinations of input variables and correct output for each input) and verified
- Simply put, their software requirements are simple.

Side Bar

Assignment #3

System Complexity

and

Accidents

Software in Complex Systems

Assignment #3: Read Chapter 1 The Origins of Accidents of Scott Sagan's book, ***The Limitation of Safety*** (Princeton University Press, 1993), and discuss the subject with one's own critic view. The first paragraph should comprehensively summarize the entire report. Submit (1) a paper report by Oct 16 and (2) a presentation file by Oct 20 via email. Selected good works will be invited to present in the class of Oct 21.

- Software in Complex Systems:
  - **If requirements are complex**, S/W faults can be expected to be made **during system development** → lead to **residual S/W faults** making into the installed S/W

S/W Faults/Failures and Effects

- 3 Types of S/W
  - Application S/W
    - S/W made/created by designer
  - System S/W
    - Third party S/W like Windows, iOS, Android, or Unix
    - Hosts the application S/W and provide an interface between the application S/W and the hardware [ex. PC, Smartphones, etc.]
  - Development S/W
    - Application development platform S/W
    - Assembler, compliers, libraries,
    - JDK
    - iOS SDK
    - Android SDK
    - MSDN

Experience suggests that if the designer is correctly using mature, field-proven system S/W and development S/W, the number of faults that can be surfaced from the application S/W will be smaller.

One clearly assumes great risk by undertaking a safety-critical compute system design using new-production system S/W and/or development S/W.

Application S/W Faults -1

- 3 categories
  - 1 Misinterpreted requirements
    - Programmer has an incorrect understanding of the requirements
    - In a complex system with requirements of a hundred or more pages, dangerous misinterpretation can be made, where, particularly, the programmer has limited understanding of the physical application.
  - 3 Clerical Error
    - Typographical errors
      - Period(.) used instead of comma(,)
      - Sign reversals (+ → - ; - → +)
      - “>” instead of “>>”

Application S/W Faults -2

- 3 categories
  - 2 Incorrect software design or implementation
    - Requirements are understood correctly, but an error is made in the design of the software or in coding.
    - This is the classic “software bug”
    - Subtle fault which can be introduced under the assumption that the coding correctly follows the requirements
    - Error causes
      - Wrong variable names
      - Wrong functions
      - Mistake in a loop index range
      - Failing to initialize variables
      - Calling the wrong subroutine
      - Falling into an infinite loop
      - Stack overflow

Most Common Errors in C++

ace.cs.ohiou.edu/new_users/error.html

Listed below are some common programming errors

1. Misuse of the Include Guard.

A common mistake is to use same symbol in multiple files for #ifndef.

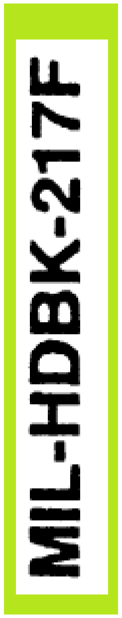
2. Typo's : Using ">" for ">>" and "<" for "<<"
3. Trying to directly access the private variables in the main program.
4. Switch Statments without break.
5. Wrong usage of postfix and prefix operator (diff between i++ and ++i)
6. Undeclared and Unitialised Variables and functions.
7. ALWAYS USE MAKE FILE if you have more than one C++ program. The order of compilations matters a lot too.
8. Trying to include "INCORRECT" header fuction.
9. Marking a member function as const in the class definition but not in the member function implementation.
10. Returning a value in a void function.
11. Confusing the name of an array with the contents of the first element.
12. Cstring array Errors - Arr[10] = Arr[0] to Arr[9]. Trying to access Arr[10] element.
13. Using "=" (assignment operator) instead of "= =" (comparison operators) `scanf()` without '&' and wrong format.(IN C)
14. Trying to divide a number by Zero.
15. Poor Loop Exiting comparisons will tend to either loop being not executed at all or goes to an infinite loop.
16. Not using string functions and treating the strings are integer . Say trying to compare string by (string1= = string2) , rather than using `strcmp` command
17. CString not terminated by '\0'- Null character
18. Mismatched "{" or IF-ELSE statements or for that matter any looping statment.
19. Namespace errors

Design Faults and Failures

- Causes of Design Requirements ["expected actions of the compute system"] and Design Faults
  - 1 Personnel Error
    - Outright mistakes
    - Omissions
    - Misinterpretations
  - 2 Limited Engineering Knowledge
    - Limited engineering knowledge available
    - Not enough experience on unpredictable faults
      - Nuclear plants
      - Airliners
  - 3 Added Complexity
    - Safety-Related Components added to the basic computer control system in the safety-critical systems → simple design problem becomes highly complex problem
    - In general, systems get more complex, and deployed computer control system and safety-related system are complicated and "out-of-hands"

Part Failure Rate Determination - Activity

- Understanding the Failure Rate Models
  - Internal structure, package type, manufacturing process, testing process, screening process, quality control, and the condition the part is installed and used.
- Preparation
  - MIL-HDBK-217F
    - printout of section 5 – for guided example for microcircuits
    - PDF file for other sections for resistors, capacitors, diodes, etc.
  - Notes or scratch papers
  - Calculators or Calculator Software
  - Patience



Part Failure Rate Model
(5.1 Gate/Logic Arrays and Microprocessors)

$$\lambda_p = (C_1\pi_T + C_2\pi_E)\,\pi_Q\pi_L \quad \text{Failures}/10^6 \text{ Hours}$$

λ_p : Failure Rate

C_1 : Die Complexity Failure Rate

C_2 : Package Failure Rate

π_T : Temperature Factor

π_E : Environmental Factor

π_Q : Quality Factor

π_L : Learning Factor (Years in Production)

Microprocessor
Die Complexity Failure Rate - C_1

No. Bits	Bipolar C_1	MOS C_1
Up to 8	.060	.14
Up to 16	.12	.28
Up to 32	.24	.56

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10

Part Failure Rate Model
(5.2 MOS Memories)

$$\lambda_p = (C_1 \pi_T + C_2 \pi_E + \lambda_{cyc}) \pi_Q \pi_L \text{ Failures}/10^6 \text{ Hours}$$

λ_p : Failure Rate

C_1 : Die Complexity Failure Rate

C_2 : Package Failure Rate

π_T : Temperature Factor

π_E : Environmental Factor

π_Q : Quality Factor

π_L : Learning Factor (Years in Production)

λ_{cyc} : Read/Write Cycling Inducded Failure Rate (EEPROMS only)

$\lambda_{cyc} = 0$ For all other devices

$$\lambda_{cyc} = \left[A_1 \; B_1 + \frac{A_2 B_2}{\pi_Q} \right] \pi_{ECC}$$

A_1 B_1 A_2 B_2 : Model Factor

π_{ECC} : Error Correction Code Options

Error Correction Code (ECC) Options:

1. No On-Chip ECC	$\pi_{ECC} = 1.0$
2. On-Chip Hamming Code	$\pi_{ECC} = .72$
3. Two-Needs-One Redundant Cell Approach	$\pi_{ECC} = .68$

Part Failure Rate Model
(5.3 CMOS VLSI with more than 60,000 gates)

$$\lambda_p = \lambda_{BD}\pi_{MFG}\pi_T\pi_{CD} + \lambda_{BP}\pi_E\pi_Q\pi_{PT} + \lambda_{EOS} \quad \text{Failures}/10^6 \text{ Hours}$$

λ_p : Failure Rate

C_1 : Die Complexity Failure Rate

C_2 : Package Failure Rate

π_T : Temperature Factor

π_E : Environmental Factor

π_Q : Quality Factor

π_L : Learning Factor (Years in Production)

λ_{BD} : Die Base Failure Rate

π_{MFG} : Manufacturing Process Correction Factor

π_{CD} : Die Complexity Correction Factor

λ_{BP} : Package Base Failure Rate

π_{PT} : Package Type Correctin Factor

λ_{EOS} : Electrical Ovestress Failure Rate

Part Type	λ_{BD}
Logic and Custom	0.16
Gate Array	0.24

Package Type	π_{PT}	
	Hermetic	Nonhermetic
DIP	1.0	1.3
Pin Grid Array	2.2	2.9
Chip Carrier	4.7	6.1

Part Failure Rate Model
(5.4 GaAs and Digital Device [of FET])

$$\lambda_p = [\, C_1 \pi_T \pi_A + C_2 \pi_E \,] \pi_L \pi_Q \text{ Failures}/10^6 \text{ Hours}$$

λ_p : Failure Rate

C_1 : Die Complexity Failure Rate

C_2 : Package Failure Rate

π_T : Temperature Factor

π_E : Environmental Factor

π_Q : Quality Factor

π_L : Learning Factor (Years in Production)

π_A : Device ApplicationFactor

Application	π_A
Digital Devices All Digital Applications	1.0

Digital: Die Complexity Failure Rates - C_1

Complexity (No. of Elements)	C_1
1 to 1000	25
1,001 to 10,000	51

1. C_1 accounts for the following active elements: transistors, diodes.

Part Failure Rate Model
(Section 5.5 Hybrid Microcircuits)

DESCRIPTION
Hybrid Microcircuits

$$\lambda_p = [\Sigma N_c \lambda_c] (1 + .2 \pi_E) \pi_F \pi_Q \pi_L \text{ Failures}/10^6 \text{ Hours}$$

N_c = Number of Each Particular Component
λ_c = Failure Rate of Each Particular Component

The general procedure for developing an overall hybrid failure rate is to calculate an individual failure rate for each component type used in the hybrid and then sum them. This summation is then modified to account for the overall hybrid function (π_F), screening level (π_Q), and maturity (π_L). The hybrid package failure rate is a function of the active component failure modified by the environmental factor (i.e., (1 + .2 π_E)). Only the component types listed in the following table are considered to contribute significantly to the overall failure rate of most hybrids. All other component types (e.g., resistors, inductors, etc.) are considered to contribute insignificantly to the overall hybrid failure rate, and are assumed to have a failure rate of zero. This simplification is valid for most hybrids; however, if the hybrid consists of mostly passive components then a failure rate should be calculated for these devices. If factoring in other component types, assume π_Q = 1, π_E =1 and T_A = Hybrid Case Temperature for these calculations.

Determination of λ_c

Determine λ_c for These Component Types	Handbook Section	Make These Assumptions When Determining λ_c
Microcircuits	5	$C_2 = 0$, $\pi_Q = 1$, $\pi_L = 1$, T_J as Determined from Section 5.12, $\lambda_{BP} = 0$ (for VHSIC).
Discrete Semiconductors	6	$\pi_Q = 1$, T_J as Determined from Section 6.14, $\pi_E = 1$.
Capacitors	10	$\pi_Q = 1$, T_A = Hybrid Case Temperature, $\pi_E = 1$.

Failure Rate Determination Example 1 (Sec 5.13)

Example 1: CMOS Digital Gate Array

Given: A CMOS digital timing chip (4046) in an airborne inhabited cargo application, case temperature 48°C, 75mW power dissipation. The device is procured with normal manufacturer's screening consisting of temperature cycling, constant acceleration, electrical testing, seal test and external visual inspection, in the sequence given. The component manufacturer also performs a B-level burn-in followed by electrical testing. All screens and tests are performed to the applicable MIL-STD-883 screening method. The package is a 24 pin ceramic DIP with a glass seal. The device has been manufactured for several years and has 1000 transistors.

- Solution

$$\lambda_p = (C_1 \pi_T + C_2 \pi_E) \pi_Q \pi_L \quad \text{Failures}/10^6 \text{ Hours}$$

C_1	=	.020	1000 Transistors ≈ 250 Gates, MOS C_1 Table, Digital Column

P 5-3

MOS Digital and Linear Gate/Logic Array Die Complex

Digital No. Gates	Digital C_1	Linear No. Transistors	Linear C_1
1 to 100	.010	1 to 100	.010
101 to 1,000	.020	101 to 300	.020
1,001 to 3,000	.040	301 to 1,000	.040
3,001 to 10,000	.080	1,001 to 10,000	.060
10,001 to 30,000	.16		
30,001 to 60,000	.29		

# of logic gates (L), which have N inputs, contained in T transistor chip:

$$L = \frac{T}{2*N} \quad \text{or} \quad \frac{T}{2*(N+1)}$$

5,001 to 20,000	.0068

NAND, NOR, NOT: transistors = 2 * # of inputs

AND, OR, transistors = 2 * # of inputs + 2

Failure Rate Determination Example 1

- Solution (-continued) $\lambda_p = (C_1\pi_T + C_2\pi_E)\,\pi_Q\pi_L$ Failures/10^6 Hours

π_T = .29	Determine T_J from Section 5.11 $T_J = 48°C + (28°C/W)(.075W) = 50°C$ Determine π_T from Section 5.8, Digital MOS Column.

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10

5.8 MICROCIRCUITS, π_T TABLE FOR ALL

Temperature Factor For All Microcircuits - π_T

	TTL, ASTTL, CML, HTTL, FTTL, DTL, ECL, ALSTTL	F, LTTL, STTL	BiCMOS, LSTTL	III, I³L, ISL	Digital MOS, VHSIC CMOS	Linear (Bipolar & MOS)	M
Ea(eV) → T_J (°C)	.4	.45	.5	.6	.35	.65	
25	.10	.10	.10	.10	.10	.10	
30	.13	.13	.14	.15	.13	.15	
35	.17	.18	.19	.21	.16	.23	
40	.21	.23	.25	.31	.19	.34	
45				.43	.24	.49	
				.61	.29	.71	
				.85	.35	1.0	
				1.2	.42	1.4	
				1.6	.50	2.0	
				2.1	.60	2.8	
				2.9	.71	3.8	
				3.8	.84	5.2	
				5.0	.98	7.0	

E_a = Effective Activation Energy (eV) (Shown Above)

T_J = Worse Case Junction Temperature (Silicon Devices) or Average Active Device Channel Temperature (GaAs Devices).

See Section 5.11 (or Section 5.12 for Hybrids) for T_J Determination.

NOTES: 1. $T_J = T_C + P\,\theta_{JC}$

T_C = Case Temperature (°C)

P = Device Power Dissipation (W)

θ_{JC} = Junction to Case Thermal Resistance (°C/W)

Example 1

5.11 MICROCIRCUITS, T_J DETERMINATION, (ALL EXCEPT HYBRIDS)

75mW

$$T_J = T_C + \theta_{JC} P$$

>>> 48+28*0.075
50.100000000000001

T_J = Worst Case Junction Temperature (°C).

T_C = Case Temperature (°C). If not available, use the following default table.

48

θ_{JC} = Junction-to-case thermal resistance (°C/watt) for a device soldered into a printed circuit board. If θ_{JC} is not available, use a value contained in a specification for the closest equivalent device or use the following table.

Package Type (Ceramic Only)	Die Area > 14,400 mil^2 θ_{JC} (°C/W)	Die Area ≤ 14,400 mil^2 θ_{JC} (°C/W)
Dual-In-Line	11	28
Flat Package	10	22
Chip Carrier	10	20
Pin Grid Array	10	20
Can	–	70

75mW

P = The maximum power dissipation realized in a system application. If the applied power is not available, use the maximum power dissipation from the specification for the closest equivalent device.

Failure Rate Determination Example 1

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10

NOTES: 1. T_J = $T_C + P\,\theta_{JC}$
T_C = Case Temperature (°C)
P = Device Power Dissipation (W)
θ_{JC} = Junction to Case Thermal Resistance (°C/W)

5.8 MICROCIRCUITS, π_T TABLE FOR ALL

Temperature Factor For All Microcircuits - π_T

	TTL, ASTTL, CML, HTTL, FTTL, DTL, ECL, ALSTTL	F, LTTL, STTL	BiCMOS, LSTTL	III, I²L, ISL	Digital MOS, VHSIC CMOS	Linear (Bipolar & MOS)	M
Ea(eV) → T_J (°C)	.4	.45	.5	.6	.35	.65	
25	.10	.10	.10	.10	.10	.10	
30	.13	.13	.14	.15	.13	.15	
35	.17	.18	.19	.21	.16	.23	
40	.21	.23	.25	.31	.19	.34	
45	.27	.3	.34	.43	.24	.49	
50	.33	.39	.45	.61	.29	.71	
55	.42	.50	.59	.85	.35	1.0	
60	.51	.63	.77	1.2	.42	1.4	
65	.63	.80	1.0	1.6	.50	2.0	
70	.77	1.0	1.3	2.1	.60	2.8	
75	.94	1.2	1.6	2.9	.71	3.8	
80	1.1	1.5	2.1	3.8	.84	5.2	
85	1.4	1.9	2.6	5.0	.98	7.0	

π_T = .29

Determine T_J from Section 5.11

T_J = 48°C + (28°C/W)(.075W) = 50°C

Determine π_T from Section 5.8, Digital MOS Column.

Failure Rate Determination Example 1

C_2	=	.011	Section 5.9

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10

Package Failure Rate for all Microcircuits - C_2

	Package Type				
Number of Functional Pins, N_p	Hermetic: DIPs w/Solder or Weld Seal, Pin Grid Array (PGA)[1], SMT (Leaded and Nonleaded)	DIPs with Glass Seal[2]	Flatpacks with Axial Leads on 50 Mil Centers[3]	Cans[4]	Nonhermetic: DIPs, PGA, SMT (Leaded and Nonleaded)[5]
3	.00092	.00047	.00022	.00027	.0012
4	.0013	.00073	.00037	.00049	.0016
6	.0019	.0013	.00078	.0011	.0025
8	.0026	.0021	.0013	.0020	.0034
10	.0034	.0029	.0020	.0031	.0043
12	.0041	.0038	.0028	.0044	.0053
14	.0048	.0048	.0037	.0060	.0062
16	.0056	.0059	.0047	.0079	.0072
18	.0064	.0071	.0058		.0082
22	.0079	.0096	.0083		.010
24	.0087	.011	.0098		.011
28	.010	.014			.013
36	.013	.020			.017
40	.015	.024			.019
64	.025	.048			.032
80	.032				.041
128	.053				.068

Failure Rate Determination Example 1

π_E	= 4.0	Section 5.10
π_L	= 1	Section 5.10

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10

Table 3-2: Environmental Symbol and Description (cont'd)

Environment	π_E Symbol	Equivalent MIL-HDBK-217E, Notice 1 π_E Symbol	Description
Airborne, Inhabited, Cargo	A_{IC}	A_{IC} A_{IT} A_{IB}	Typical conditions in cargo compartments which can be occupied by an aircrew. Environment extremes of pressure, temperature, shock and vibration are minimal. Examples include long mission aircraft such as the C130, C5, B52, and C141. This category also applies to inhabited areas in lower performance smaller aircraft such as the T38.

5.10 MICROCIRCUITS, π_E, λ_L AND π_Q TABLES FOR ALL

Environment Factor - π_E

Environment	π_E
G_B	.50
G_F	2.0
G_M	4.0
N_S	4.0
N_U	6.0
A_{IC}	4.0
A_{IF}	5.0
A_{UC}	5.0
A_{UF}	8.0
A_{RW}	8.0
S_F	.50
M_F	5.0
M_L	12
C_L	220

Learning Factor - π_L

Years in Production, Y	π_L
$\leq .1$	2.0
.5	1.8
1.0	1.5
1.5	1.2
≥ 2.0	1.0

$$\pi_L = .01 \exp(5.35 - .35Y)$$

Y = Years generic device type has been in production

Failure Rate Determination Example 1

π_Q = 3.1

Section 5.10

Group 1 Tests	50 Points
Group 3 Tests (B-level)	30 Points
TOTAL	80 Points

$$\pi_Q = 2 + \frac{87}{80} = 3.1$$

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10

Quality Factors (cont'd): π_Q Calculation for Custom Screening Programs

Group	MIL-STD-883 Screen/Test (Note 3)	Point Valuation
1*	TM 1010 (Temperature Cycle, Cond B Minimum) and TM 2001 (Constant Acceleration, Cond B Minimum) and TM 5004 (or 5008 for Hybrids) (Final Electricals @ Temp Extremes) and TM 1014 (Seal Test, Cond A, B, or C) and TM 2009 (External Visual)	50
2*	TM 1010 (Temperature Cycle, Cond B Minimum) or TM 2001 (Constant Acceleration, Cond B Minimum) TM 5004 (or 5008 for Hybrids) (Final Electricals @ Temp Extremes) and TM 1014 (Seal Test, Cond A, B, or C) and TM 2009 (External Visual)	37
3	Pre-Burn in Electricals TM 1015 (Burn-in B-Level/S-Level) and TM 5004 (or 5008 for Hybrids) (Post Burn-in Electricals @ Temp Extremes)	30 (B Level) 36 (S Level)

$$\pi_Q = 2 + \frac{87}{\Sigma \text{ Point Valuations}}$$

EXAMPLES:

1 Mfg. performs Group 1 test and Class B burn-in:

$$\pi_Q = 2 + \frac{87}{50+30} = 3.1$$

Failure Rate Determination Example 1 - Finally

Example 1: CMOS Digital Gate Array

Given: A CMOS digital timing chip (4046) in an airborne inhabited cargo application, case temperature 48°C, 75mW power dissipation. The device is procured with normal manufacturer's screening consisting of temperature cycling, constant acceleration, electrical testing, seal test and external visual inspection, in the sequence given. The component manufacturer also performs a B-level burn-in followed by electrical testing. All screens and tests are performed to the applicable MIL-STD-883 screening method. The package is a 24 pin ceramic DIP with a glass seal. The device has been manufactured for several years and has 1000 transistors.

- **Solution**

$$\lambda_p = (C_1\pi_T + C_2\pi_E)\,\pi_Q\pi_L \quad \text{Failures}/10^6 \text{ Hours}$$

$C_1 = .020$

$\pi_T = .29$

$C_2 = .011$

$\pi_E = 4.0$

$\pi_Q = 3.1$

$\pi_L = 1$

$$\lambda_p = [\,(.020)(.29) + (.011)\,(4)\,]\,(3.1)(1) = .15$$

Failure/10^6 Hours

```
>>> 1000000/0.15
6666666.666666667
>>> 365*24
8760
>>> 6666666/8760
761
>>>
```

Example 2 – Class Activity

Example 2: EEPROM

Given: A 128K Flotox EEPROM that is expected to have a T_J of 80°C and experience 10,000 read/write cycles over the life of the system. The part is procured to all requirements of Paragraph 1.2.1, MIL-STD-883, Class B screening level requirements and has been in production for three years. It is packaged in a 28 pin DIP with a glass seal and will be used in an airborne uninhabited cargo application.

$$\pi_p = (C_1 \pi_T + C_2 \pi_E + \lambda_{cyc}) \pi_Q \pi_L \qquad \text{Section 5.2}$$

- What is EEPROM?
- What is Flotox (FLOating gate Tunneling Oxide) EEPROM?

Example 2 – Class Activity – Step 1

Example 2: EEPROM

Given: A 128K Flotox EEPROM that is expected to have a T_J of 80°C and experience 10,000 read/write cycles over the life of the system. The part is procured to all requirements of Paragraph 1.2.1, MIL-STD-883, Class B screening level requirements and has been in production for three years. It is packaged in a 28 pin DIP with a glass seal and will be used in an airborne uninhabited cargo application.

$$\pi_p = (C_1 \pi_T + C_2 \pi_E + \lambda_{cyc}) \pi_Q \pi_L$$ Section 5.2

C_1 = .0034 Section 5.2

Example 2 – Class Activity – Step 2

Example 2: EEPROM

Given: A 128K Flotox EEPROM that is expected to have a T_J of 80°C and experience 10,000 read/write cycles over the life of the system. The part is procured to all requirements of Paragraph 1.2.1, MIL-STD-883, Class B screening level requirements and has been in production for three years. It is packaged in a 28 pin DIP with a glass seal and will be used in an airborne uninhabited cargo application.

$$\pi_p = (C_1 \pi_T + C_2 \pi_E + \lambda_{cyc}) \pi_Q \pi_L \qquad \text{Section 5.2}$$

π_T = 3.8 Section 5.8

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10
λ_{cyc} (EEPROMS only)	Page 5-5
$\lambda_{cyc} = 0$	For all other devices

Example 2 – Class Activity – Step 3

Example 2: EEPROM

Given: A 128K Flotox EEPROM that is expected to have a T_J of 80°C and experience 10,000 read/write cycles over the life of the system. The part is procured to all requirements of Paragraph 1.2.1, MIL-STD-883, Class B screening level requirements and has been in production for three years. It is packaged in a 28 pin DIP with a glass seal and will be used in an airborne uninhabited cargo application.

$$\lambda_p = (C_1 \pi_T + C_2 \pi_E + \lambda_{cyc}) \pi_Q \pi_L$$ Section 5.2

C_2 = .014 Section 5.9

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10
λ_{cyc} (EEPROMS only)	Page 5-5
$\lambda_{cyc} = 0$	For all other devices

Example 2 – Class Activity – Step 4

Example 2: EEPROM

Given: A 128K Flotox EEPROM that is expected to have a T_J of 80°C and experience 10,000 read/write cycles over the life of the system. The part is procured to all requirements of Paragraph 1.2.1, MIL-STD-883, Class B screening level requirements and has been in production for three years. It is packaged in a 28 pin DIP with a glass seal and will be used in an airborne uninhabited cargo application.

$$\pi_p = (C_1 \pi_T + C_2 \pi_E + \lambda_{cyc}) \pi_Q \pi_L$$ Section 5.2

π_E = 5.0 Section 5.10

π_L = 1.0 Section 5.10

π_Q = 2.0 Section 5.10

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10
λ_{cyc} (EEPROMS only)	Page 5-5
λ_{cyc} = 0	For all other devices

Example 2 – Class Activity – Step 5

Example 2: EEPROM

Given: A 128K Flotox EEPROM that is expected to have a T_J of 80°C and experience 10,000 read/write cycles over the life of the system. The part is procured to all requirements of Paragraph 1.2.1, MIL-STD-883, Class B screening level requirements and has been in production for three years. It is packaged in a 28 pin DIP with a glass seal and will be used in an airborne uninhabited cargo application.

$$\lambda_p = (C_1 \pi_T + C_2 \pi_E + \lambda_{cyc}) \pi_Q \pi_L \qquad \text{Section 5.2}$$

All Other Model Parameters

Parameter	Refer to
π_T	Section 5.8
C_2	Section 5.9
π_E, π_Q, π_L	Section 5.10
λ_{cyc} (EEPROMS only)	Page 5-5
$\lambda_{cyc} = 0$	For all other devices

λ_{cyc} = .38

Section 5.2:

$$\lambda_{cyc} = \left[A_1 B_1 + \frac{A_2 B_2}{\pi_Q}\right] \pi_{ECC}$$

$A_2 = B_2 = 0$ for Flotox

Assume No ECC, $\pi_{ECC} = 1$

$A_1 = .1$, $7K \le C \le 15K$ Entry

$B_1 = 3.8$ (Use Equation 1 at bottom of B_1 and B_2 Table)

$\lambda_{cyc} = A_1 B_1 = (.1)(3.8) = .38$

There are more sections and subsections

MILITARY HANDBOOK

RELIABILITY PREDICTION OF ELECTRONIC EQUIPMENT

NOT MEASUREMENT SENSITIVE

MIL-HDBK-217F

2 DECEMBER 1991

SUPERSEDING
MIL-HDBK-217E, Notice 1
2 January 1990

RADC-TR-90-72
Final Technical Report
May 1990

- Microcircuits (Sec. 5)
- Discrete Semiconductors (Sec 6) – **Diode, transistors**, etc
- **Resistors** (Sec. 9)
- **Capacitors** (Sec. 10)
- **Inductive** Devices (Sec. 11)
- Rotating Devices – Motors (Sec. 12)
- Relays (Sec. 13)
- Switches (Sec. 14)
- Connectors (Sec. 15)
- And more !!!

Section 6

6.0 DISCRETE SEMICONDUCTORS, INTRODUCTION

6.1 DIODES, LOW FREQUENCY

$\lambda_p = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E$ Failures/10^6 Hours

6.2 DIODES, HIGH FREQUENCY (MICROWAVE, RF)

$\lambda_p = \lambda_b \pi_T \pi_A \pi_R \pi_Q \pi_E$ Failures/10^6 Hours

6.3 TRANSISTORS, LOW FREQUENCY, BIPOLAR

$\lambda_p = \lambda_b \pi_T \pi_A \pi_R \pi_S \pi_Q \pi_E$ Failures/10^6 Hours

6.4 TRANSISTORS, LOW FREQUENCY, SI FET

$\lambda_p = \lambda_b \pi_T \pi_A \pi_Q \pi_E$ Failures/10^6 Hours

6.5 TRANSISTORS, UNIJUNCTION

$\lambda_p = \lambda_b \pi_T \pi_Q \pi_E$ Failures/10^6 Hours

6.6 TRANSISTORS, LOW NOISE, HIGH FREQUENCY, BIPOLAR

$\lambda_p = \lambda_b \pi_T \pi_R \pi_S \pi_Q \pi_E$ Failures/10^6 Hours

6.7 TRANSISTORS, HIGH POWER, HIGH FREQUENCY, BIPOLAR

$\lambda_p = \lambda_b \pi_T \pi_A \pi_M \pi_Q \pi_E$ Failures/10^6 Hours

Section 9

9.0 RESISTORS, INTRODUCTION

9.1 RESISTORS, FIXED, COMPOSITION

$\lambda_p = \lambda_b \pi_R \pi_Q \pi_E$ Failures/10^6 Hours

9.2 RESISTORS, FIXED, FILM

$\lambda_p = \lambda_b \pi_R \pi_Q \pi_E$ Failures/10^6 Hours

9.3 RESISTORS, FIXED, FILM, POWER

$\lambda_p = \lambda_b \pi_R \pi_Q \pi_E$ Failures/10^6 Hours

9.4 RESISTORS, NETWORK, FIXED, FILM

$\lambda_p = .00006\, \pi_T\, \pi_{NR} \pi_Q \pi_E$ Failures/10^6 Hours

9.5 RESISTORS, FIXED, WIREWOUND

$\lambda_p = \lambda_b \pi_R \pi_Q \pi_E$ Failures/10^6 Hours

9.6 RESISTORS, FIXED, WIREWOUND, POWER

$\lambda_p = \lambda_b \pi_R \pi_Q \pi_E$ Failures/10^6 Hours

9.7 RESISTORS, FIXED, WIREWOUND, POWER, CHASSIS MOUNTED

$\lambda_p = \lambda_b \pi_R \pi_Q \pi_E$ Failures/10^6 Hours

9.8 RESISTORS, THERMISTOR

$\lambda_p = \lambda_b \pi_Q \pi_E$ Failures/10^6 Hours

Section 10

10.1 CAPACITORS, FIXED, PAPER, BY-PASS $\lambda_p = \lambda_b \pi_{CV} \pi_Q \pi_E$ Failures/10^6 Hours

10.2 CAPACITORS, FIXED, PAPER, FEED-THROUGH

10.3 CAPACITORS, FIXED, PAPER AND PLASTIC FILM

10.4 CAPACITORS, FIXED, METALLIZED PAPER, PAPER-PLASTIC AND PLASTIC

10.5 CAPACITORS, FIXED, PLASTIC AND METALLIZED PLASTIC

10.6 CAPACITORS, FIXED, SUPER-METALLIZED PLASTIC

10.7 CAPACITORS, FIXED, MICA

10.8 CAPACITORS, FIXED, MICA, BUTTON

10.9 CAPACITORS, FIXED, GLASS

10.10 CAPACITORS, FIXED, CERAMIC, GENERAL PURPOSE

10.11 CAPACITORS, FIXED, CERAMIC, TEMPERATURE COMPENSATING AND CHIP

10.20 CAPACITORS, EXAMPLE

Sections 11 & 12

11.1 INDUCTIVE DEVICES, TRANSFORMERS $\lambda_p = \lambda_b \pi_Q \pi_E$ Failures/10^6 Hours

11.2 INDUCTIVE DEVICES, COILS $\lambda_p = \lambda_b \pi_C \pi_Q \pi_E$ Failures/10^6 Hours

11.3 INDUCTIVE DEVICES, DETERMINATION OF HOT SPOT TEMPERATURE

12.1 ROTATING DEVICES, MOTORS $\lambda_p = \left[\frac{t^2}{\alpha_B{}^3} + \frac{1}{\alpha_W}\right] \times 10^6$ Failures/10^6 Hours

Sections 13 & 14

13.1 RELAYS, MECHANICAL $\lambda_p = \lambda_b \pi_L \pi_C \pi_{CYC} \pi_F \pi_Q \pi_E$ Failures/10^6 Hours

13.2 RELAYS, SOLID STATE AND TIME DELAY $\lambda_p = \lambda_b \pi_Q \pi_E$ Failures/10^6 Hours

14.1 SWITCHES, TOGGLE OR PUSHBUTTON

$\lambda_p = \lambda_b \pi_{CYC} \pi_L \pi_C \pi_E$ Failures/10^6 Hours

14.2 SWITCHES, BASIC SENSITIVE

14.3 SWITCHES, ROTARY

14.5 SWITCHES, CIRCUIT BREAKERS

Sections 15 & 16

15.1 CONNECTORS, GENERAL (EXCEPT PRINTED CIRCUIT BOARD)

$$\lambda_p = \lambda_b \pi_K \pi_P \pi_E \text{ Failures}/10^6 \text{ Hours}$$

15.2 CONNECTORS, PRINTED CIRCUIT BOARD

15.3 CONNECTORS, INTEGRATED CIRCUIT SOCKETS

$$\lambda_p = \lambda_b \pi_P \pi_E \text{ Failures}/10^6 \text{ Hours}$$

16.1 INTERCONNECTION ASSEMBLIES WITH PLATED THROUGH HOLES

$$\lambda_p = \lambda_b \left[N_1 \pi_C + N_2 (\pi_C + 13) \right] \pi_Q \pi_E \text{ Failures}/10^6 \text{ Hours}$$

Sections 17 - 23

17.1 CONNECTIONS $\lambda_p = \lambda_b \pi_Q \pi_E$ Failures/10^6 Hours

18.1 METERS, PANEL $\lambda_p = \lambda_b \pi_A \pi_F \pi_Q \pi_E$ Failures/10^6 Hours

19.1 QUARTZ CRYSTALS $\lambda_p = \lambda_b \pi_Q \pi_E$ Failures/10^6 Hours

20.1 LAMPS $\lambda_p = \lambda_b \pi_U \pi_A \pi_E$ Failures/10^6 Hours

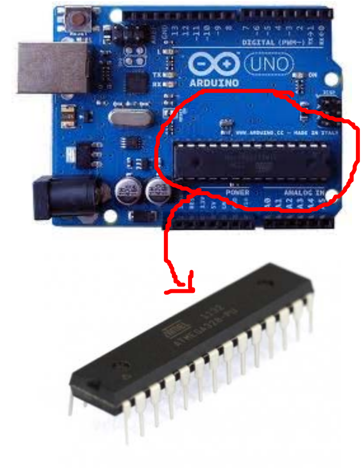
21.1 ELECTRONIC FILTERS, NON-TUNABLE

$\lambda_p = \lambda_b \pi_Q \pi_E$ Failures/10^6 Hours

22.1 FUSES $\lambda_p = \lambda_b \pi_E$ Failures/10^6 Hours

23.1 MISCELLANEOUS PARTS

Failure Rate Determination – Class Project



- Failure Rate Calculations for:
  - 1. The popular microcontroller board ***Arduino UNO*** is built on Atmel microcontroller ATmega328. Referring the Atmel Microcontroller datasheet and the **MIL-HDBK-217 manual**, determine **the failure rate of the ATmega328 microcontroller**
  - 2. Texas Instrument's TLC2254M is Quad micro-power operational amplifier, and is QML certified for Military and Defense Application. Determine the **failure rate of TLC2254M** by referring MIL-HDBK-217 and TLC2254M datasheet from Texas Instrument. Note that TLC2254M is a Hybrid IC with numerous resistors, transistors, diodes, and capacitors, which all are to be considered in determining the failure rate

- Report should have details steps with explanations and justifications.
- Report Submission Due: **TBD**