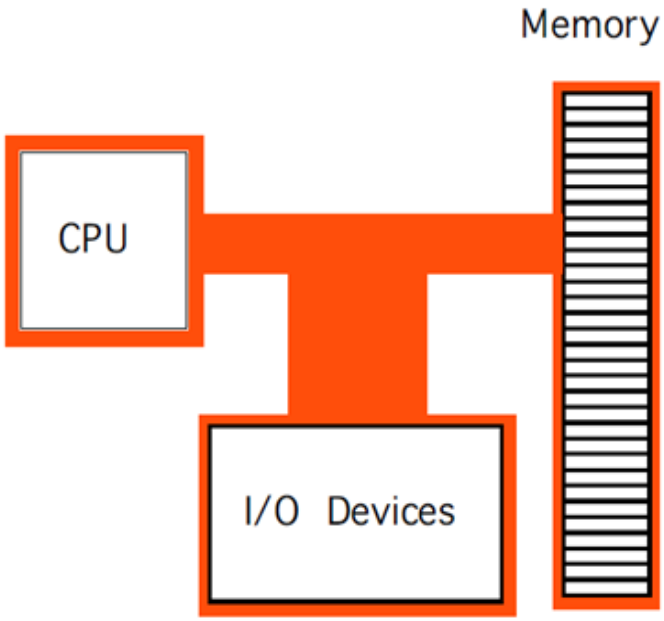
System Organization

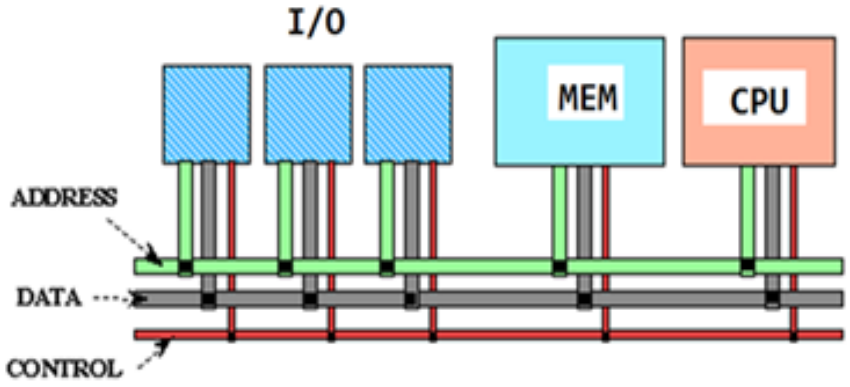
"architecture"

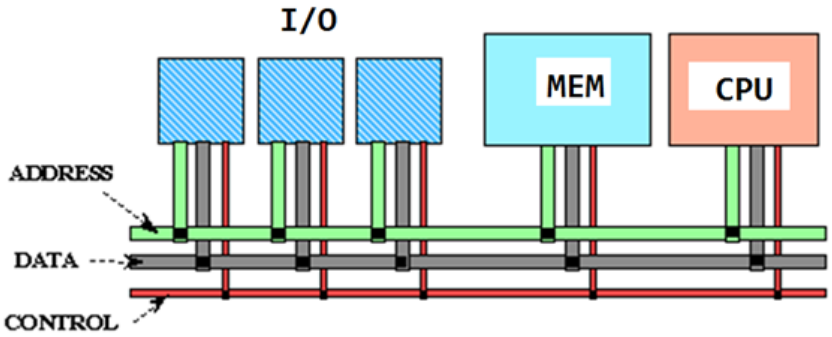
- Microarchitecture
- Instruction Set architecture (ISA)

System Organization



System Bus





Address Bus

Data Bus

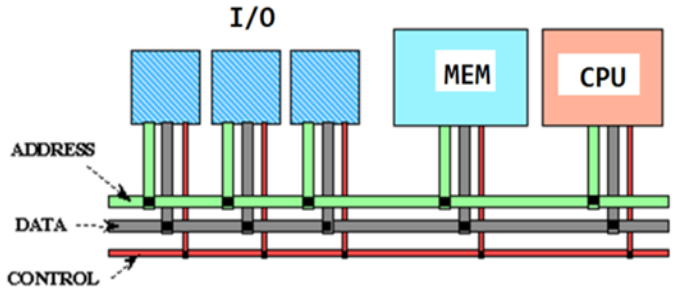
Address Bus

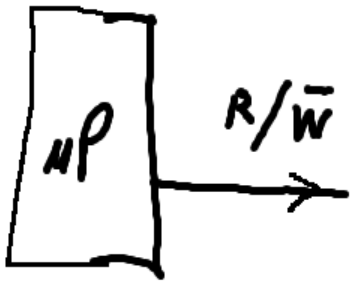
Range of unique address

Address Bus

- What would be the address bus size for a processor which had max addressable memory locations of 256 GB?

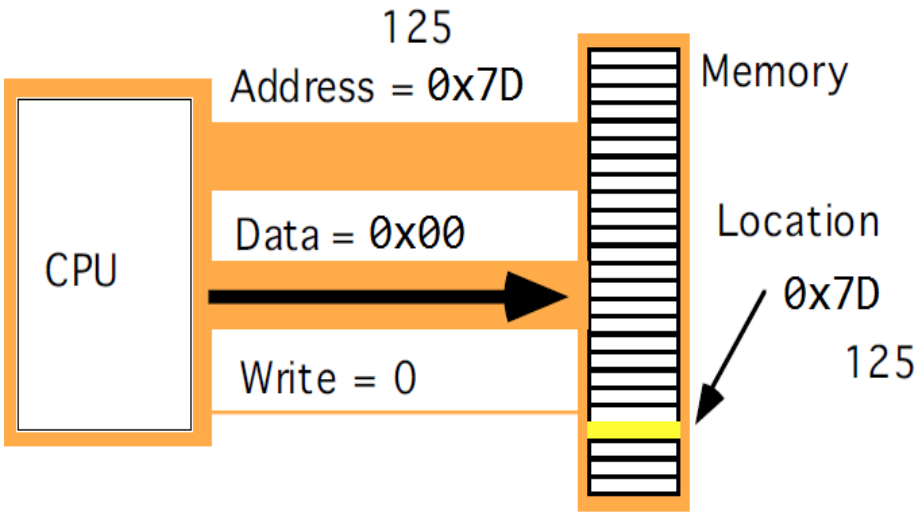
Control Bus





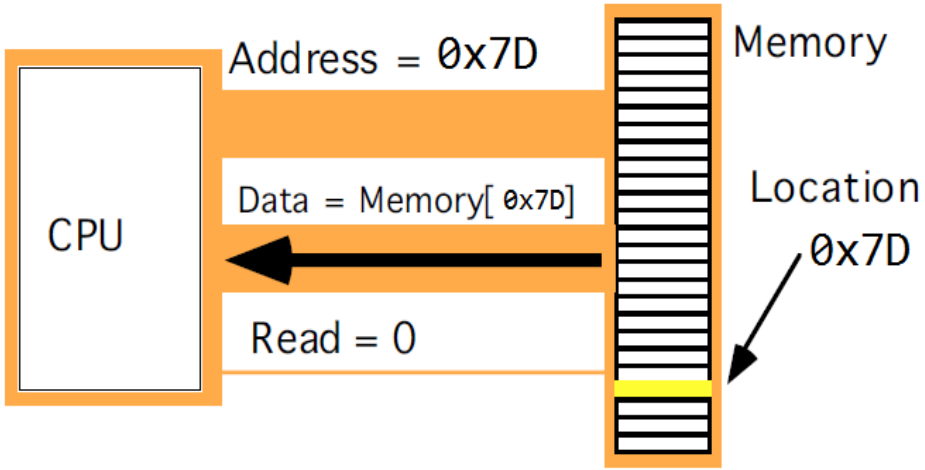
Memory Write

Memory[0x7D]:=0 %pseudo-code



Memory Read

CPU:= Memory[0x7D]:%pseudo-code



Multi-Byte Write/Read ??

Memory Access Example

Memory[0x0000c0]:=0x1234ABCD

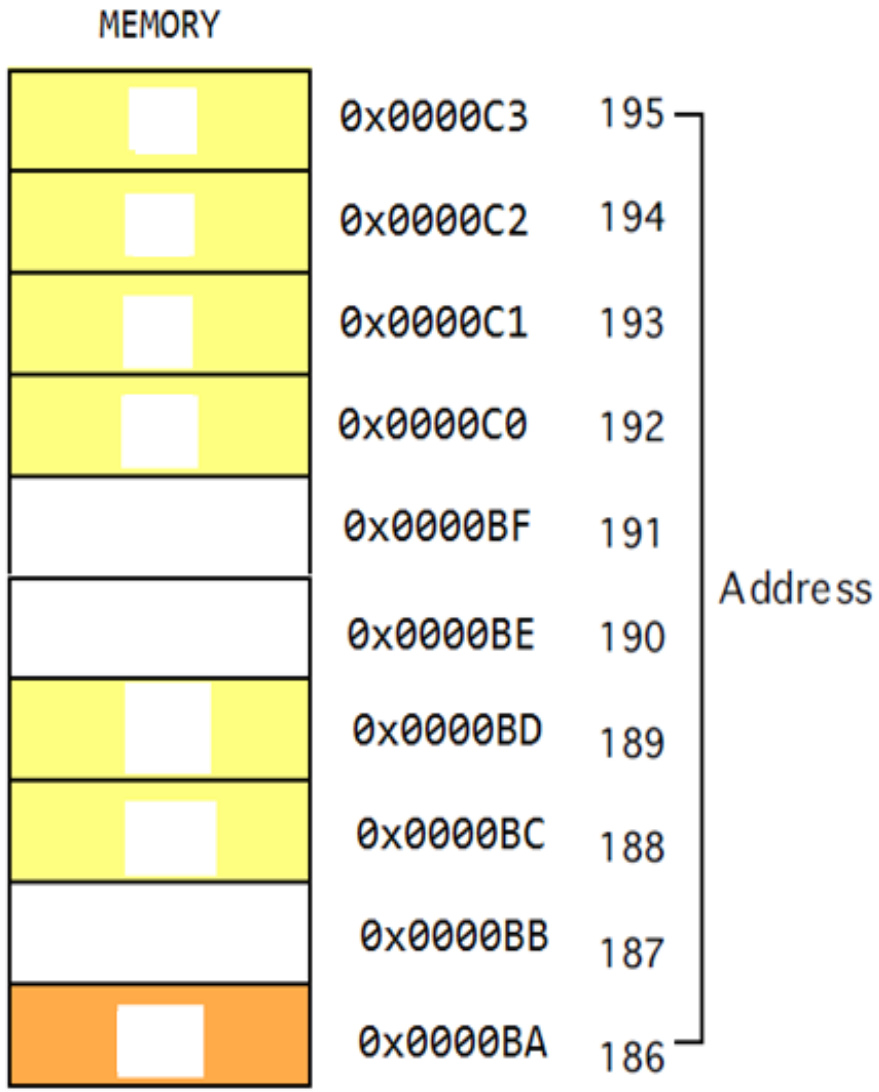
Double Word at address 192
0x0000C0

Memory[0x0000bc]:=0x12AB

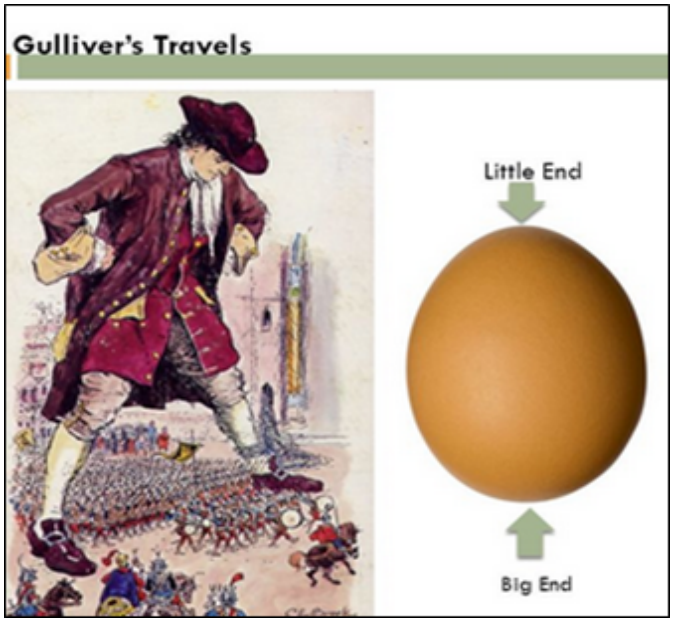
Word at address 188
0x0000BC

Memory[0x0000BA]:= 0x12

Byte at address 186
0x0000BA



Big-Endian vs. Little-Endian



- Big-Endian:
- Little- Endian:

Store data

```
        dst   src
MOV     0,    $3210
MOV     2,    $76543210
```

000006h	
000005	
000004	
000003	
000002	
000001	
000000	

Little-Endian

Intel

```
        src   dst
MOVE    $3210,    0
MOVE    $76543210,2
```

000000h	
000001	
000002	
000003	
000004	
000005	
000006	

Big-Endian

Motorola

"Endianness" Endian-Architecture

Computer System Endianness

Platform	Endian Architecture
ARM*	Bi-Endian
DEC Alpha*	Little-Endian
HP PA-RISC 8000*	Bi-Endian
IBM PowerPC*	Bi-Endian
Intel® 80x86	Little-Endian
Intel® IXP network processors	Bi-Endian
Intel® Itanium® processor family	Bi-Endian
Java Virtual Machine*	Big-Endian
MIPS*	Bi-Endian
Motorola 68k*	Big-Endian
Sun SPARC*	Big-Endian

Common file formats

Little-Endian Format	Big-Endian Format	Variable or Bi-Endian Format
BMP (Windows* & OS/2)	PSD (Adobe Photoshop*)	DXF (AutoCAD*)
GIF	IMG (GEM Raster*)	PS (Postscript*, 8 bit interpreted text, no Endian issue)
FLI (Autodesk Animator*)	JPEG, JPG	
PCX (PC Paintbrush*)	MacPaint	POV (Persistence of Visionraytracer*)
QTM (MAC Quicktime*)	SGI (Silicon Graphics*)	
RTF (Rich Text Format)	Sun Raster	RIFF (WAV & AVI*)
	WPG (WordPerfect*)	TIFF
		XWD (X Window Dump*)
Bus Protocols	**Network Protocols**	**Bus Protocols**
Infiniband	TCP/IP	GMII (8 bit wide bus, no Endian issue)
PCI Express	UDP	
PCI-32/PCI-64		
USB		

Endian-Neutral (or Bi-Endian) Approaches

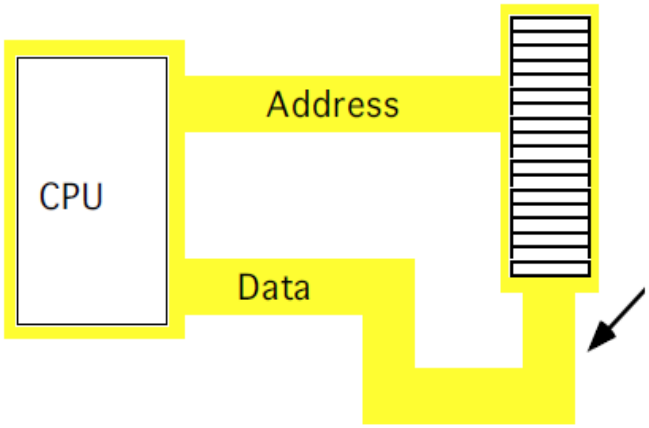
Coming Soon !!

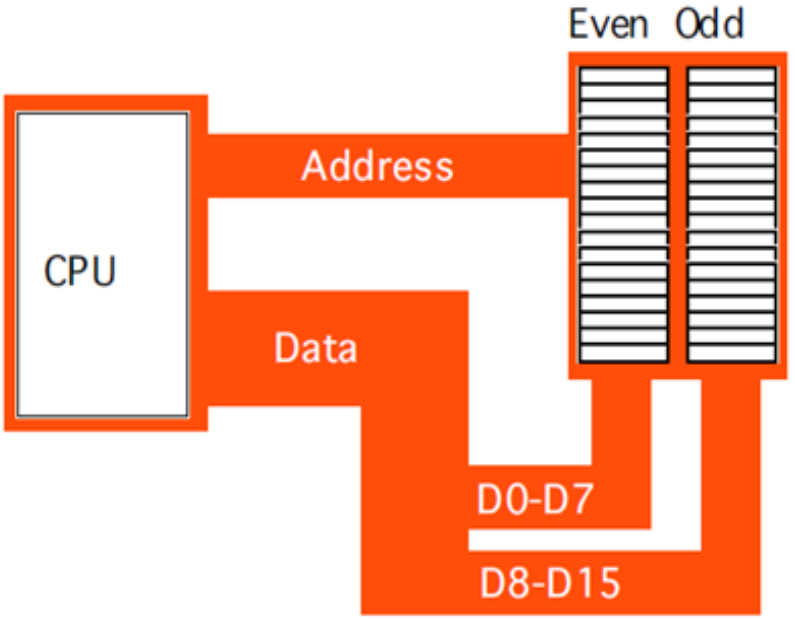
Sneak Preview !!

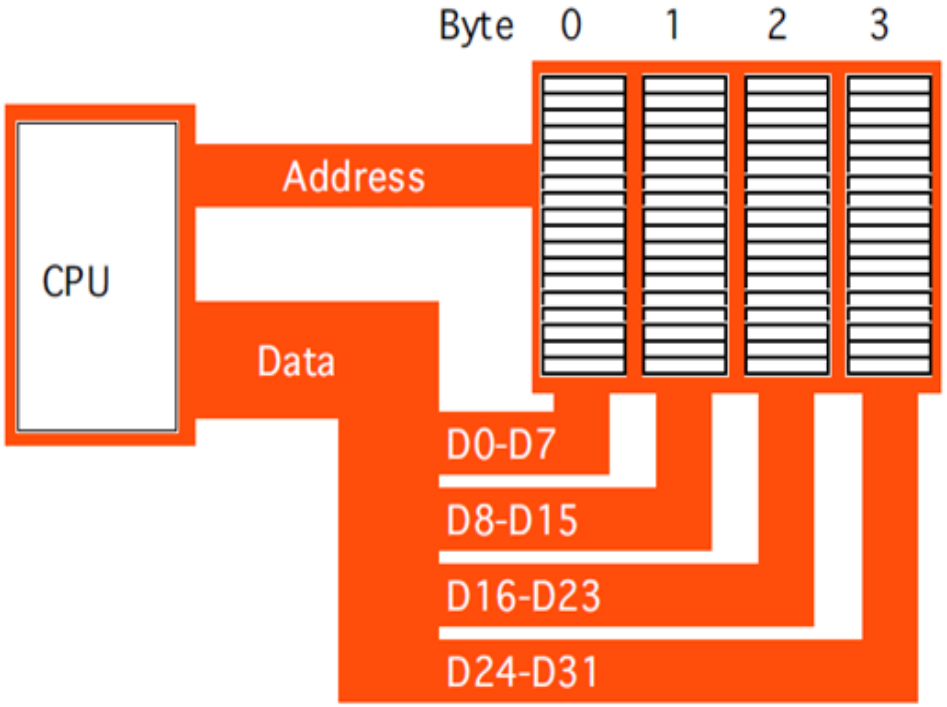
Technical Essay

- Technical ~~Report~~ essay on "Socio-Economic Responsibility of Technical Approach – the cost of two Endians"
- Questions:
  - What are the 2 endians?
  - How 2 endians were developed?
  - What's the technical cost of the problem?
  - What's the impact to society in general ?
  - What is the current remedy to the problem ?
  - If you're involved from the start in multi-byte data storage, what would you do to have a problem-free approach ?
- Scoring Rubrics
- Submission Deadline

CPU-Memory Interface for Byte and Multi-Byte Access



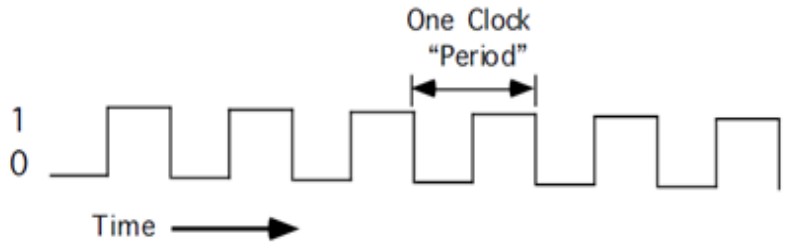




I/O Subsystem

System Timing

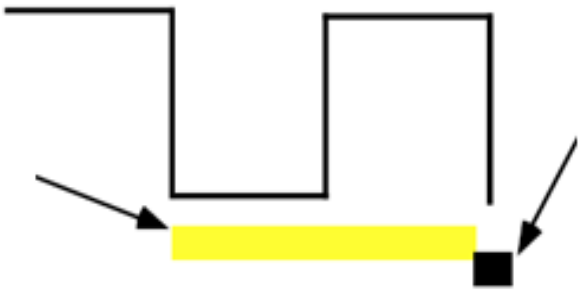
System Clock



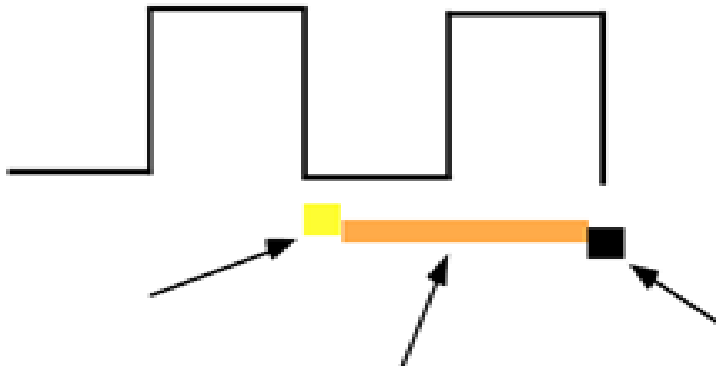
Memory Access and System Clock

- Memory Access Time:

WRITING



READING



Memory Access and System Clock

3

Memory speed (access time) is much slower than CPU

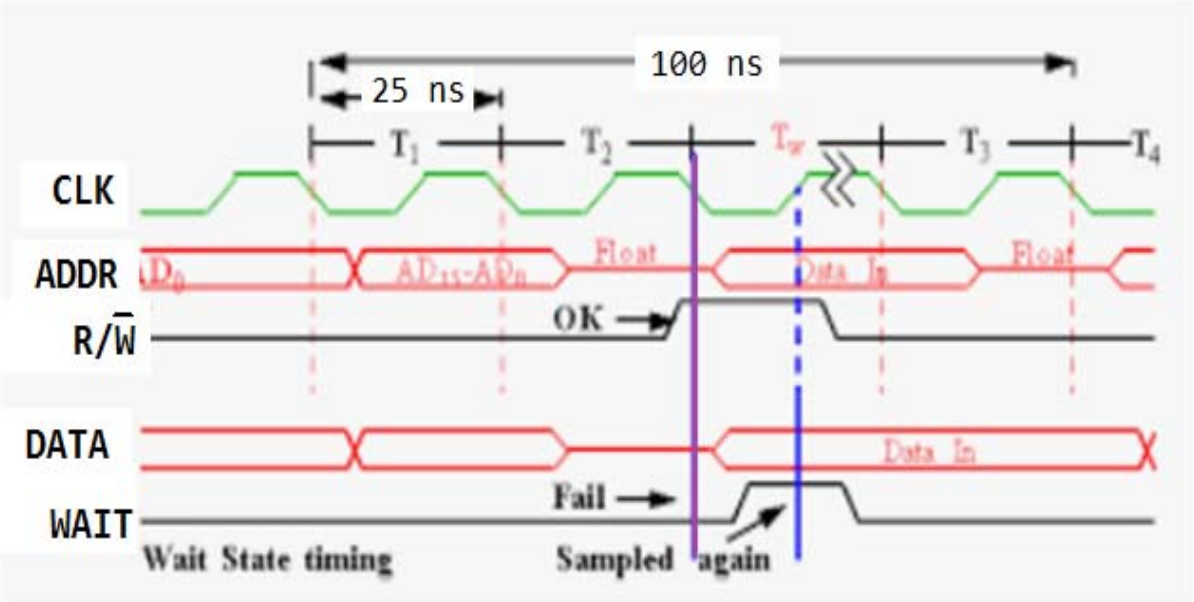
RAM (Random access memory): 50 - 100 ns

Typical 80486 (33MHZ) uses 70 ns memory

- CPU clock period is about 33 ns:
  - how to manage using 70-ns RAM?

4

- Wait States - example study

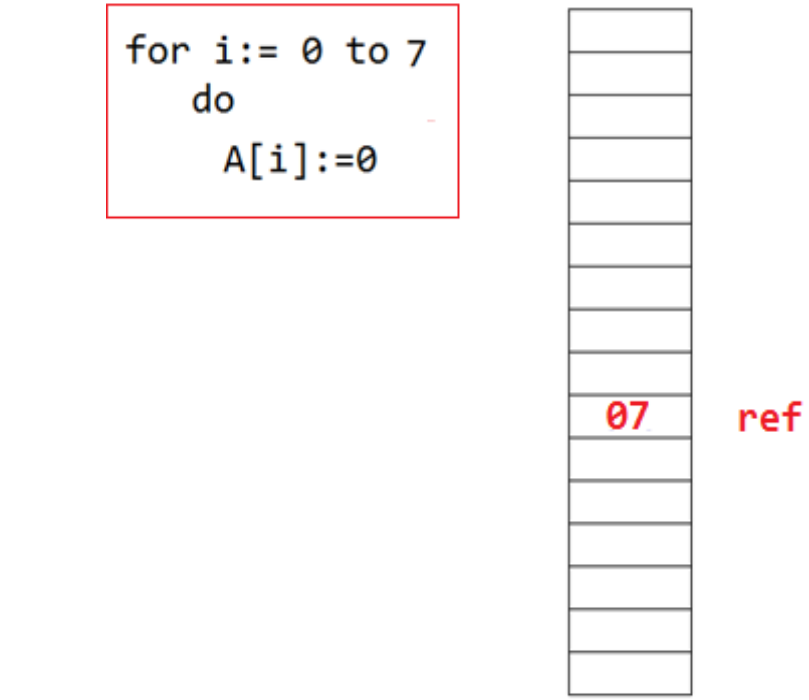


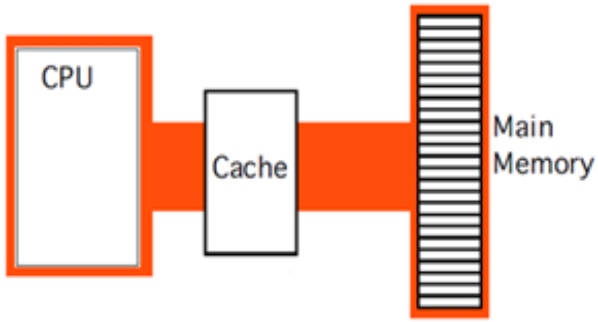
Memory Access and System Clock

Memory speed (access time) is much slower than CPU

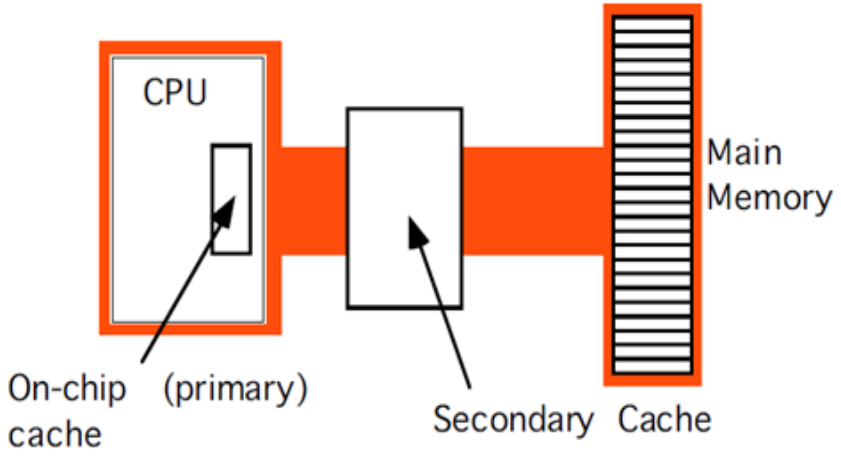
Cache Memory

```
for i:= 0 to 7
    do
      A[i]:=0
```





2-Level Cache System



Programming and Cache Memory