EECE416 Microcomputer Fundamentals
Fall 2021
Dr. Charles Kim

Assignment 4 (200 points)

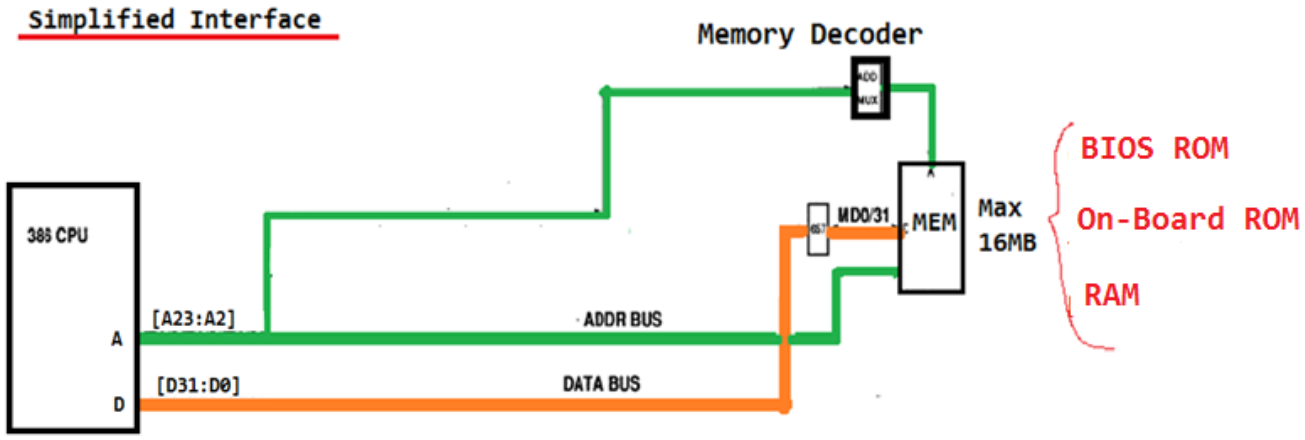
A. Questions

1. For the schematic diagram of ***386-Schematics_1*** which is available from the web page (see the left side of this very assignment), Find (a) the size of ROM, (b) the size of RAM, and (c) draw the memory map for the 386 processor.

2. For the schematic diagram of ***386-Schematics_2*** which is available from the web page (see the left side of this very assignment), design and draw the memory decoder circuitry for ROM and RAM pairs, with following address ranges:
ROM:[0xFB0000 – 0xFB3FFF] and
RAM:[0xF90000 – 0xF9FFFF]

3. For the simplified schematic diagram of the ***KEEN 3310 Personal Computer*** below, draw a complete schematic diagram by adding appropriate number of memories and their decoding circuits for the following 3 types of memory with their corresponding starting addresses:

On-Board ROM (64KB): 0x0E0000
BIOS ROM (64KB): 0x0F0000
RAM (8MB): 0x100000



B.1 Score Distribution and Scoring Rubric for #1 and #2: Total points = 100

	#1 [50]	#2 [50]
50 pts	Correct size of memories and the memory map with neat works of bit patterns to support the answers	Correct design and circuit connection with neat works of bit patterns to support the answer
30 pts	Correct size of memories but incorrect memory map with neat works of bit patterns to support the answers	Correct design but incorrect circuit connection with neat works of bit patterns to support the answer
20 pts	Correct size of memories and correct memory map without supporting works neatly displayed	Correct design but correct circuit connection without supporting works of bit patterns
0 pt	Incorrect answers without detailed bit patterns described	Incorrect decoder circuitry without adequate amount of work displayed

B.2 Score Distribution and Scoring Rubric for #3: Total points = 100

	#3 [100]
100 pts	(a) A neat schematic with all memory types in proper quantities are correctly connected to the address lines, data lines, and control lines to the 386 processor accompanied with correct memory decoding circuits, and (b) a description of the process and manual works which led to the resultant schematics.
80 pts	(a) A neat schematic with all memory types in proper quantities are correctly connected to the address lines, data lines, and control lines to the 386 processor accompanied with somewhat incorrect memory decoding circuits, and (b) a description of the process and manual works which led to the resultant schematics.
60 pts	(a) A neat schematic with all memory types in proper quantities are correctly connected to the address lines, data lines, and control lines to the 386 processor accompanied with correct memory decoding circuits, but there is no (b) description of the process and manual works which led to the resultant schematics.
50 pts	(a) A neat schematic with all memory types in proper quantities are correctly connected to the address lines, data lines, and control lines to the 386 processor accompanied with somewhat incorrect memory decoding circuits, and there is no (b) description of the process and manual works which led to the resultant schematics.
20 pts	(a) Incomplete schematic and (b) incomplete description
0 pt	No meaningful work

C. Submission: Work on a paper or on word processing software or drawing application, and send me an electronic copy (file) of your work via email or Slack. Name your file as follows: **416Assign4_LastName.xxx** (xxx for file type, docx, doc, pdf, png, etc)

D. Submission due: Before 8:00pm Wednesday October 13, 2020

E. Extension Request of Submission: Usually granted upon request